Power driven placement with layout aware supply voltage assignment for voltage island generation in dual-Vdd designs

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Outline

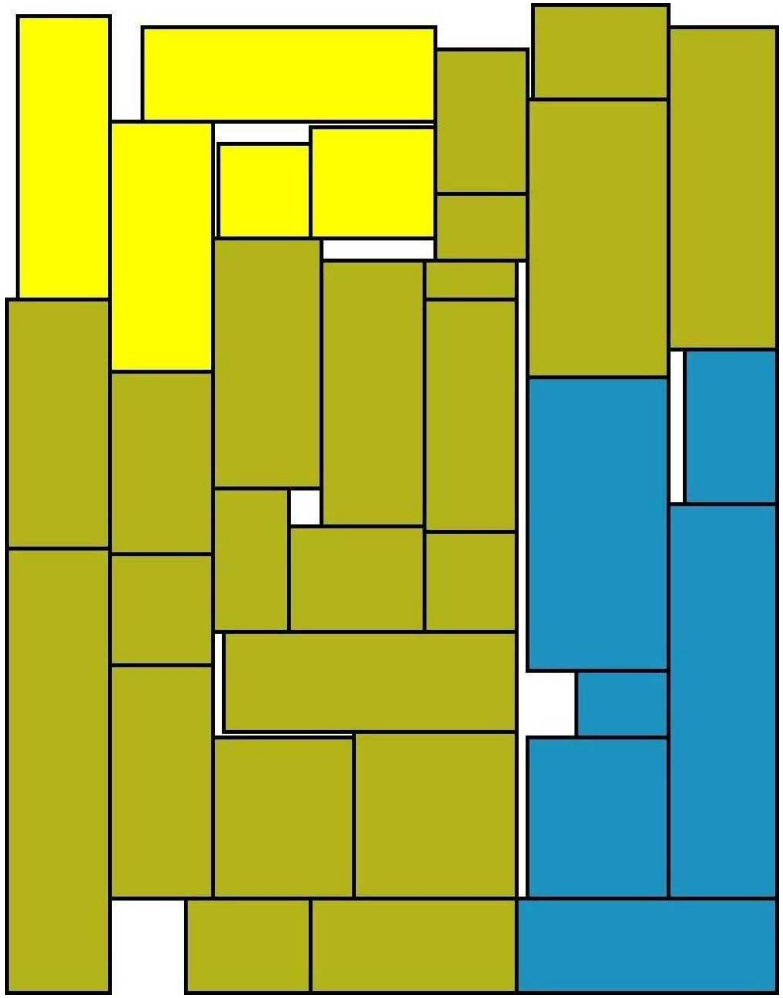
- Introduction and related works
- Motivation
- Our flow
- Implementation
- Results
- Conclusion

Introduction

- Lowering supply voltage to save energy
  - Dynamic power
  - Static power
- Low voltage causes slowdown of devices.
- Multiple supply voltages
  - High voltage on critical paths
  - Low voltage on other paths

Multiple Supply Voltages

- Macro block level
  - Design planning
  - J. Hu et al., ISLPED'04
- Cell level (our focus)
  - Different cells have different voltages.
  - More flexible



New Challenges

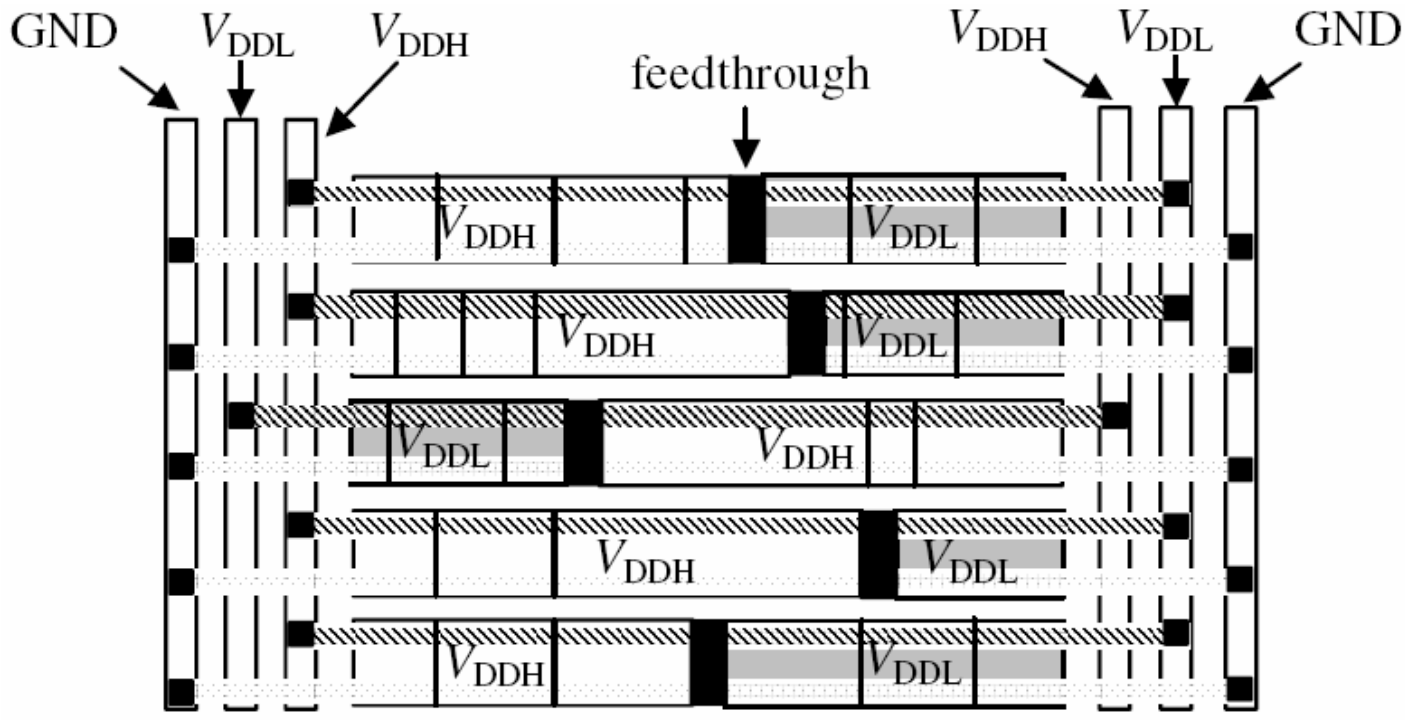
- Level converter
  - VddL cells can’t drive VddH cells directly.
- Layout
  - Power delivery networks become complicated.
  - Cells under the same voltage should be clustered.

Related works: voltage assignment

- Works on the netlist, based on STA.
- Substituting VddH cells with VddL cells.
- Clustered voltage scaling (CVS)
  - K. Usami and M. Horowitz, ISLPED'05
- ECVS
  - C. Chen et al., TVLSI'01
  - S.H. Kulkarni et al., ISLPED'04

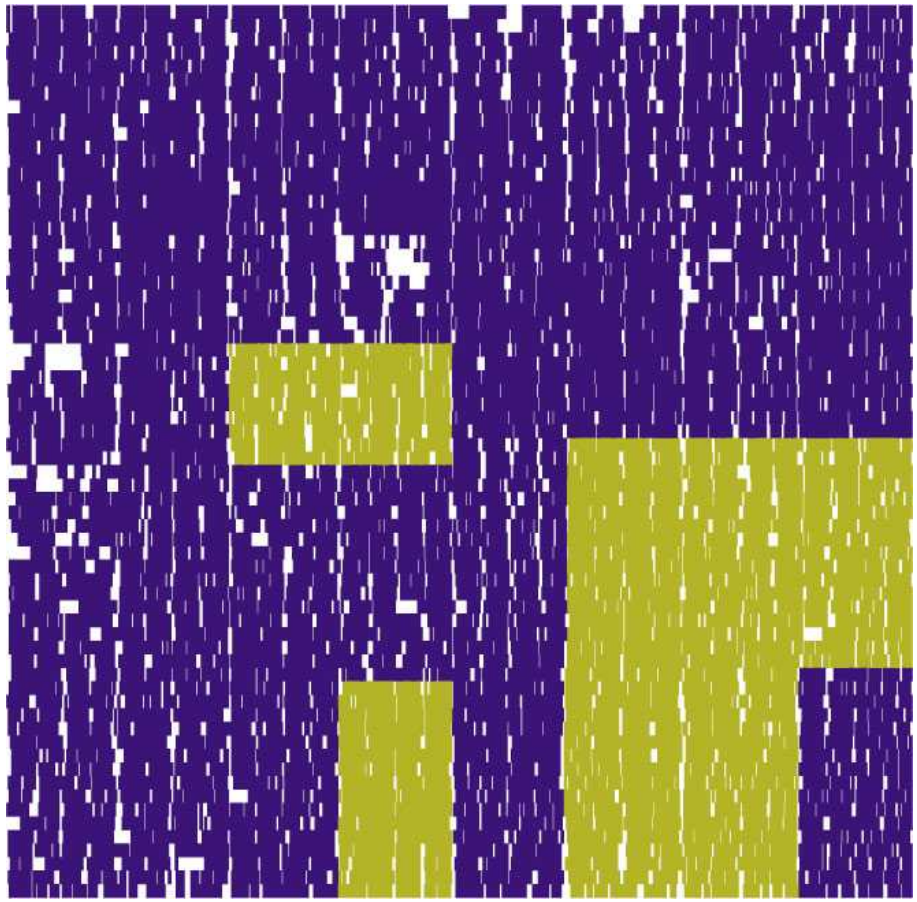
Related works: cell placement

- Row based dual Vdd placement
  - C. Yeh et al., DAC'99



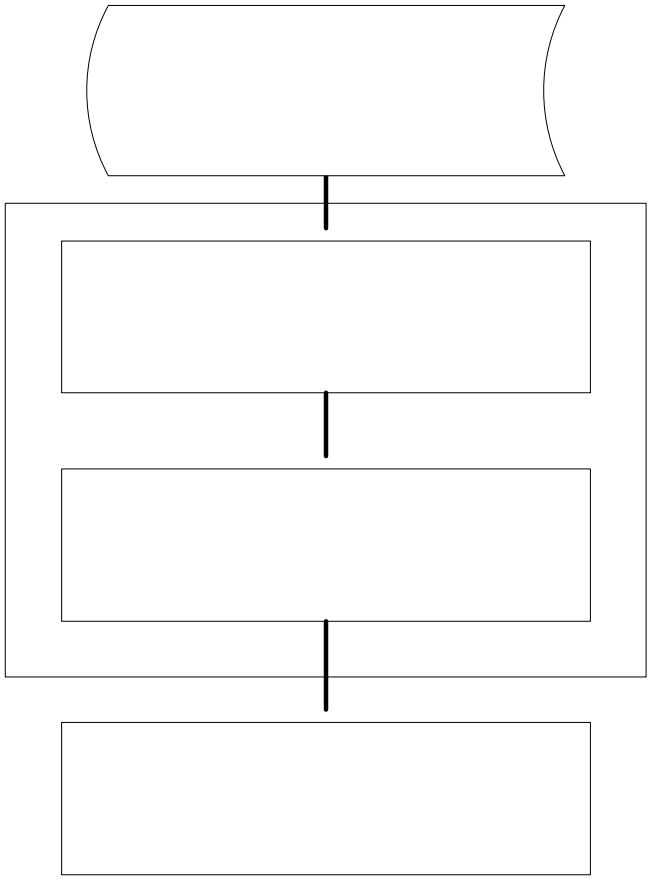
Related works: cell placement

- Region based – voltage island



Motivation

- Voltage assignment is usually performed before cell placement.
  - Hard to estimate interconnect delay.
  - Large wire length penalty caused by clustering in placement.

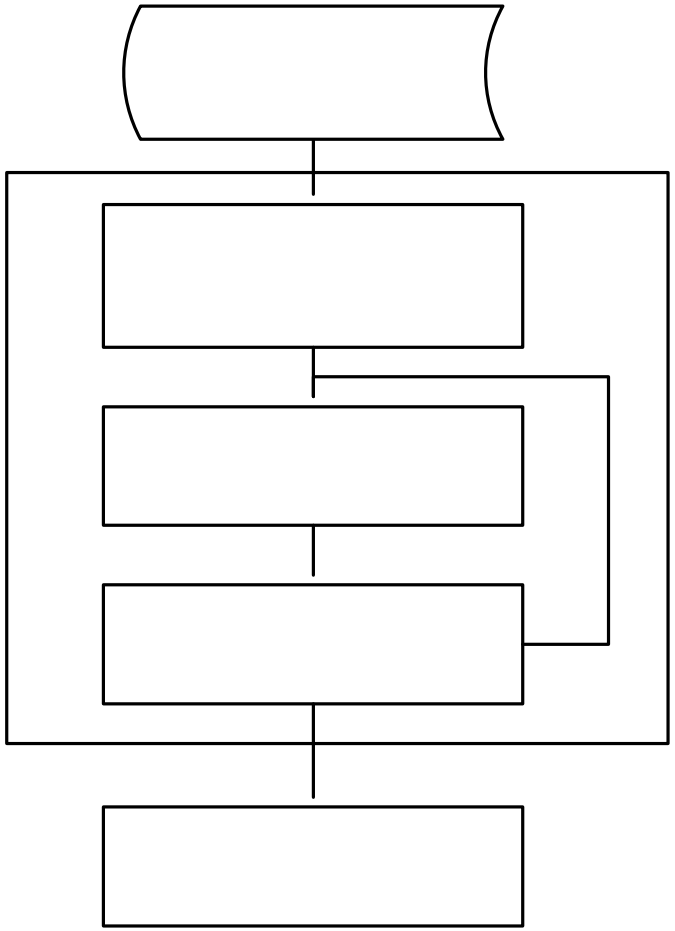


Motivation

- Solution
  - Layout aware voltage assignment.
  - Voltage island generation during placement.
- Similar approaches
  - DAC'03, R. Puri, D. Pan, et al.
  - Prof. Patrick Madden
- Goal
  - Reduce power under timing constraints
  - Implement fine-grained voltage islands with small overheads

Our flow

- Pre-layout voltage assignment is not required.
- Assign supply voltages according to a placement result.
- Iterations between voltage assignment and placement refinement.



Partition based placement

- Our placement algorithm is based on Capo 9.2.
- Partition based placer
  - Recursively partition every bin, and associated netlist (hypergraph).
  - Minimize wirelength -> minimize cut number.
  - Multilevel hypergraph partition.

Initial coarse placement

- The first several passes of global placement.
- All cells are assumed to operate under VddH.
- Timing and power driven net weighting
  - Static timing analysis
  - Consider signal activity (switching probability)

$$W = \begin{cases} (1 + c \times \alpha) \times \left(1 + \dfrac{T_0}{T_0 / N + slack}\right), & slack > 0 \\ (1 + c \times \alpha) \times (1 + N), & else \end{cases}$$

Initial voltage assignment

- Goal
  - Most VddL cells are physically clustered.
- Seed growth manner
  - First select some seed bins, so that most cells in seed bins are VddL cells. (physical adjacency)
  - Assign VddL to some other cells if possible. (logical adjacency)

Initial voltage assignment

- Select seed bins
  - Calculate the tendency of using VddL for every cell.

$$\text{tendency} = \begin{cases} \dfrac{\left(G_{\text{self}} + \gamma G_{\text{LC}}\right) \times \text{slack}}{\Delta\text{delay}}, & \text{slack} > \Delta\text{delay} \\ 0, & \text{else} \end{cases}$$

  - Bins where average cell tendency above a threshold is selected as VddL seed bins.
- Tendency values should be updated after cells in a seed bin is assigned to VddL.

Initial voltage assignment

- Growth
  - Focus on logical expansion of VddL cells.
  - Visit VddH cells in decreasing order of tendency.
  - Since the gain on level converter is considered in tendency calculation, VddH cells connecting to VddL cells are more likely to be assigned to VddL.

Placement refinement

- Goal
  - Locally adjust cell locations in order to cluster cells with the same supply voltage.
  - Consider the change in path delay.
- Implementation
  - Merge adjacent bins, and repartition the netlist, considering clustering requirement.
  - Net re-weighting after voltage assignment.
  - Add pseudo edges to pull cells closer.

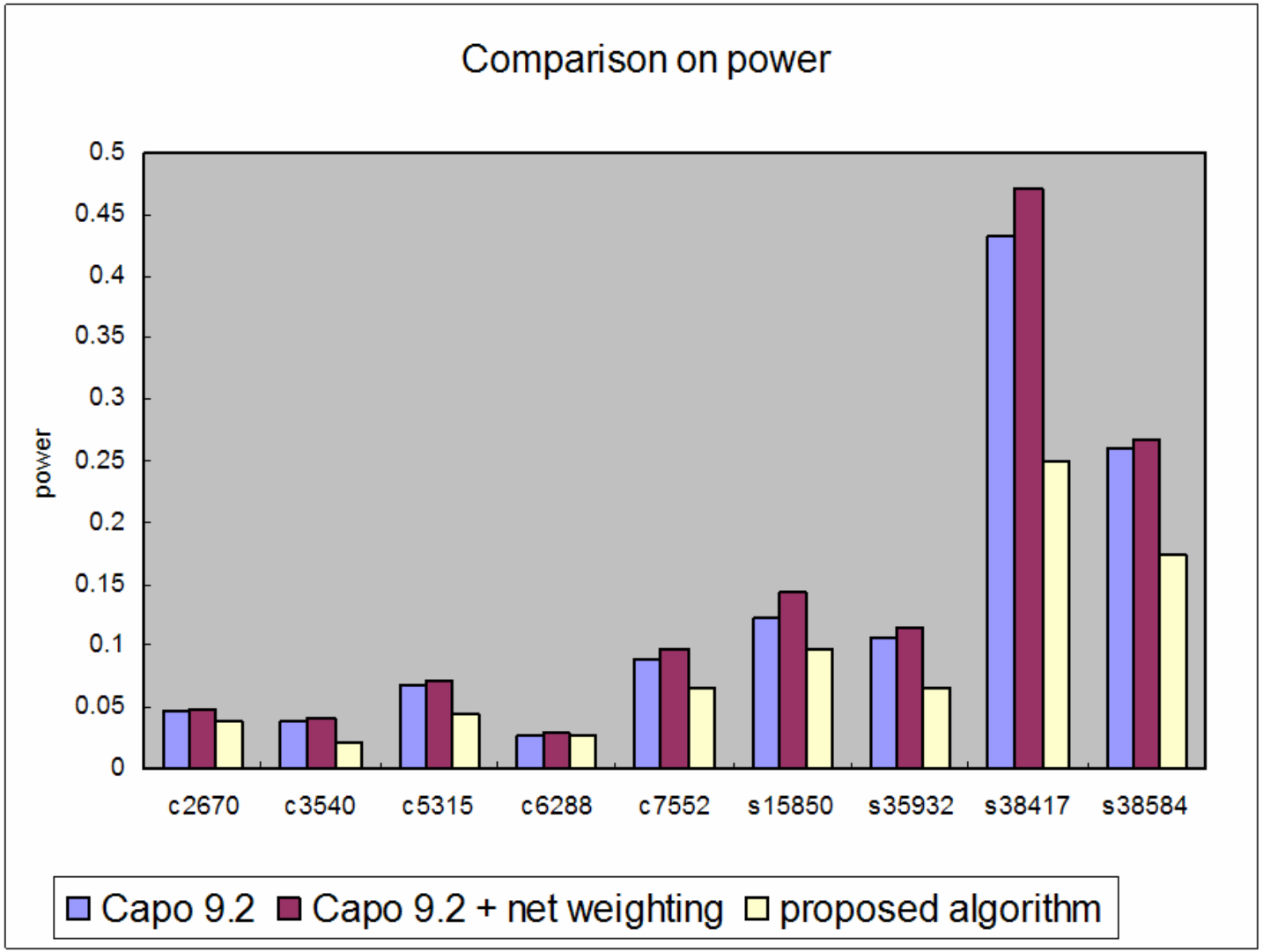
Incremental voltage assignment

- Goal
  - Form VddH or VddL islands
- Implementation
  - For bins where the portion of VddH cells is larger than a threshold, use VddH for all cells.
  - For bins where most cells are VddL cells, try to use VddL for all cells.
  - If a bin still contain VddH and VddL cells after many iterations, use VddH for this bin.

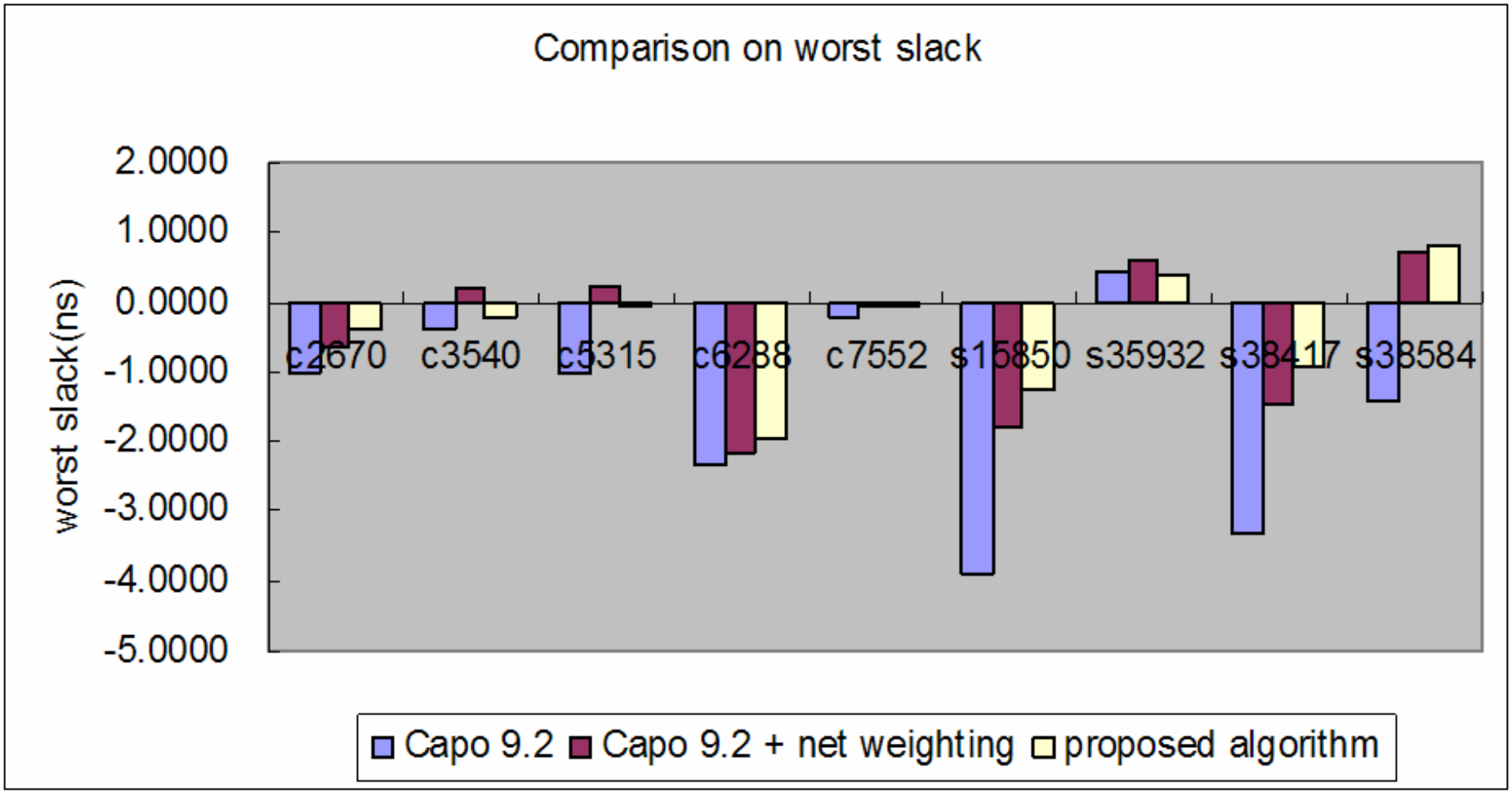
Experimental Results

- Benchmarks
  - ISCAS 85, 89 benchmarks
- VddH = 1.8V, VddL = 1.2 V
- We compare 3 algorithms
  - Capo 9.2 with default parameters
  - Capo 9.2 with our net weighting
  - Proposed algorithm

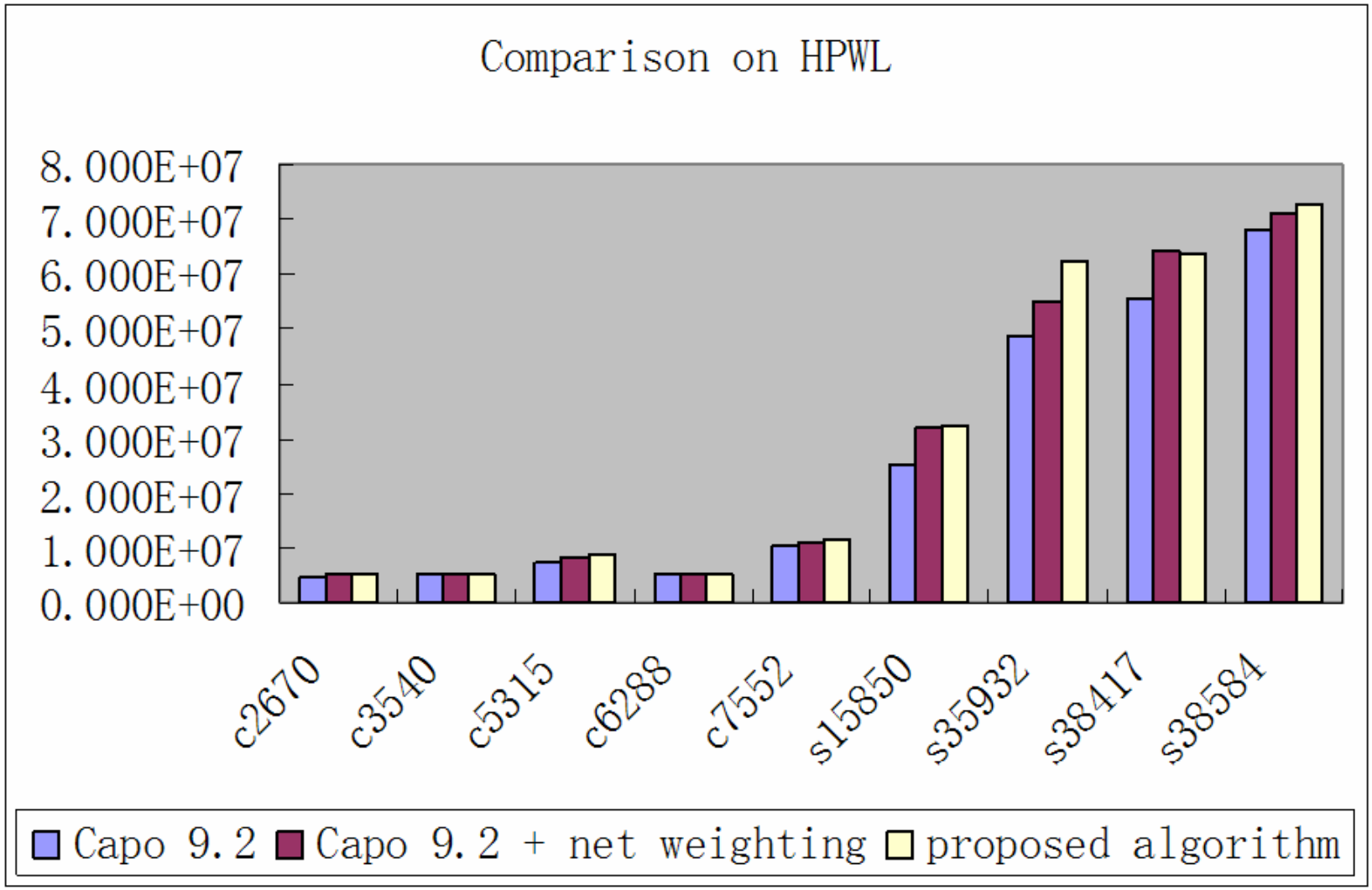
Experimental results



Experimental results



Experimental results



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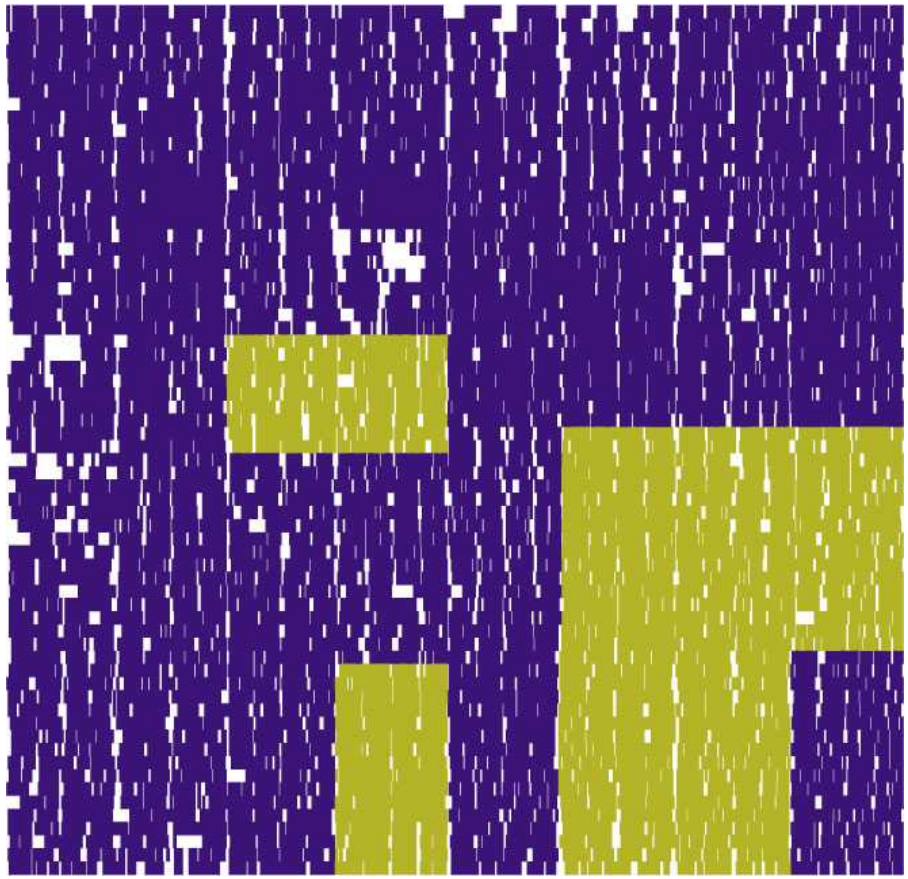

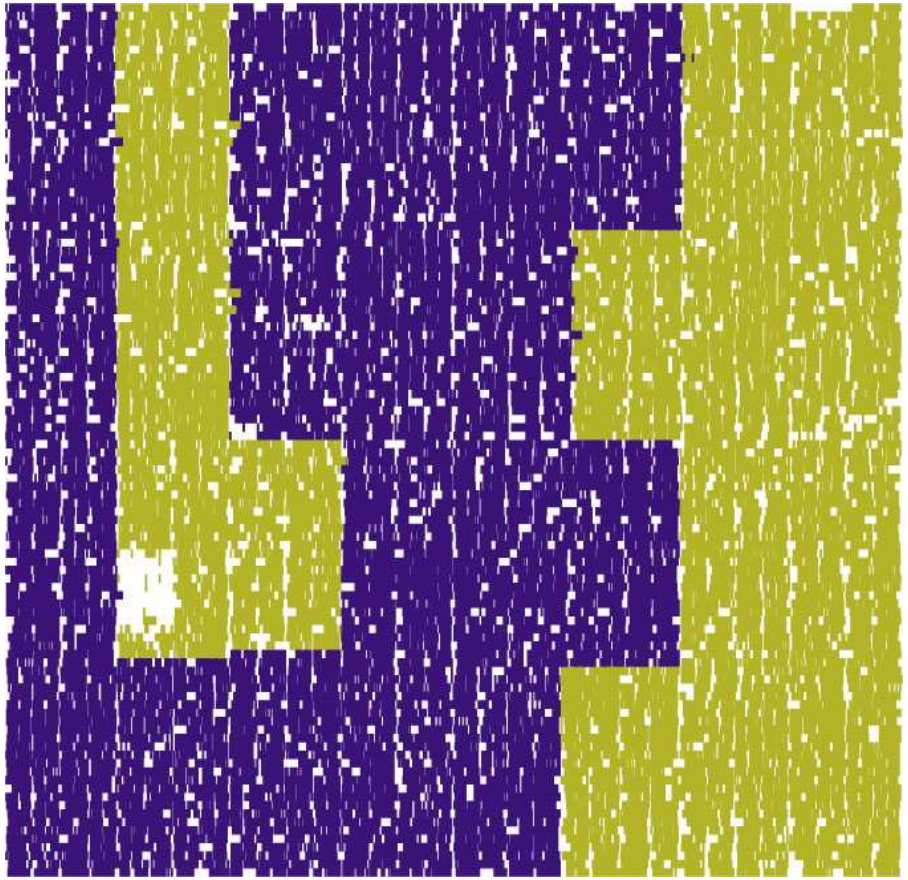

Conclusion

- Our method is effective to implement voltage island without significant wirelength increase.
- Further work can explicitly consider level converter insertion during this flow.

Thank you.