Diagonal Routing in High Performance Microprocessor Design

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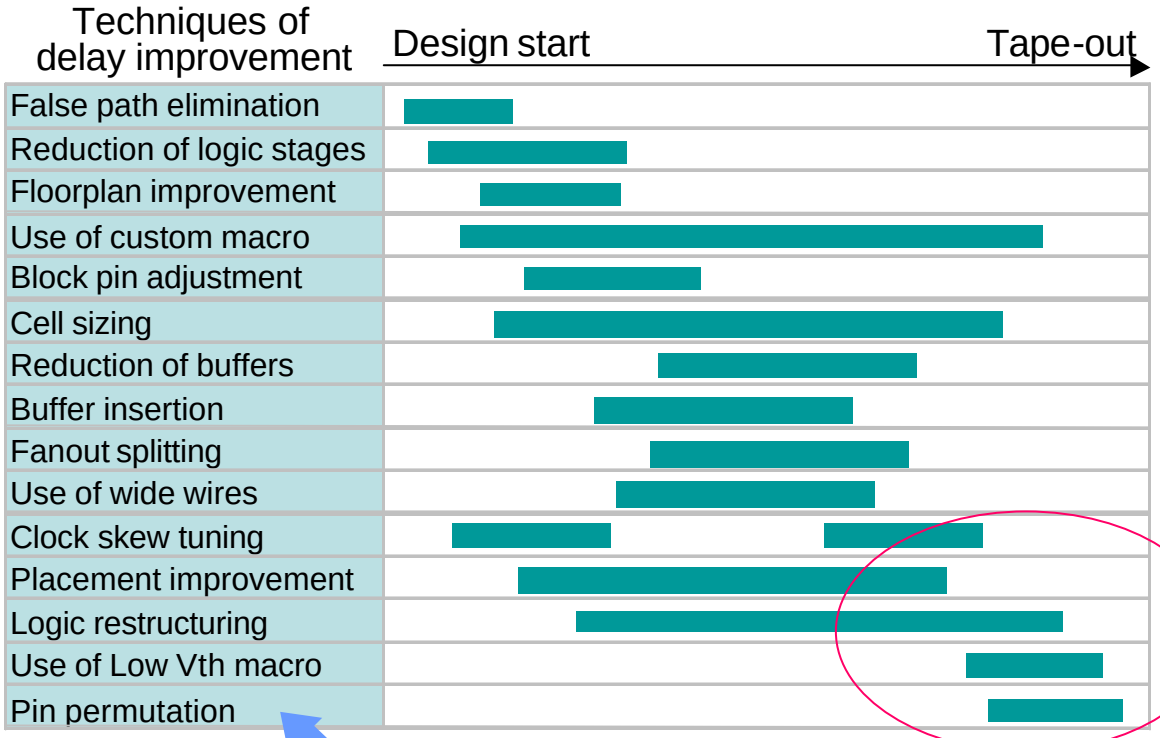
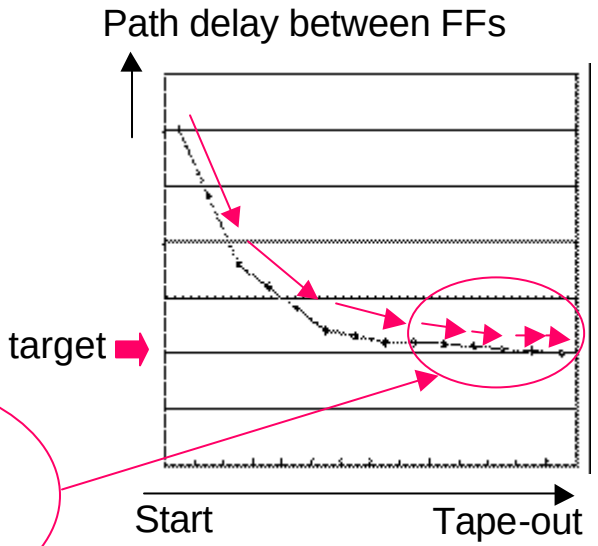
Outline

- Motivation
- Effect estimation of diagonal routing
- Implementation of CAD tools
- Results
- Conclusions

Motivation

- It is meaningful to provide designers of high performance microprocessors with new methods to improve delay.





Diagonal routing

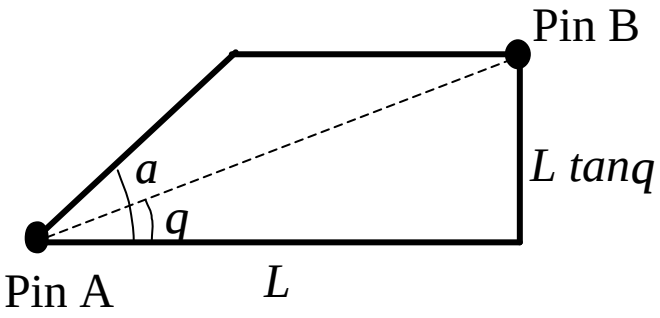
Logical and physical designs are tuned to the last pico-second!

Motivation (Cont'd)

- Difficulty of diagonal routing in LSI design
  - The difficulty lies in to support diagonal routing in all related CAD tools such as routing, timing analysis, noise analysis, layout verification and manufacturing data generation.
- Our approach
  - A diagonal routing technique that uses diagonal wiring is partially applied to critical nets.
  - Limited usage of diagonal wires minimizes the enhancement needed for the existing CAD system.

Effect estimation - theoretical

- Routing length of a net



  - Manhattan

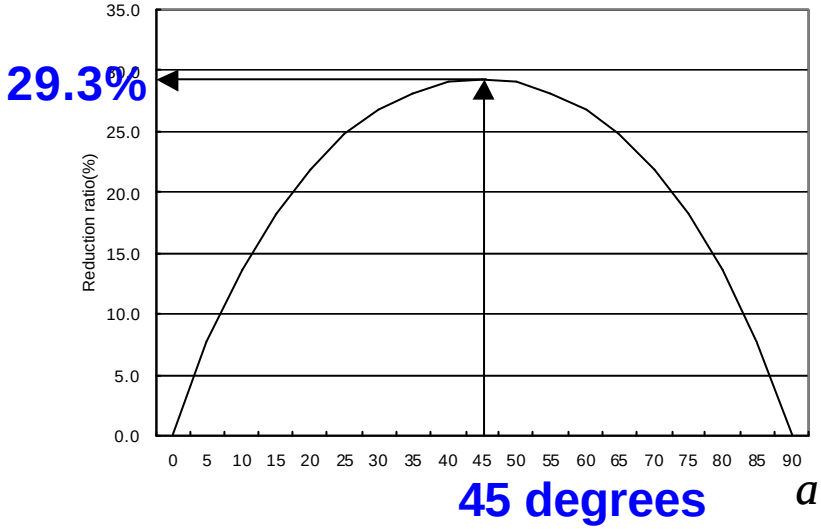
    Lxy = L(1+tan q)

  - Diagonal

    Langle(a) = L tan q /sin a + L(1- tan q /tan a)

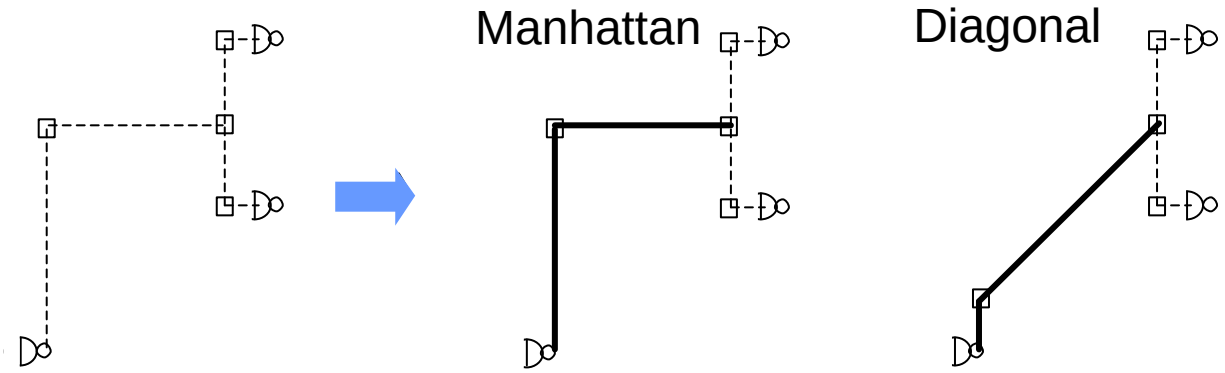
- Reduction of routing length

Reduction = (Lxy-Langle(a))/Lxy



Effect estimation - actual

- The two lengths are compared for 6,000 long distance nets in the actual design. The net length is reduced by about 12% on average by diagonal routing.

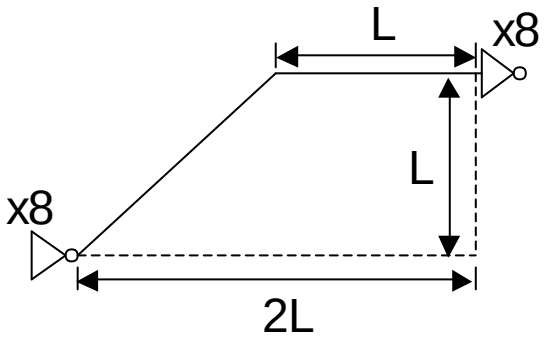


Unit: grid

	Manhattan	Diagonal	difference
Total length	25,835,198	22,569,954	3,265,244
Average net length	4,090	3,573	517

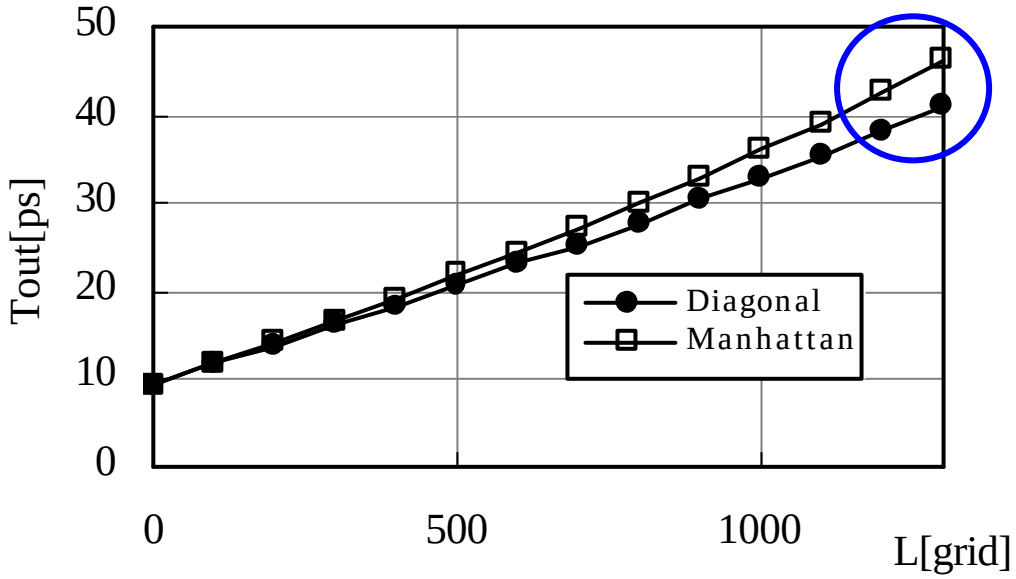
Effect estimation - delay

- When a net length is 1500, the improvement of delay is about 7 pico-seconds.
- The improvement is larger when a diagonal routing is applied to a longer net.



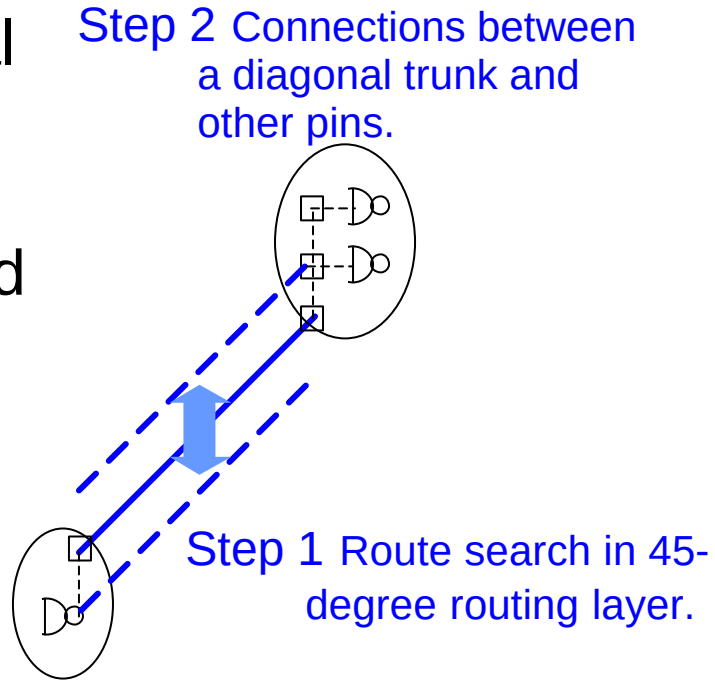
Diagonal routing can reduce the net length by about 20% in this case.

Effective!



Implementation Strategy

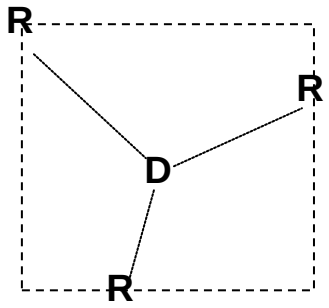
- We made these modifications with a target completion deadline of at most six months.
- This new diagonal routing function is added to our current design methodology.
- We need to implement a diagonal routing with the minimum development cost.
- A diagonal routing is implemented by the simple two steps.



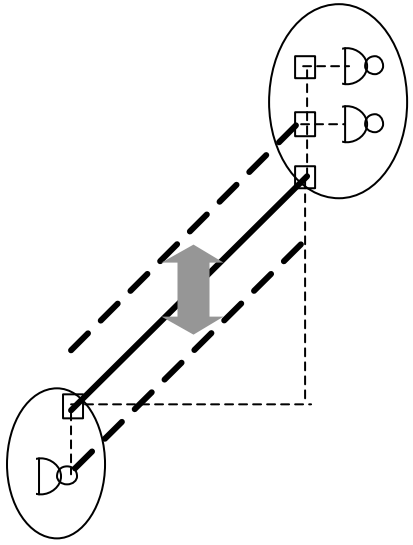
Routing algorithm

- Pseudo code

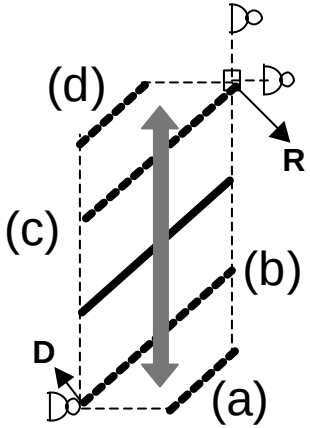
```
Diagonal_routing(P)
  flag = Routable_check(P)
  if flag == FALSE {
    W,V = Manhattan_routing(P)
  }
  else {
    S = Steiner_generation(P)
    R = Make_receiver_group(S)
    D = Select_driver(P)
    Wdiag = Diagonal_search(D,R)
    Wires,Vias = Manhattan_routing(P,Wdiag)
  }
  return(Wires,Vias)
end

Diagonal_search(D,R)
  L = Diagonal_length(D,R)
  if ( L <  a  ) then
    return(NONE)
  }
  else {
    x = Horizontal_distance(D,R)
    y = Vertical_distance(D,R)
    if ( x > y ) {
      diag_wire = Horizontal_search(D,R)
    }
    else {
      diag_wire = Vertical_search(D,R)
    }
    return(diag_wire)
  }
}
```



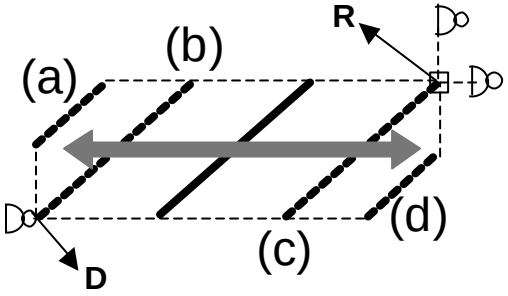
Routable check



Diagonal search



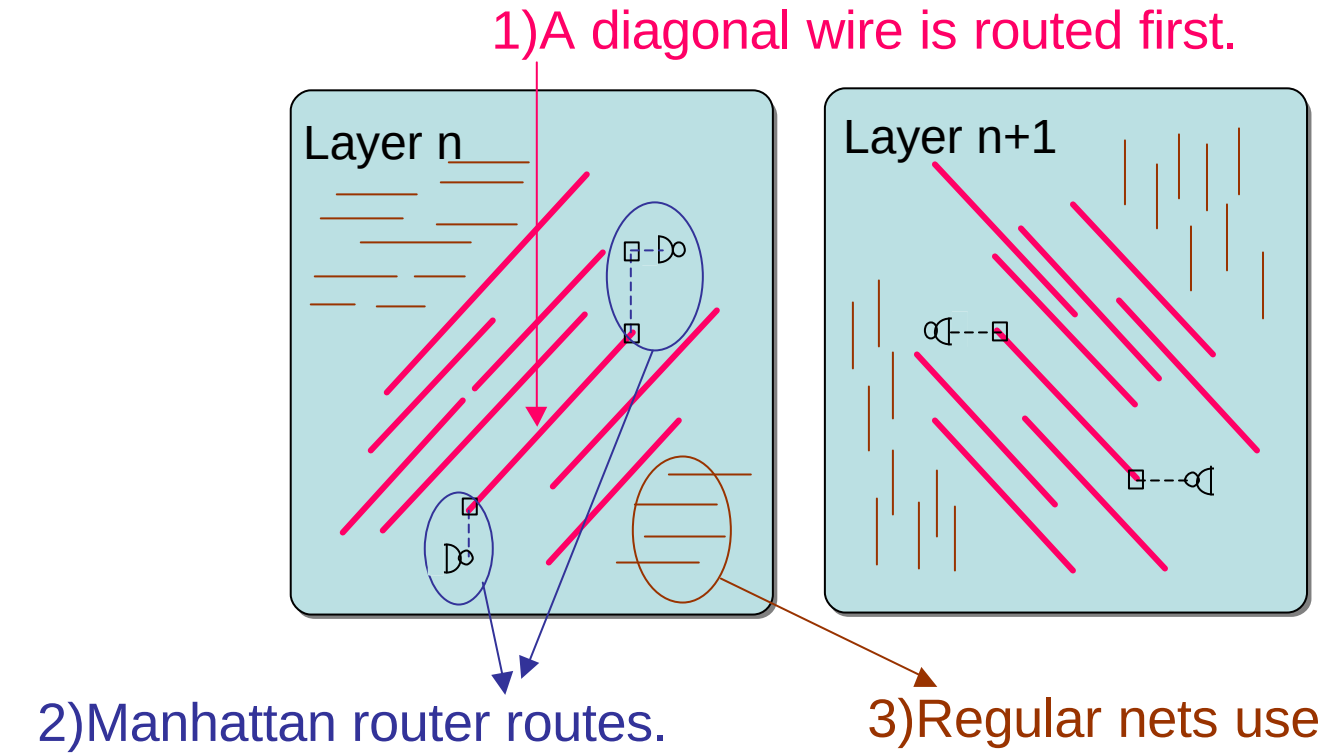
Vertical search



Horizontal search

Share with Manhattan routing

- 45 and 135 degree layers are assigned to upper layers, which have smaller wire resistance.
- Channels left unused on those layers are used to route regular nets with a conventional Manhattan routing.

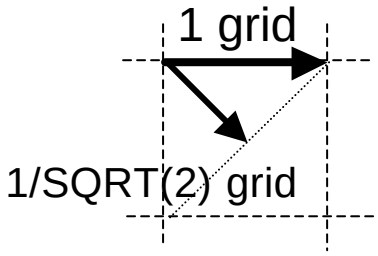


Capacitance extraction

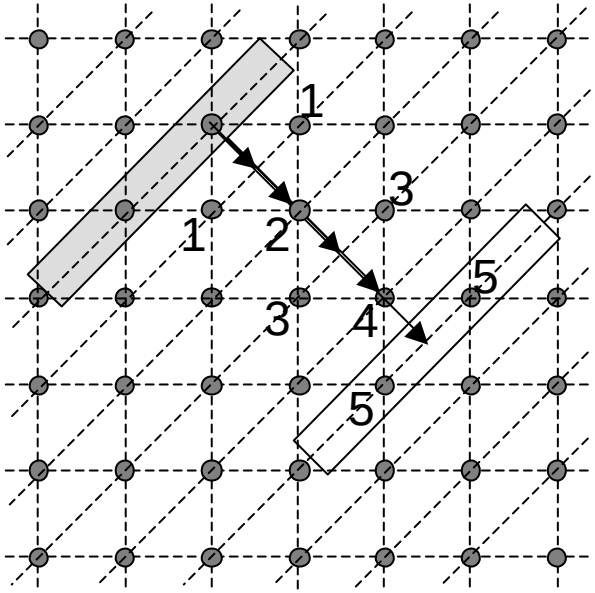
- Additional capacitance table

  Gap between Manhattan wires : 1 gird*N

  Gap between Diagonal wires : 1/SQRT(2) grid*N



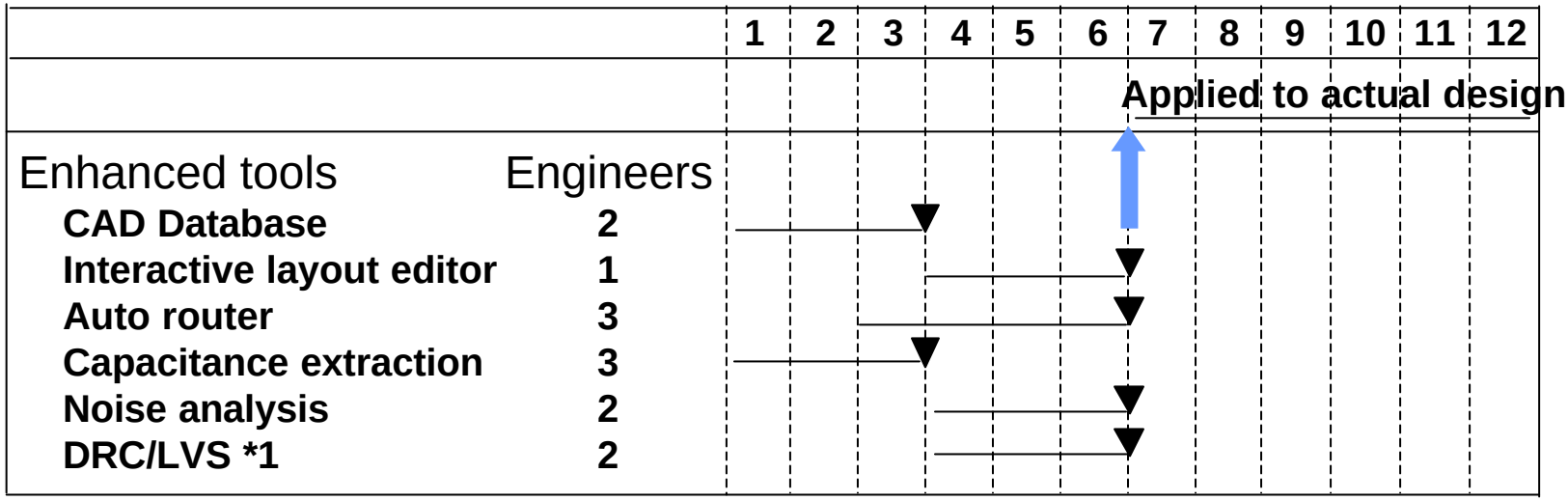
- Search for adjacent wires



- If *N* is even, the search point lies on the regular grid.
- If *N* is odd, the search point does not lie on a regular grid. Then, two regular grid points nearest to the search point are checked.

Development schedule

- Since it is necessary to complete all modifications within six months, we developed according to the following schedule.

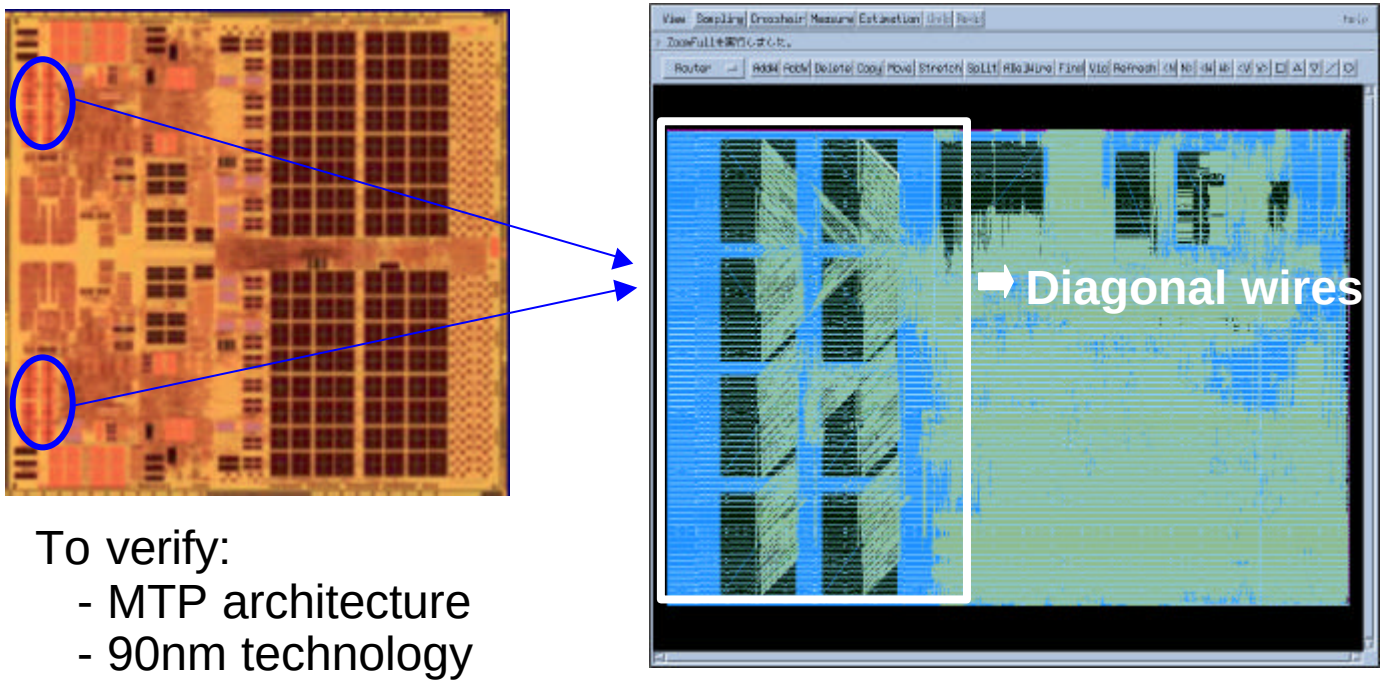


*1 This includes rule modification for Calibre from Mentor Graphics.

- Total man-power is about 30 man-months.

Applied prototype chip

- Prototype MTP chip [1]

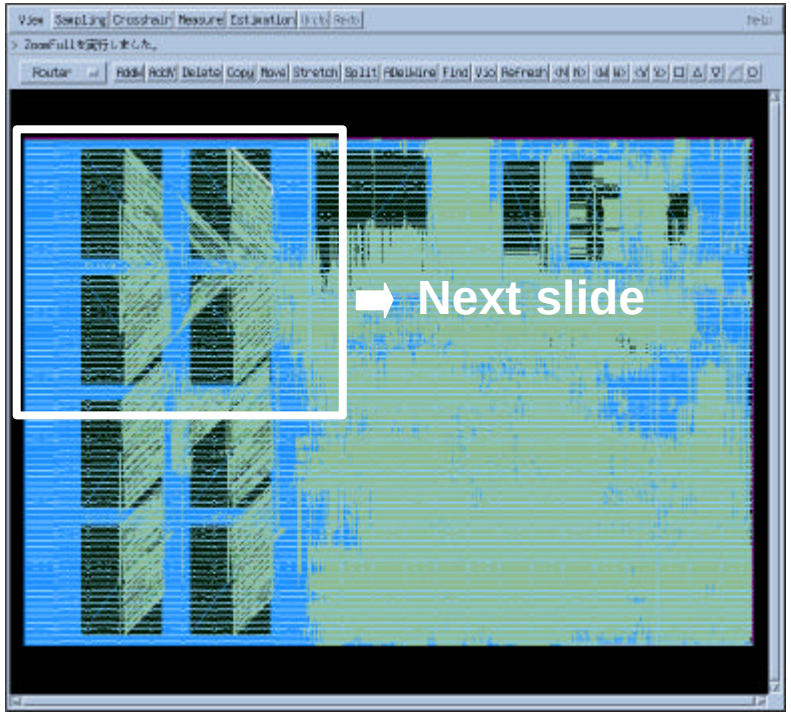


To verify:
- MTP architecture
- 90nm technology
- major custom designs

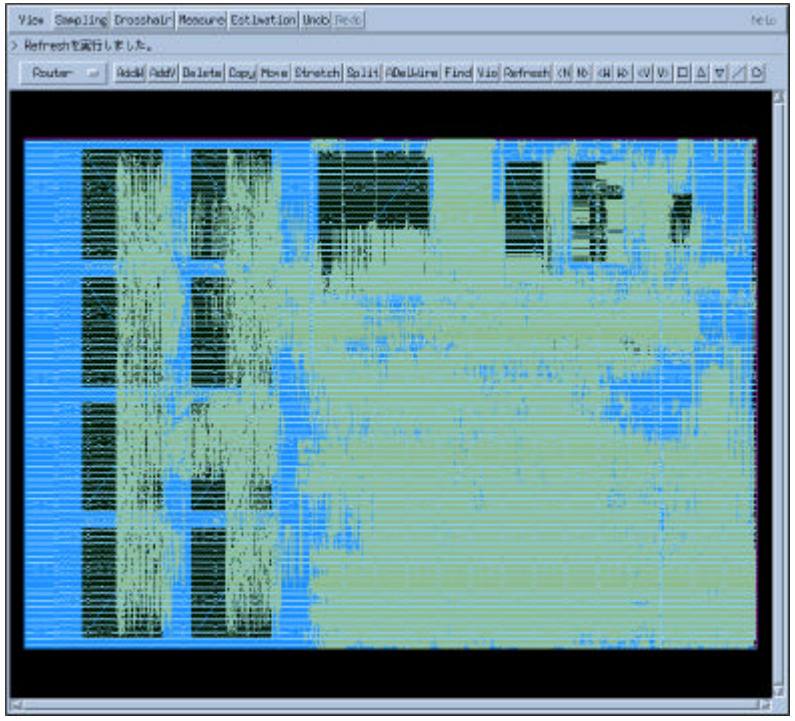
[1] Takumi Maruyama, "SPARC64 VI: Fujitsu's Next Generation Processor", presented at the microprocessor forum, 2003.

Diagonal wires

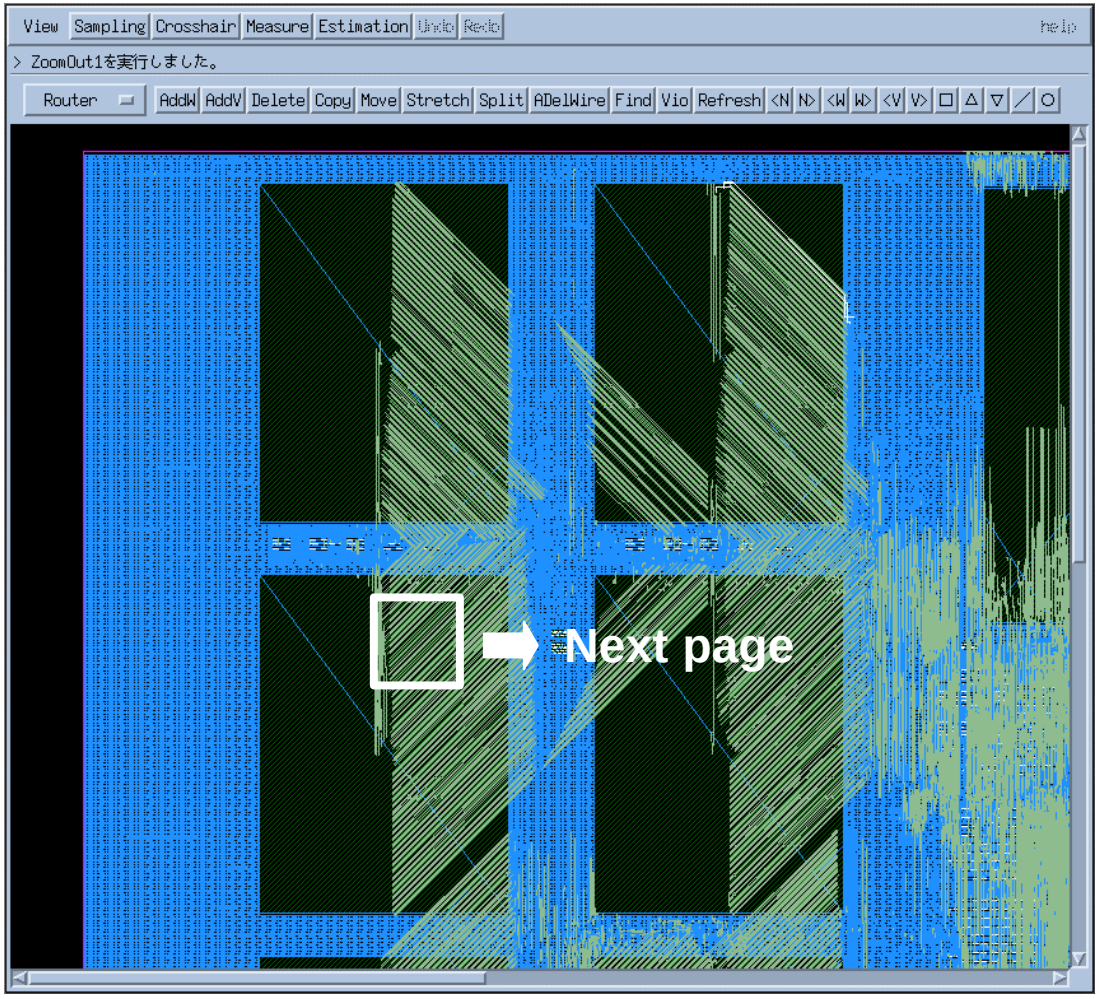
- Comparison between diagonal and Manhattan
  - Diagonal



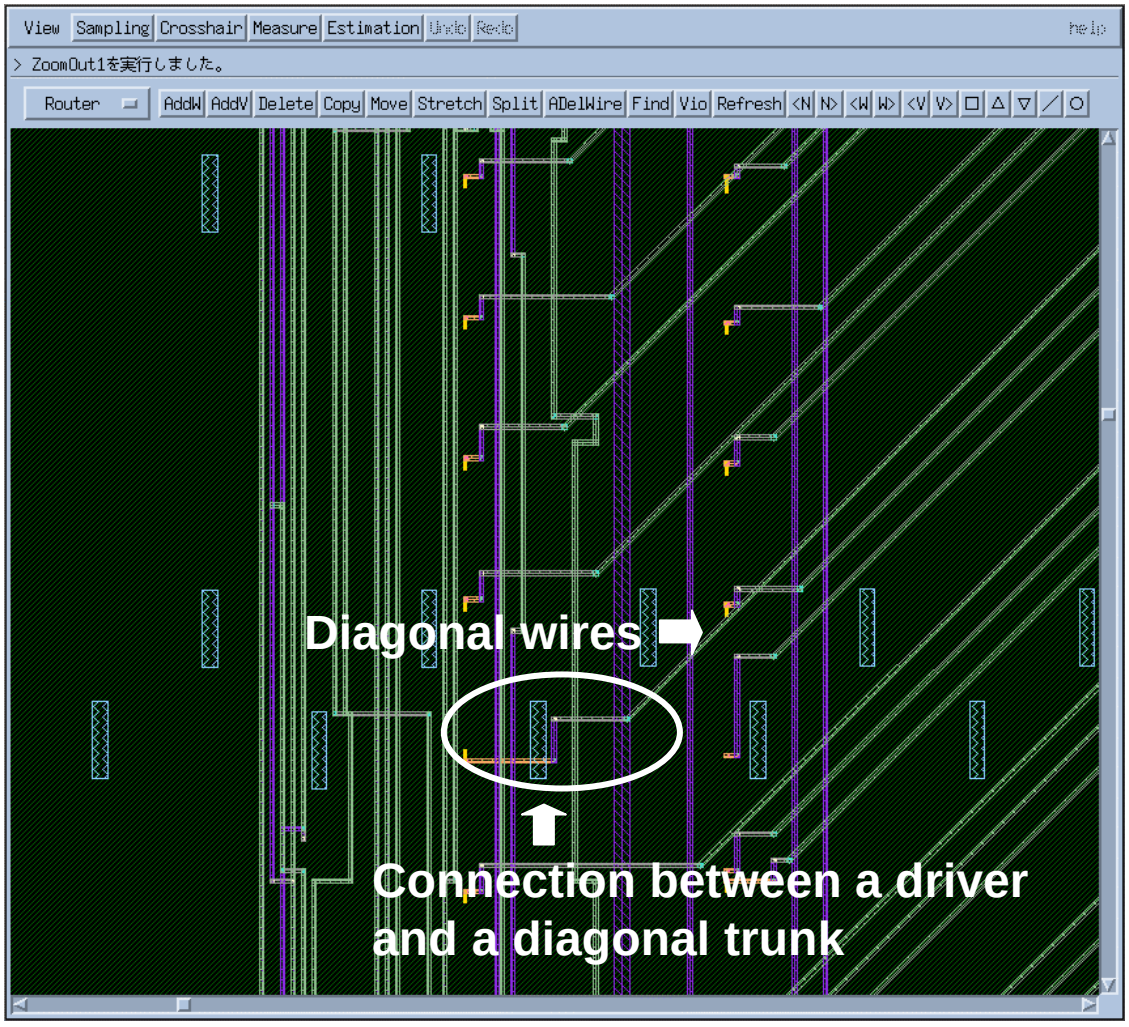
  - Manhattan



Diagonal wires (cont'd)

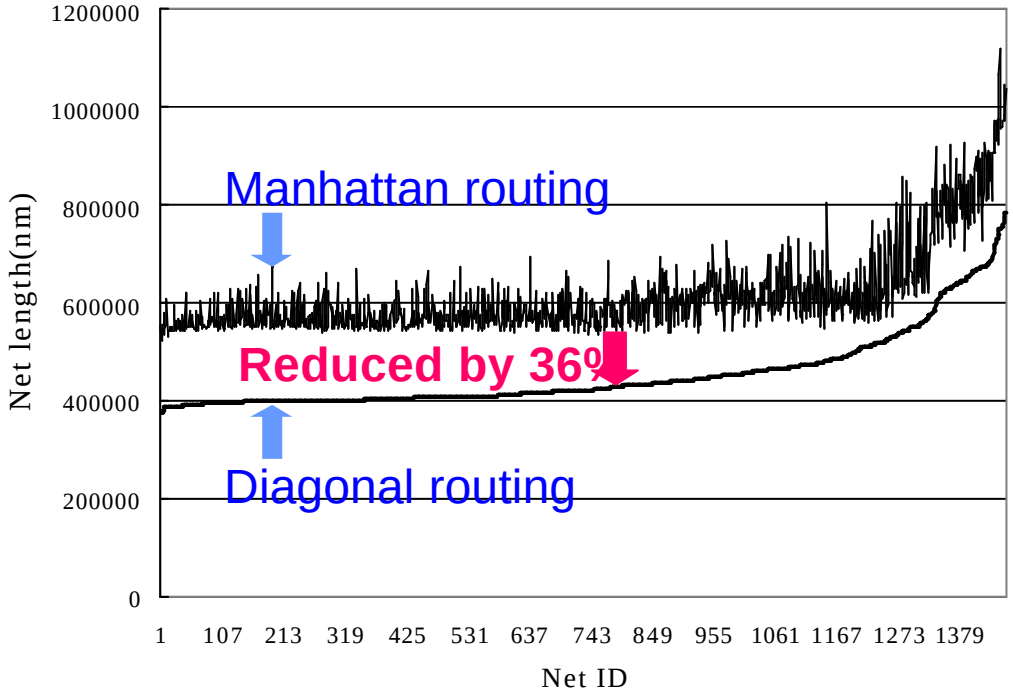


Diagonal wires (cont'd)



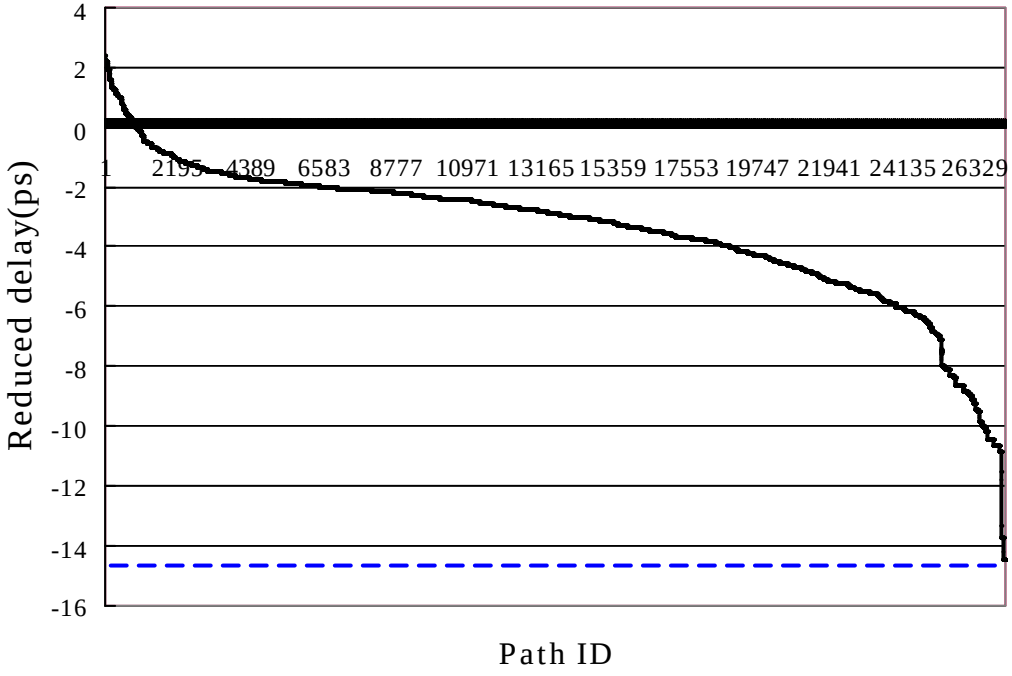
Effects - length

- Net length reduction
  - Diagonal routing reduces the net length by about 36% on average.
  - This 36% exceeds theoretical maximum value 29.3%. The reason is that the total detour of the net with a diagonal routing is smaller than that with the Manhattan routing.



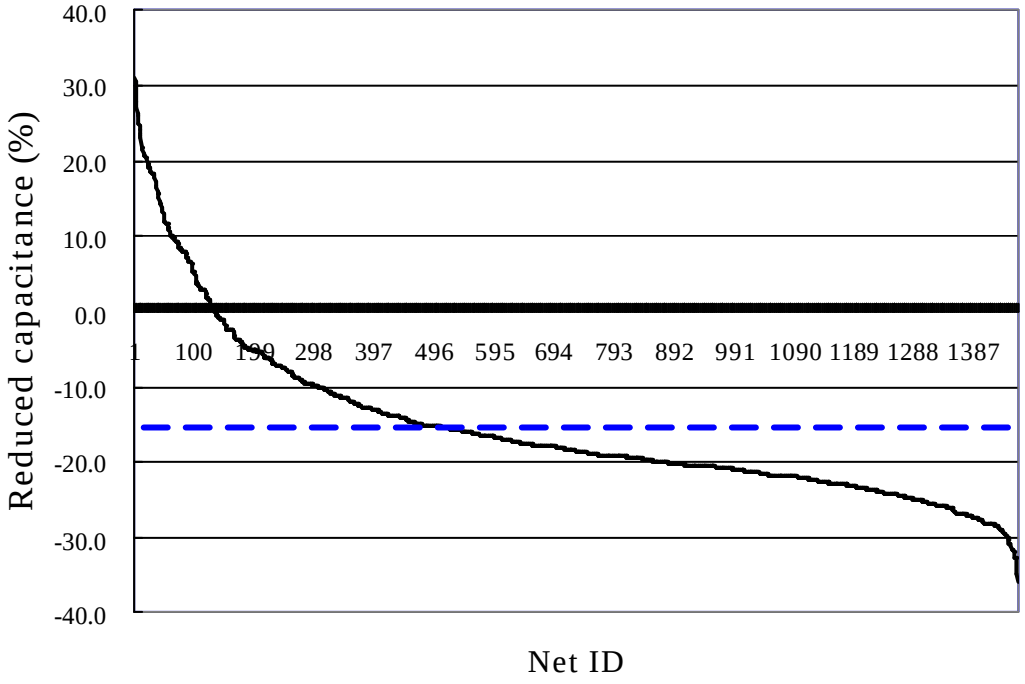
Effects - delay

- Path delay reduction
  - When a diagonal routing is applied to a critical path, path delay is improved by up to about 14 pico-seconds per net on a path. This improvement is more than the delay of a gate with no load.
  - The average improvement is about 6 pico-seconds.



Effects - noise

- Noise reduction
  - Coupling capacitance that can cause cross-talk noise is less when diagonal routing is applied. This is due to the associated reduction of net length.
  - we can expect overall cross-talk is reduced by about 15%.



Average -15%

Cross-talk reduction

Conclusions

- Conclusions
  - A new diagonal routing function is added to our current design methodology within a short period.
  - We provide microprocessor designers with diagonal routing capability as a new means to improve path delay.
  - We applied a diagonal routing to an actual prototype chip of a microprocessor with two CPU cores. We were able to reduce the net length by 36% per net on average, and path delay by up to 14 pico-seconds.
- Future work
  - To increase the number of nets to which we can apply diagonal routing, further enhancements are needed, such as automatic net selection and floorplanning & cell placement that make diagonal routing more effective.