A Novel Framework for Multilevel Full-Chip Gridless Routing

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Outline

- Introduction
- V-Shaped Multilevel Framework
  - Design Flow
  - Channel Density Initialization
  - Uncoarsening Stage
  - Coarsening
- Experimental Results
- Conclusion

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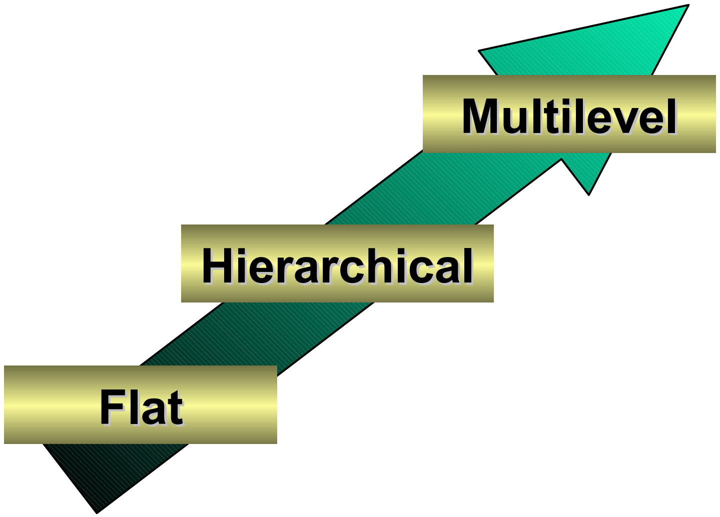
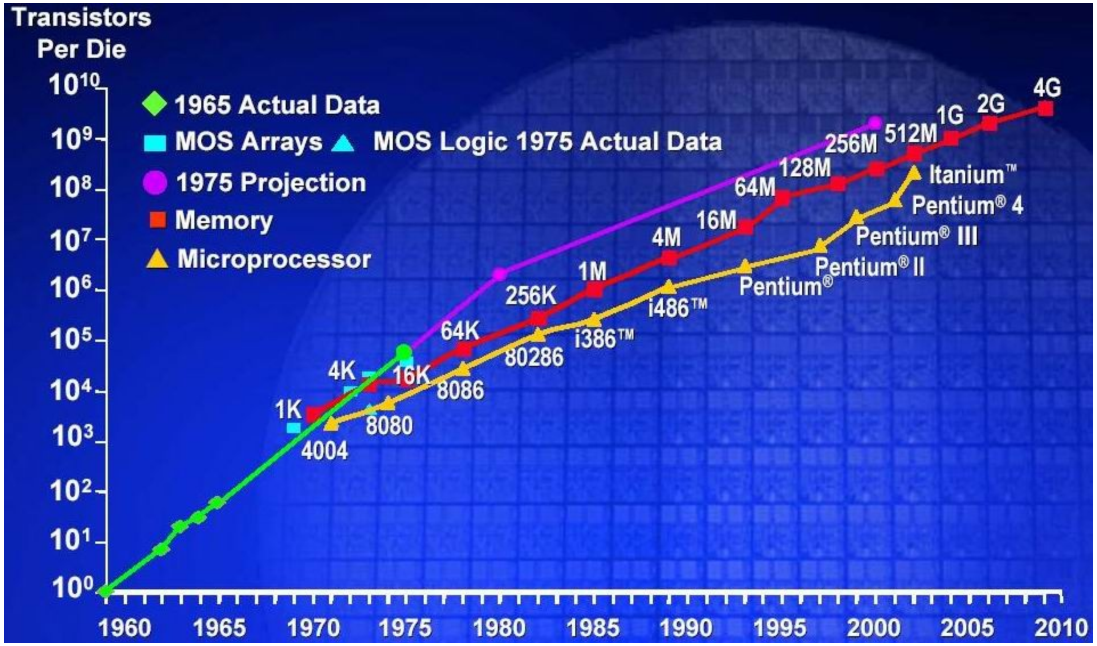
Framework Evolution

- Design complexity is growing at a dramatic speed
- Billions of transistors may be fabricated in a single chip for nanometer technology
- Need frameworks for very large-scale designs
- Framework evolution in CAD tools:
  - Flat → Hierarchical → Multilevel

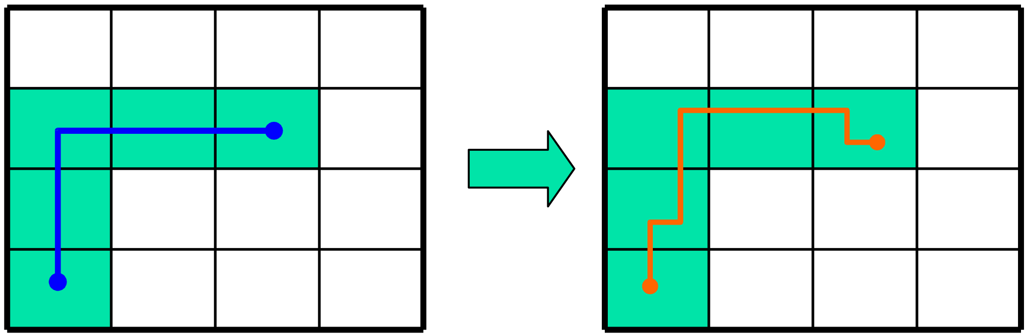




Source: Intel at ISSCC-03

Flat Routing

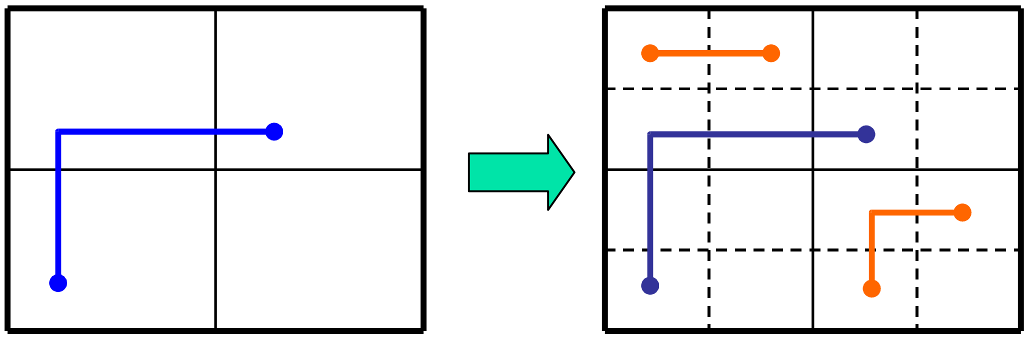
- Many flat algorithms for routing have been proposed



- Drawback
  - Hard to handle large problems

Hierarchical Routing

- Divide and conquer
  - Have good scalability

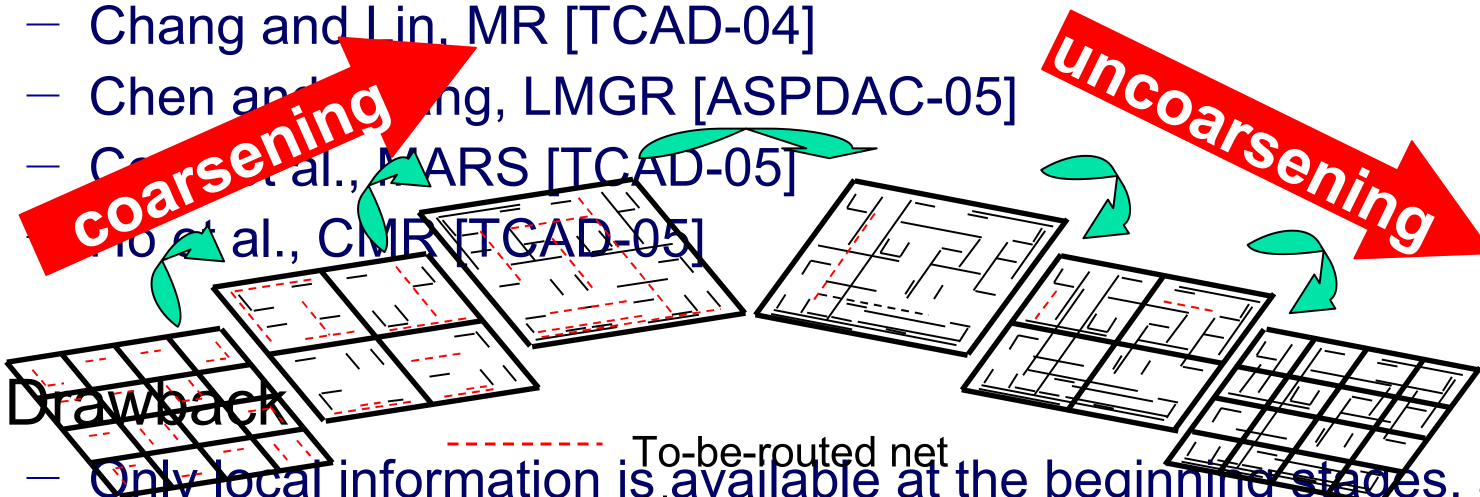


- Drawback
  - Might lack the global information for the interaction between subregions

Multilevel Routing

- Traditional Λ-shaped multilevel routing
  - Bottom-up coarsening + top-down uncoarsening
  - Often called the “V-cycle” framework in the literature
  - Name it the Λ-shaped framework as it works bottom-up and then top-down

- Academic routings:
  - Chang and Lin, MR [TCAD-04]
  - Chen and Chang, LMGR [ASPDAC-05]
  - Cong et al., MARS [TCAD-05]
  - Ho et al., CMR [TCAD-05]

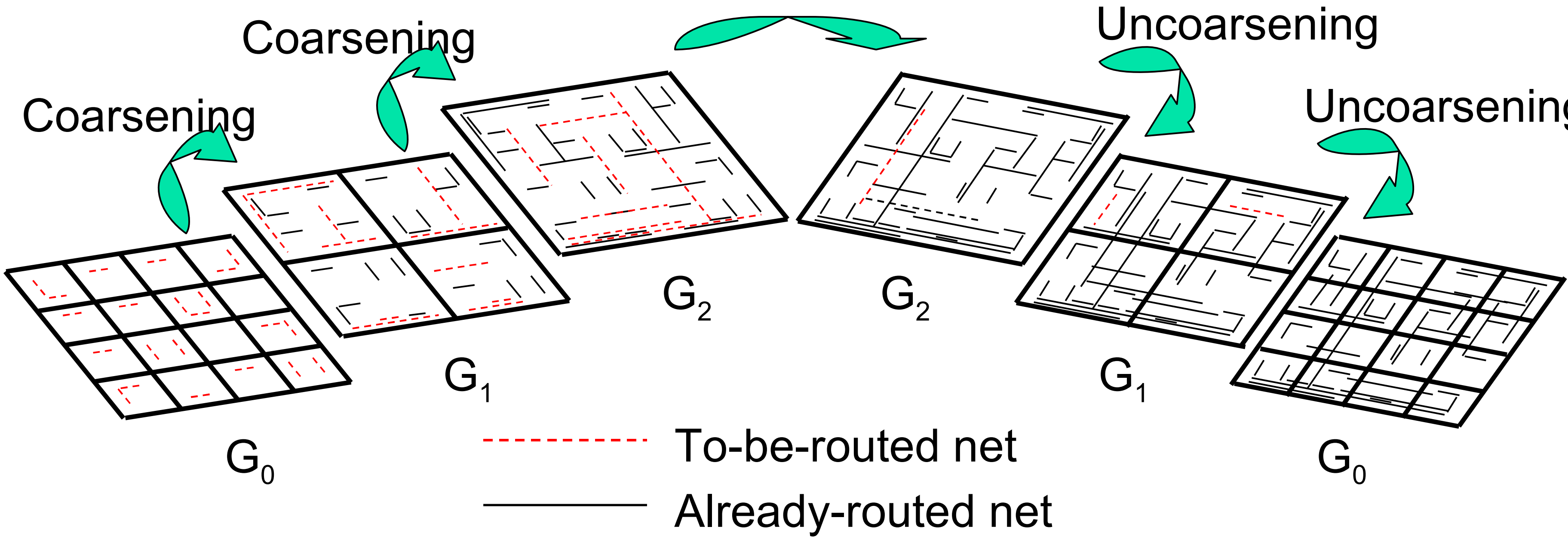


- Drawback
  - Only local information is available at the beginning stages, and thus cannot handle global circuit effects well

Λ-Shaped Multilevel Routing: LMGR

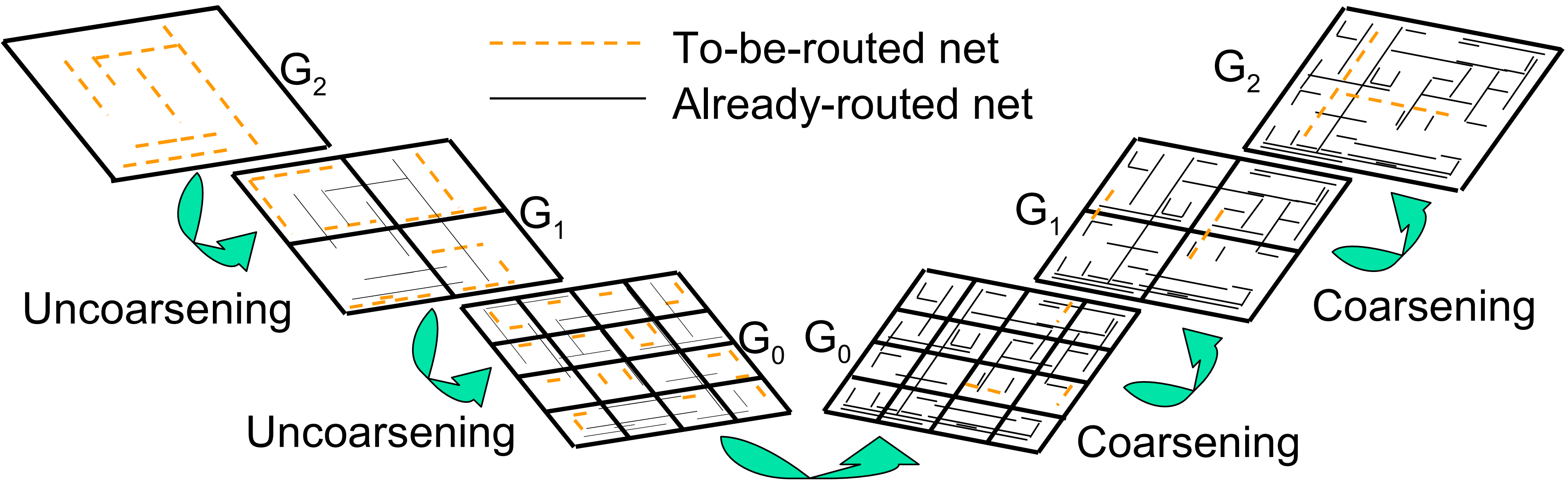
Perform global pattern routing and Dijkstra's shortest path detailed routing for local connections and then estimate routing resource for the next level.

Use global maze routing and Dijkstra's shortest path detailed routing to reroute failed connections and refine the solution.



Does not have the view of the global configuration at the earlier stages.

Our New V-Shaped Multilevel Framework



Perform global pattern routing and Dijkstra's shortest path detailed routing for local nets and then estimate routing resource for the next level.

Use global maze routing and Dijkstra's shortest path detailed routing to reroute failed connections and refine the solution.

Consider the global effects at the earlier stages.

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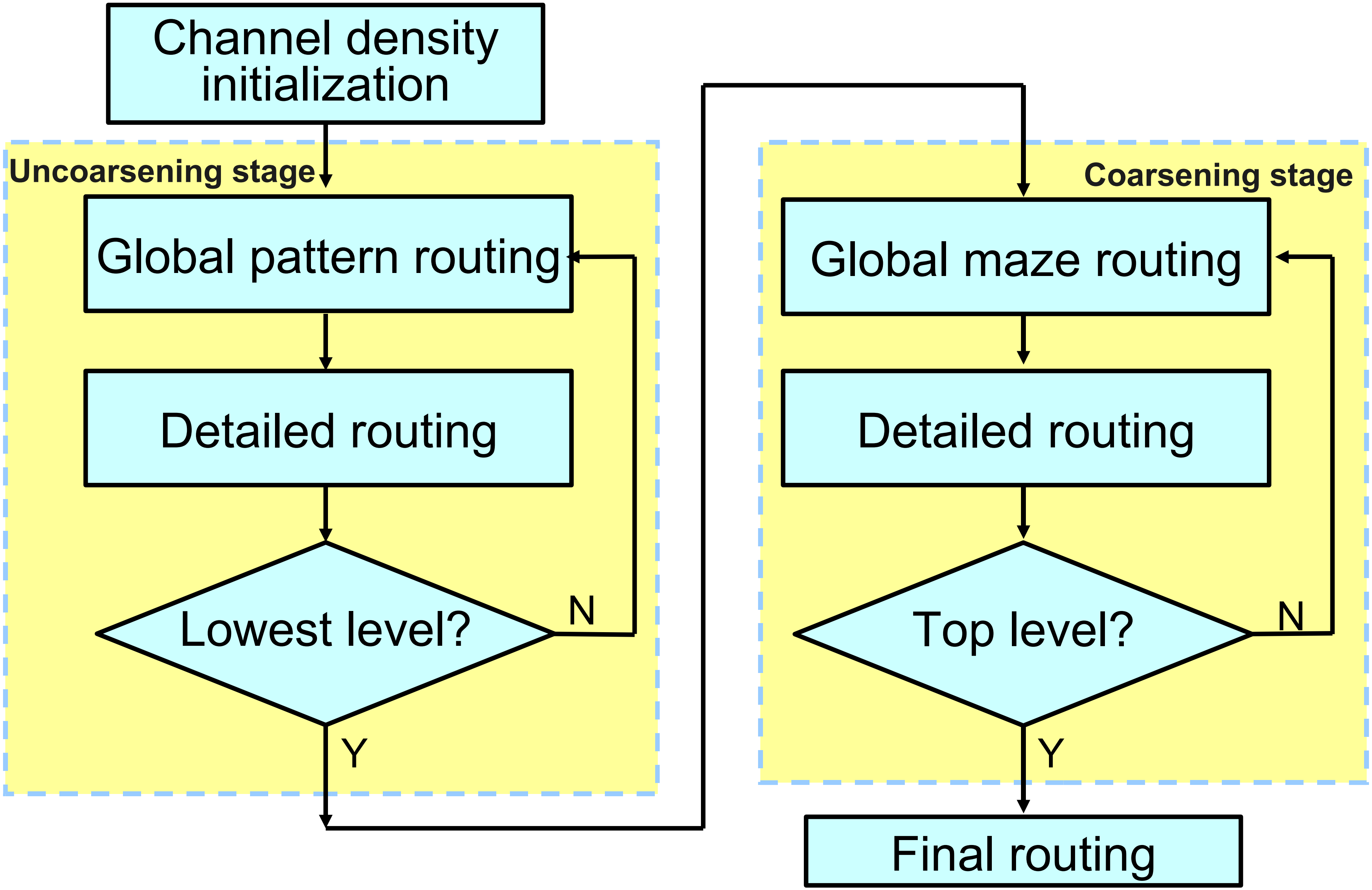
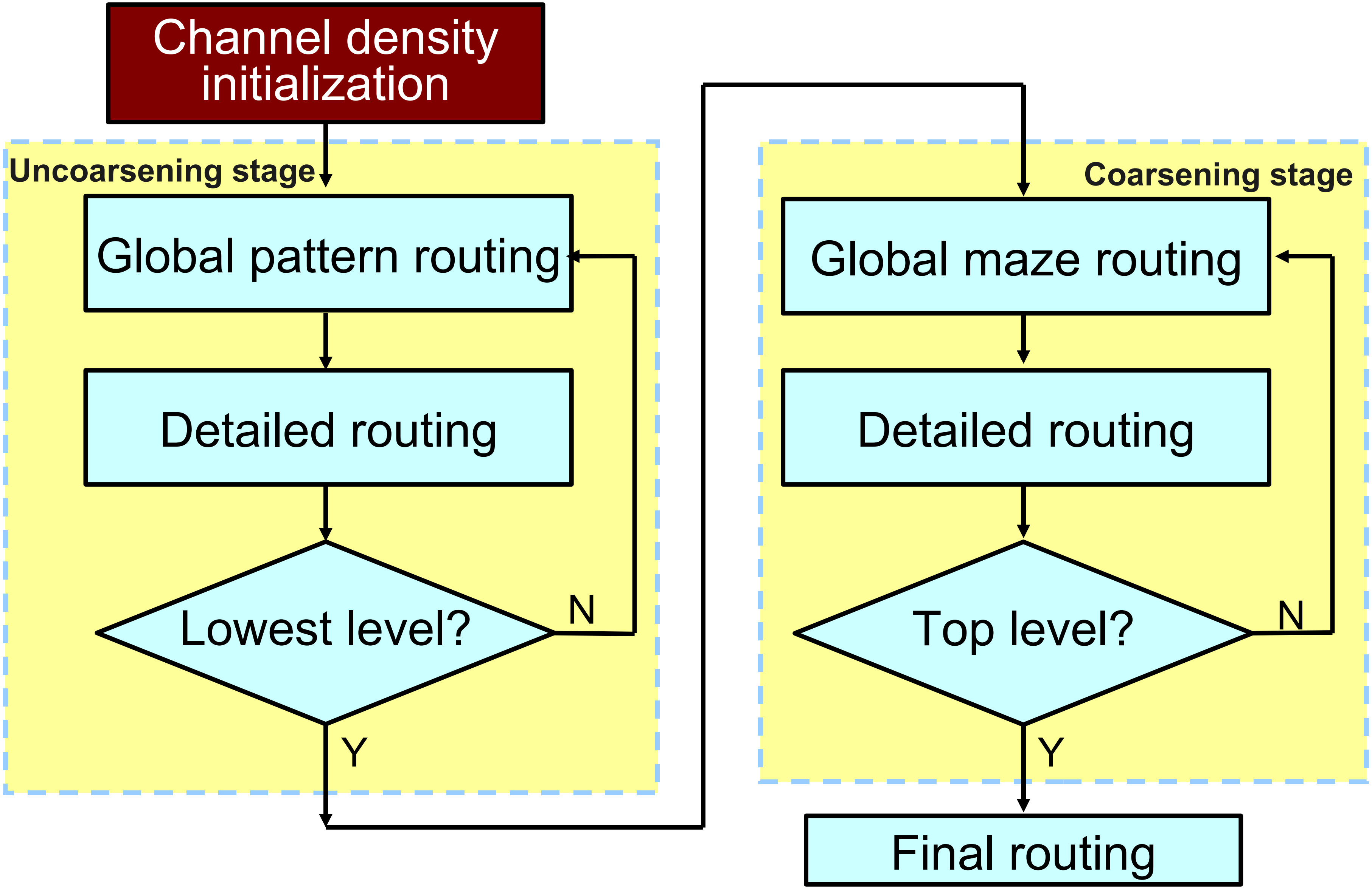
Design Flow



Channel density initialization
Uncoarsening stage
Global pattern routing
Detailed routing
Lowest level?
N
Y
Coarsening stage
Global maze routing
Detailed routing
Top level?
N
Y
Final routing

Design Flow



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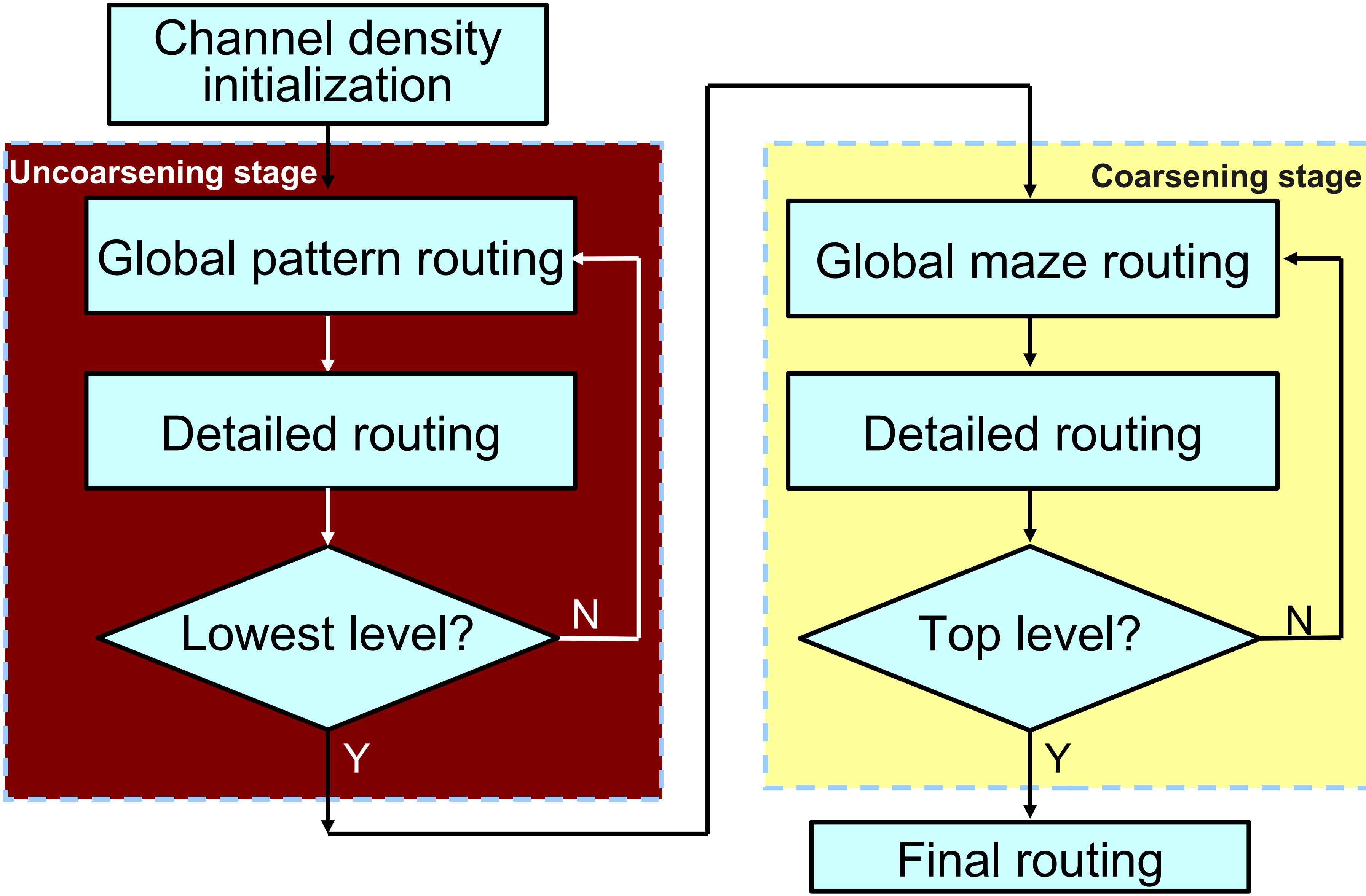
Channel Density Initialization and Updated

- Making the global routing, detailed routing, and resource estimation interact with each other can significantly improve routing completion rates
  - Only guide the latter nets passing through the area with lower congestion
  - Cannot avoid determining the bad global path of an early routed net without considering the routing resource of succeeding nets.
- Initialize the congestion map based on the pin distribution and the global-path prediction of all nets
- Update the congestion map dynamically based on both the already routed nets and the estimated unrouted nets
- Have better congestion control throughout the whole routing process

Design Flow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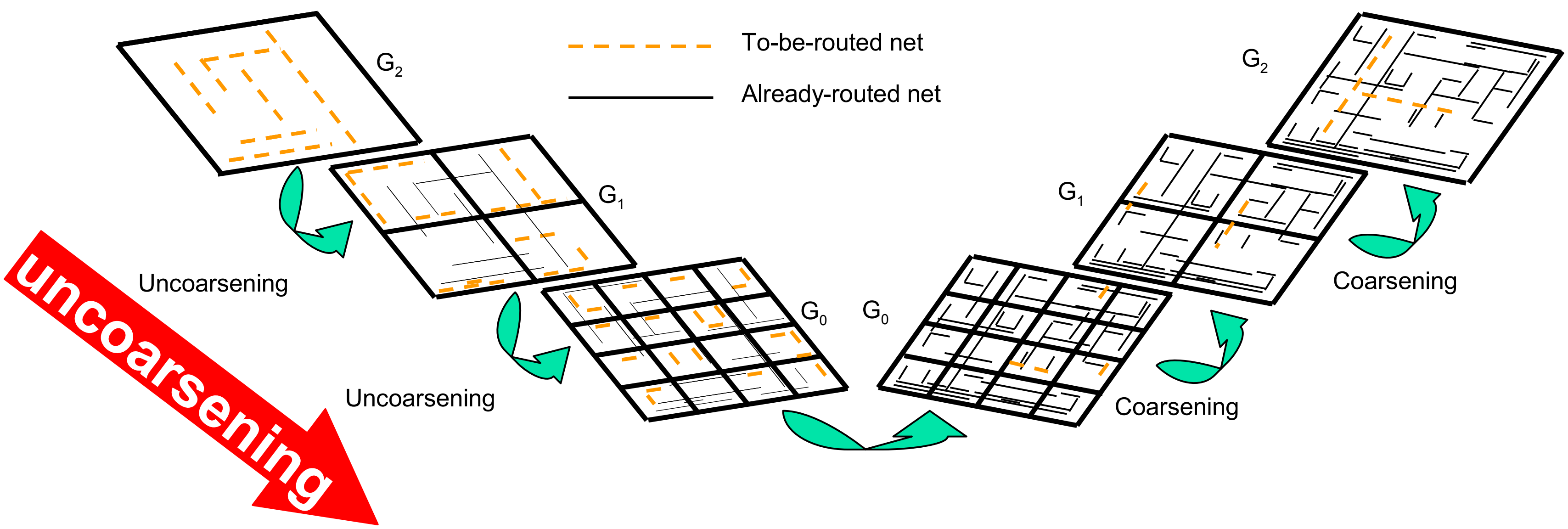
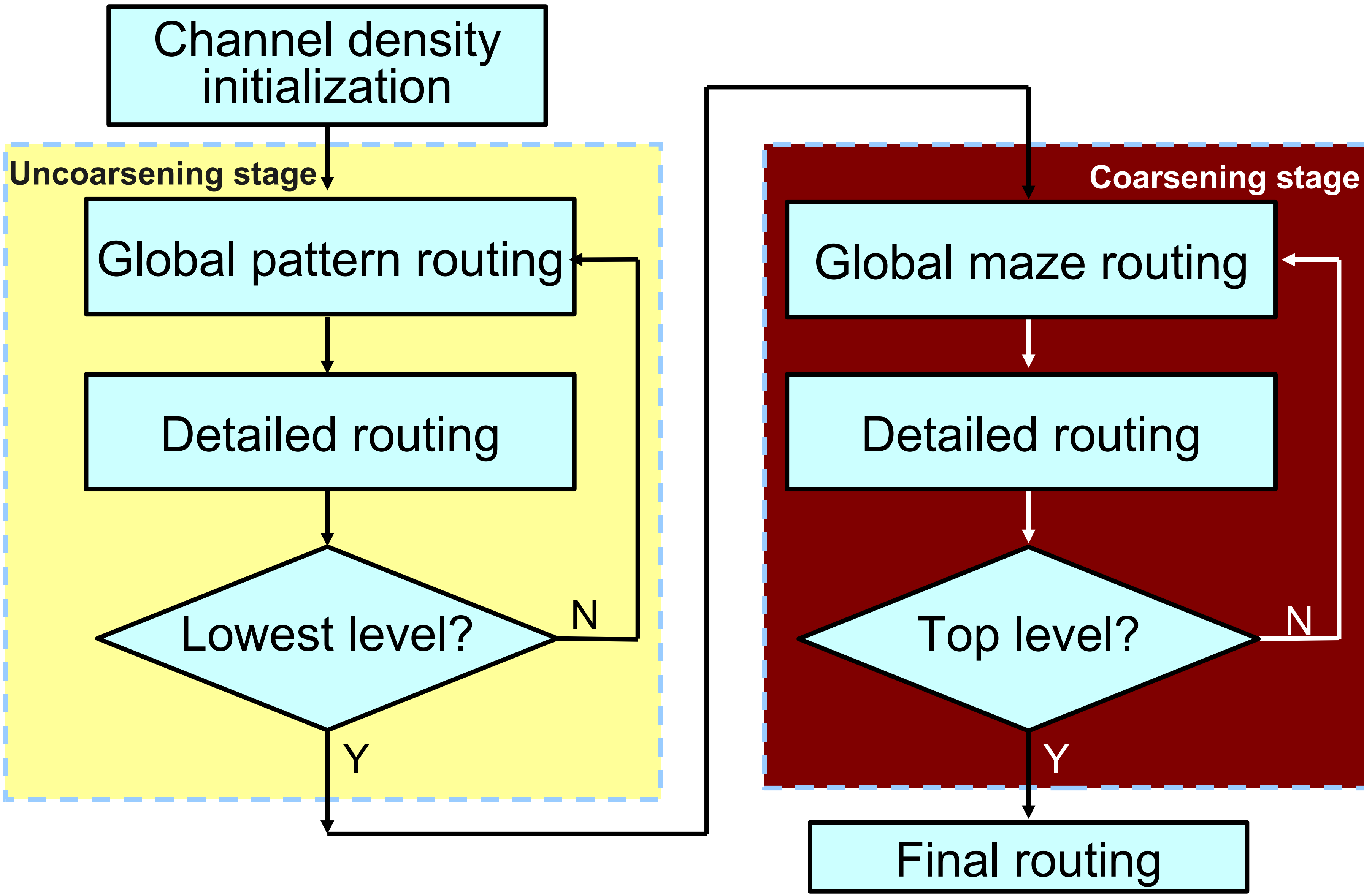
Uncoarsening Stage

- Global effect is the highest consideration in this stage
  - Longer nets are more critical
- Start from the coarsest tiles of level k; route level nets at each level



Design Flow



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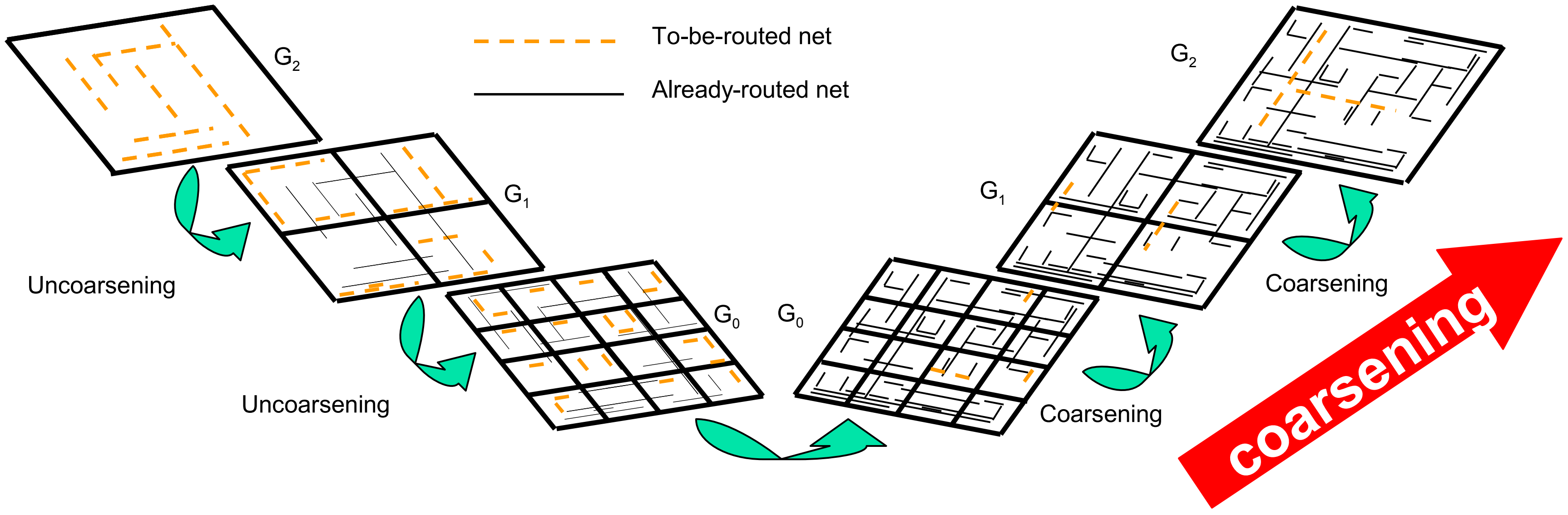
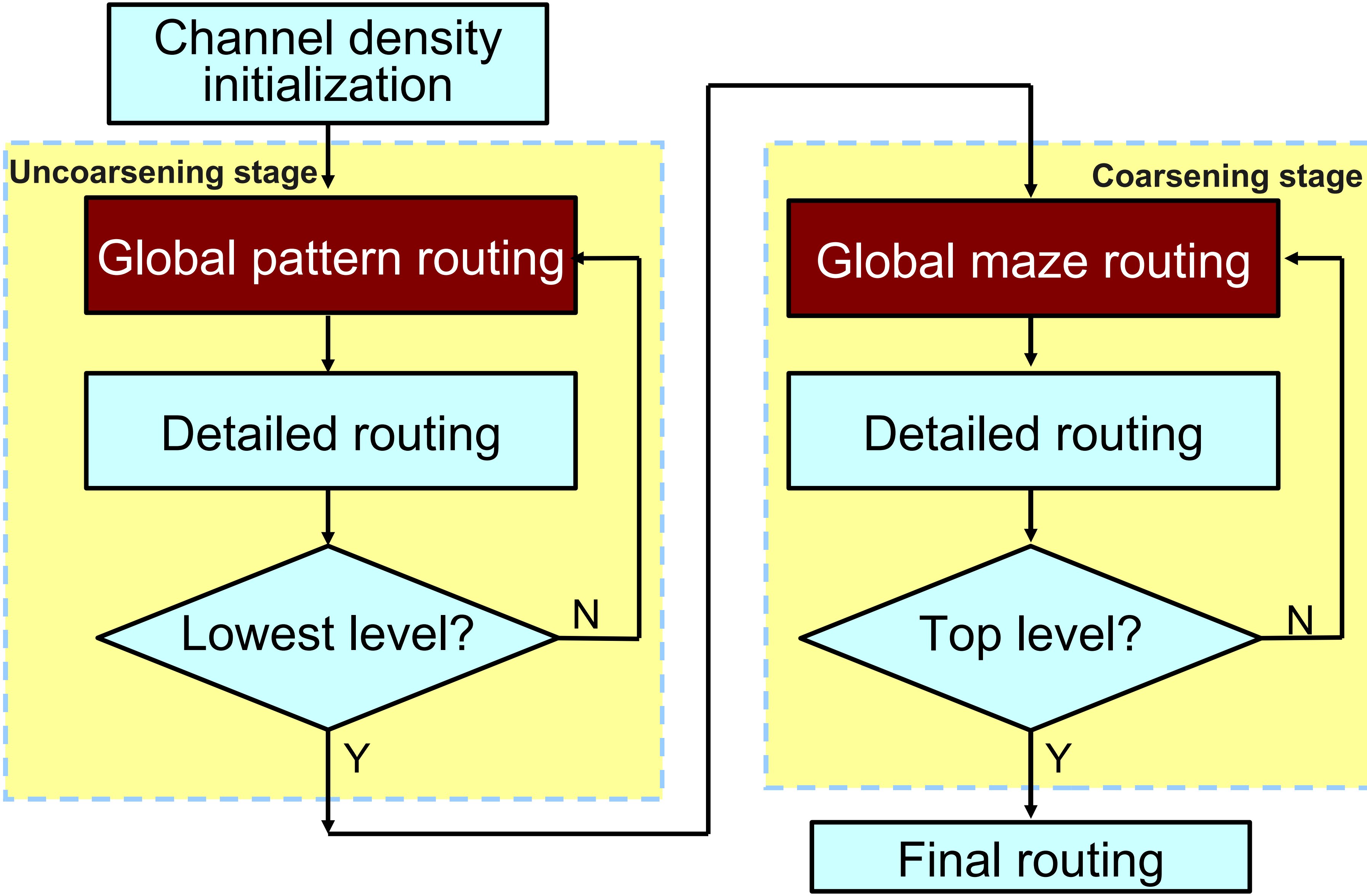
Coarsening Stage

- Routability is the highest consideration in this stage
  - Shorter connections are more critical
- Repeat the same steps as the uncoarsening stage
  - Perform maze routing at the global routing stage



Design Flow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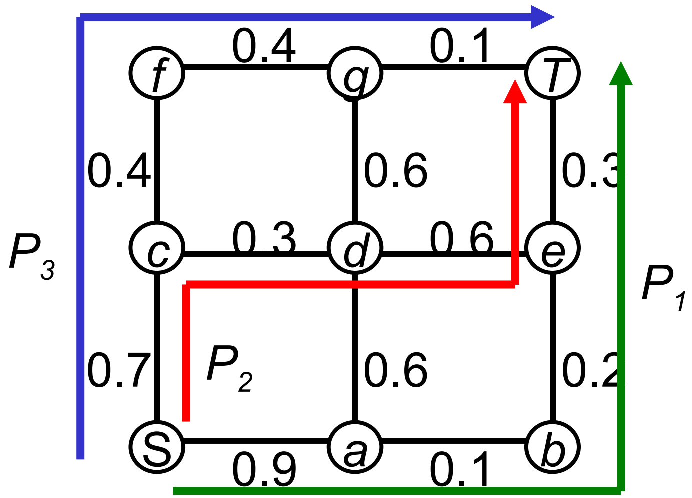
Cost Function for Global Routing

- The cost function is the sum of the maximum channel congestion and the average of the total path congestion
  - Can avoid selecting a path with lower total path congestion and higher channel congestion path
  - Can avoid selecting a path with higher overall path congestion when two path have the same maximum channel congestion

$$\alpha(R_e) = \max_{e \in R_e} c_e + \frac{1}{|R_e|} \sum_{e \in R_e} c_e$$

c_e: the congestion of edge e

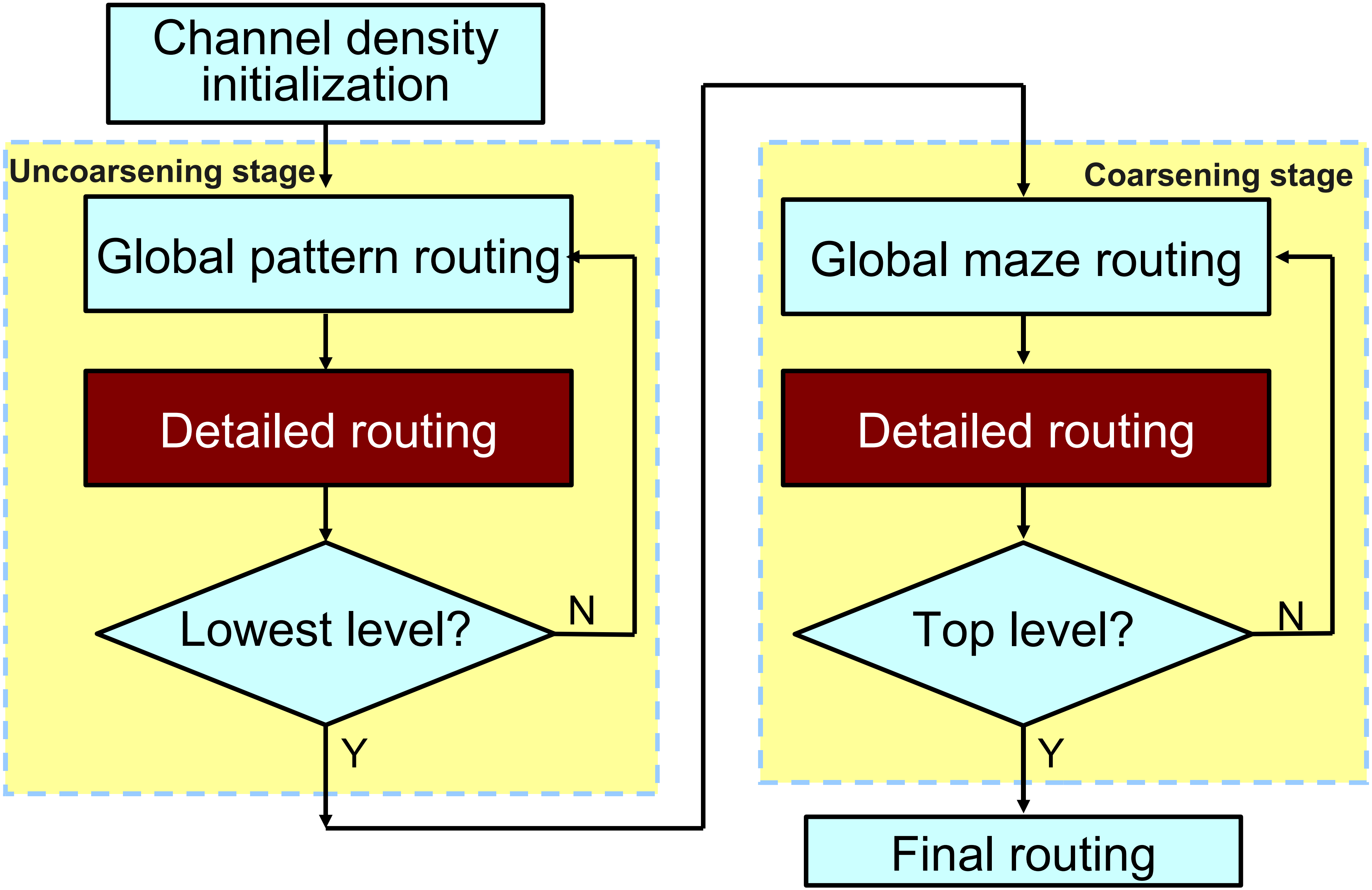


P1 has the minimal total path congestion

P2 and P3 have the same maximum channel congestion

P3 has the minimum cost

Design Flow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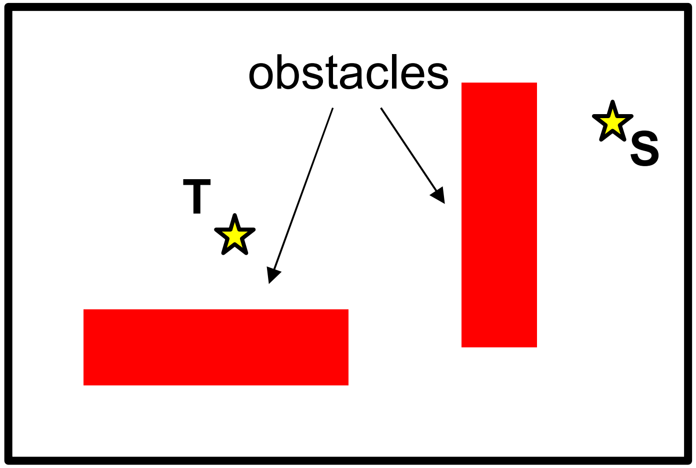
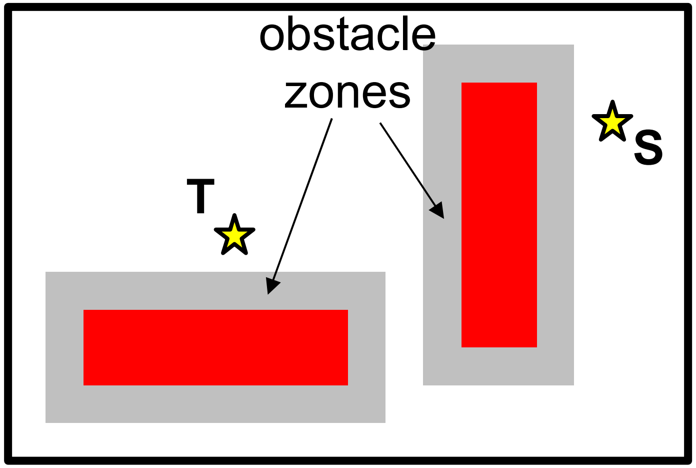
Triple-Line Graph (TLG) Model

- To find a design-rule-correct path and avoid redundant wires
- Construct the obstacle zones (gray areas) from the obstacles by taking design rules into account
  - expand the obstacle for a range which is the sum of the obstacle spacing and the half width of the routing wire
  - The area outside of the obstacle zones is available for placing the center lines of wires and mid-points of contacts



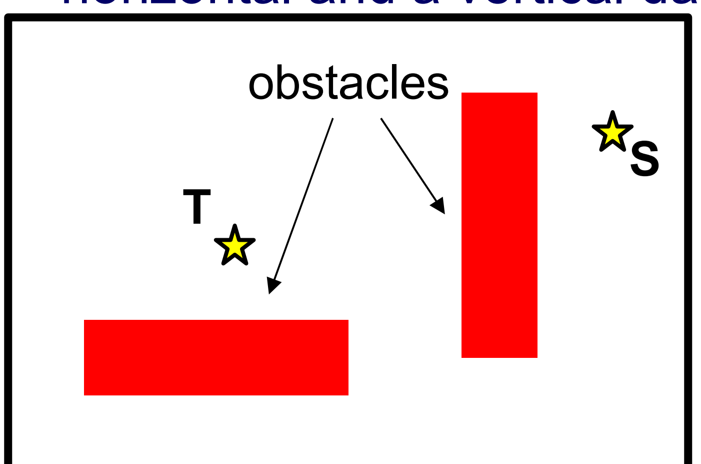
a routing example



obstacle zones construction

TLG Model (Cont'd)

- Collect all x-coordinates and y-coordinates of
  - the source and the target
  - the boundaries of all obstacle zones
  - the centers of all obstacle zones (P-lines and C-lines)
- Generate a vertical (horizontal) dashed line for each x-coordinate (y-coordinate)
- Construct a connection graph
  - a node in the connection graph denotes an intersection of a horizontal and a vertical dashed lines



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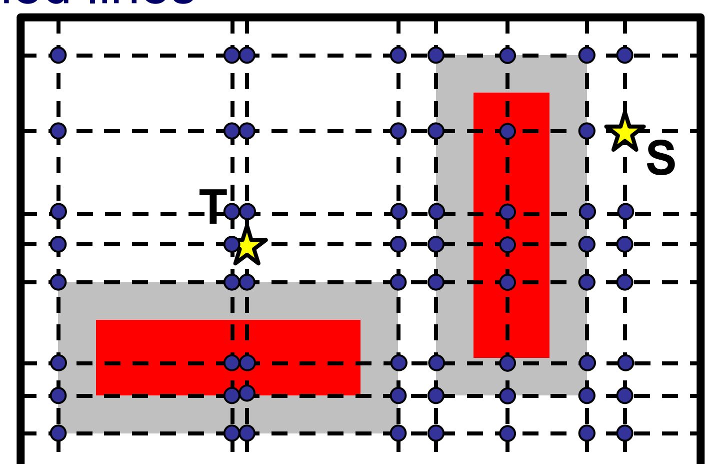
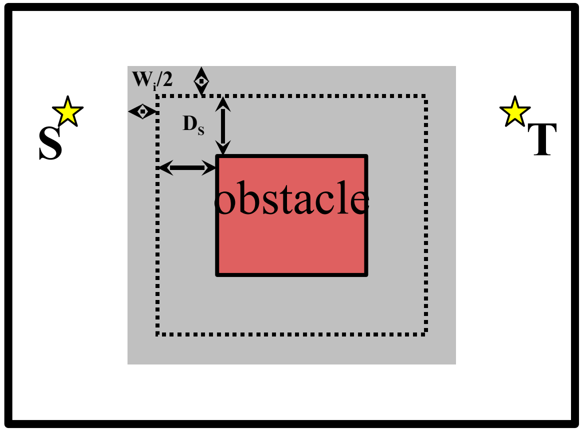


a connection graph

P-Lines

- To avoid design-rule-incorrect paths
  - pass the center of the obstacle zone
  - Is perpendicular to the routing direction of the obstacle zone



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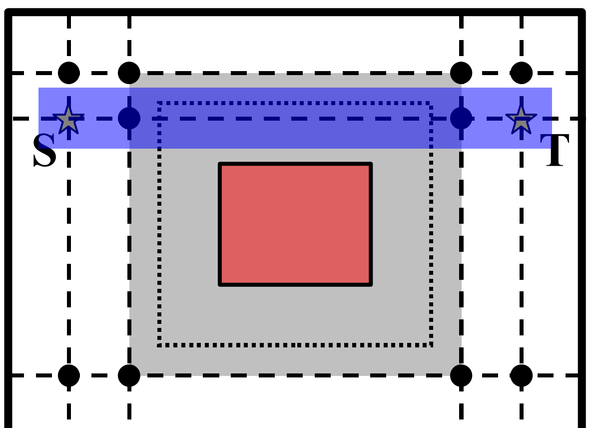
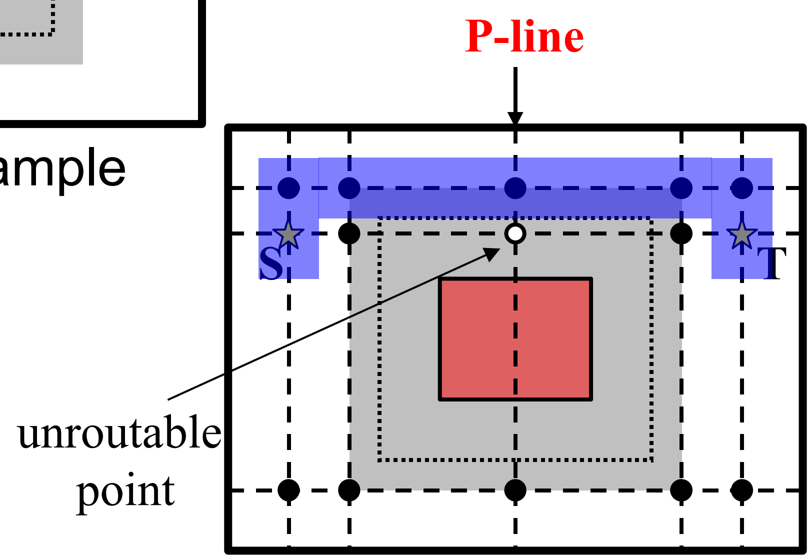


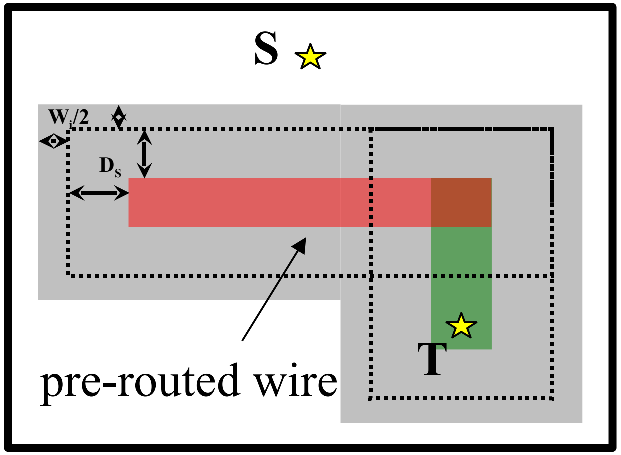
A design-rule-incorrect path



A design-rule-correct path

C-Lines

- To avoid redundant wires
  - pass the center of the obstacle zone
  - Is parallel to the routing direction of the obstacle zone



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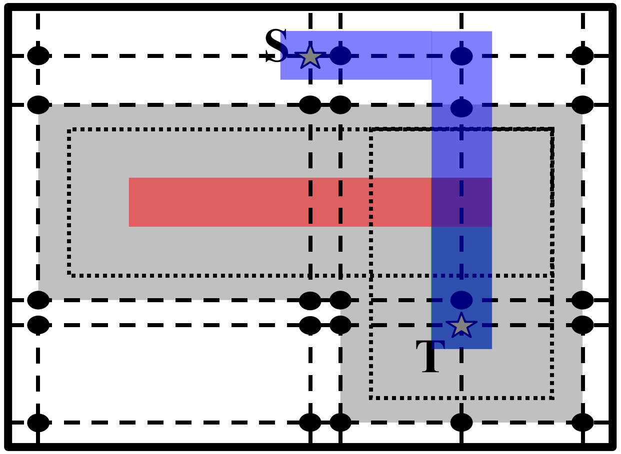
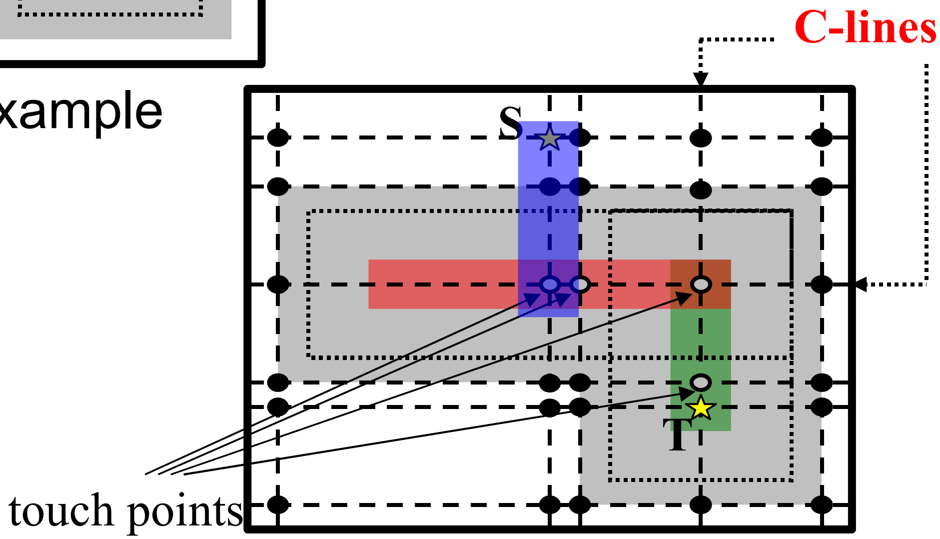
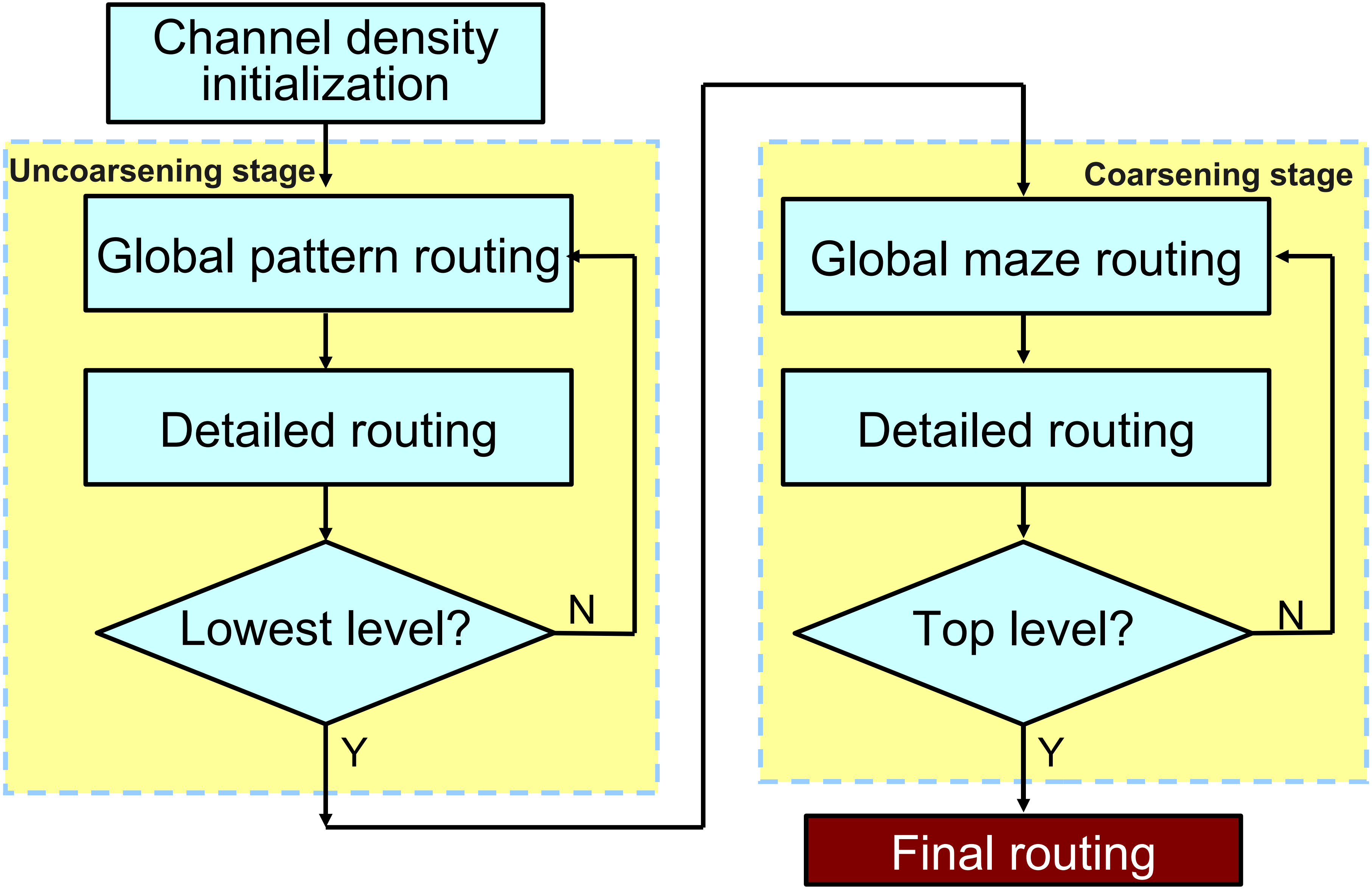


A path with an redundant wire



A path without redundant wires

Design Flow



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Experimental Settings

- Compare the following routings
  - MR [ICCAD-02, TCAD-04]
  - MARS [TCAD-05]
  - LMGR [ASPDAC-05]
  - VMGR [Ours]

- Delay computation: Elmore delay model

Multilevel Routing Comparison

Routing	Characteristics
MR	· **Λ-shaped** framework · local (coarsening) → global (uncoarsening) · **Multilevel grid-based** global and detailed routing
MARS	· **Λ-shaped** framework · local (coarsening) → global (uncoarsening) · **Multilevel gridless** global routing + **flat girdless** detailed routing
LMGR	· **Λ-shaped** framework · local (coarsening) → global (uncoarsening) · **Multilevel gridless** global and detailed routing
Ours (VMGR)	· **V-shaped** framework · global (uncoarsening) → local (coarsening) · **Multilevel gridless** global and detailed routing

1. Multilevel Routing with Uniform Nets

- Benchmarks:
  - All wire size and spacing are uniform

Circuit	Size (um^2)	#Layers	#Nets	#Pins
Mcc1	45000x39000	4	1693	3101
Mcc2	152400x152400	4	7541	25024
Struct	4903x4904	3	3551	5471
Primary1	7522x4988	3	2037	2941
Primary2	10438x6488	3	8197	11226
S5378	435x239	3	3124	4818
S9234	404x225	3	2774	4260
S13207	660x365	3	6995	10776
S15850	705x389	3	8321	12793
S38417	1144x619	3	21035	32344
S38584	1295x672	3	28177	42931

Summary Results for Routing with Uniform Nets

	Total Wirelength	Critical Path Delay	Average Net Delay	Completion Rates	CPU Time
VMGR (Ours)	1.00	1.00	1.00	1.00	1.00
MR	1.10	44.00	5.67	1.00	5.79
MARS	--	--	--	1.00	1.97
LMGR	1.02	1.21	1.00	1.00	2.44

VMGR obtains less wirelength, smaller critical path delay, and smaller average net delay than all published grid-based and gridless routers.

2. Multilevel Routing with Non-Uniform Nets

- Modify the original circuits of uniform wire sizes by using the following rules:
  - the longest 10% nets are widened to twice of the original width, while the next 10% are widened to 150% of the original width.
  - proposed by Cong et al. [TCAD-05]

Circuit	Size (um^2)	#Layers	#Nets	#Pins
vd_Mcc1	45000x39000	4	1693	3101
vd_Mcc2	152400x152400	4	7541	25024
vd_Struct	4903x4904	3	3551	5471
vd_Primary1	7522x4988	3	2037	2941
vd_Primary2	10438x6488	3	8197	11226

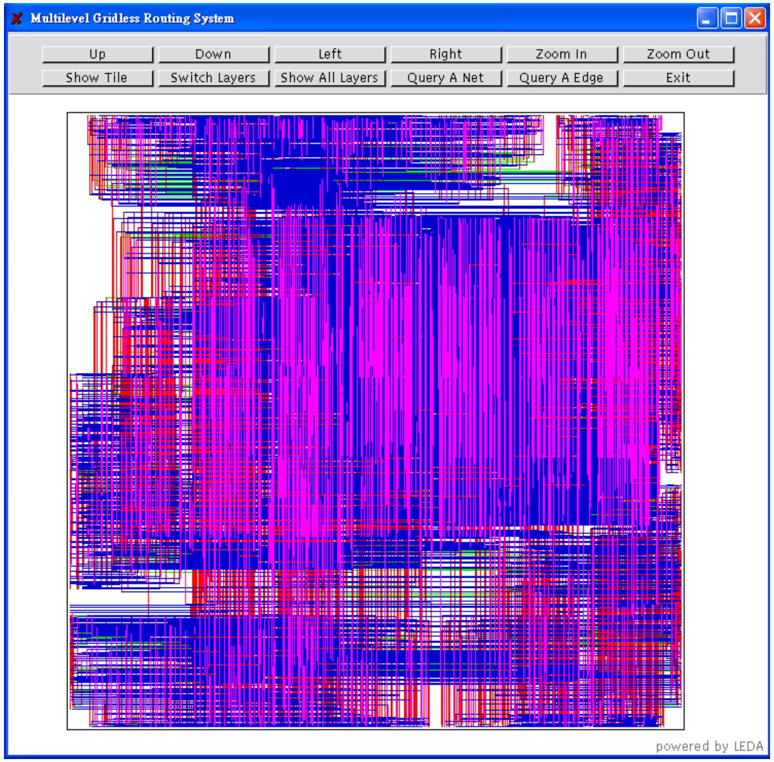
Summary Results for Routing with Non-Uniform Nets

	Total Wirelength	Has Failed Nets	Completion Rates	CPU Time
VMGR (Ours)	1.00	No	**1.00**	1.00
MARS	--	Yes	**0.99**	1.19
LMGR	1.02	Yes	**0.99**	1.91

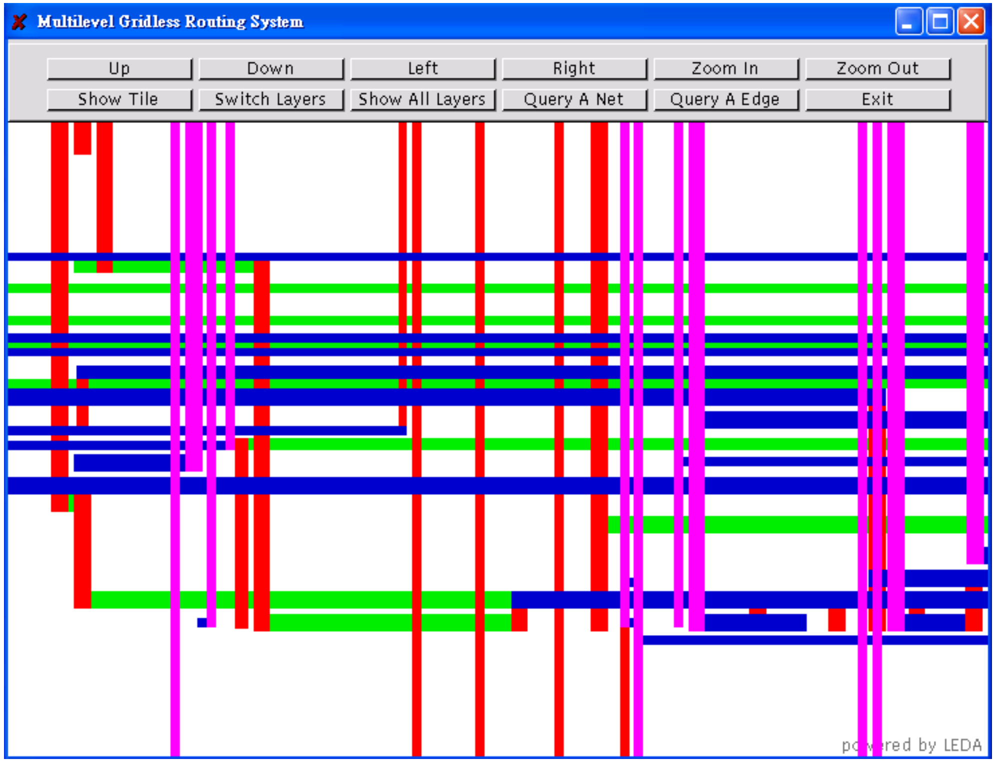
VMGR achieves the best routability among all published gridless routers.

Routing Layouts for Non-Uniform Nets

- Circuit: vd_Mcc2



The full-chip routing solution



A partial routing solution

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Conclusion

- We proposed a new V-shaped multilevel routing framework.
- Experimental results have shown that our V-shaped multilevel gridless router can obtain 100% routing completion rates with less wirelength, smaller critical path delay, and smaller average net delay than all published routers.
- Besides, it can handle designs with non-uniform wire widths well and obtained better routing solutions than all published routers.

Thank you

for Your Attention!