FCSCAN: An Efficient Multiscan-based Test Compression Technique for Test Cost Reduction

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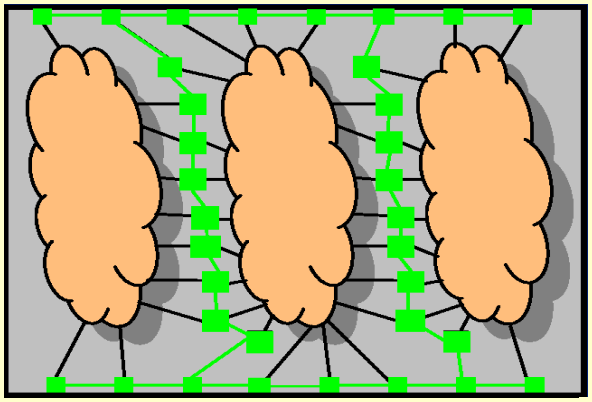
Outline

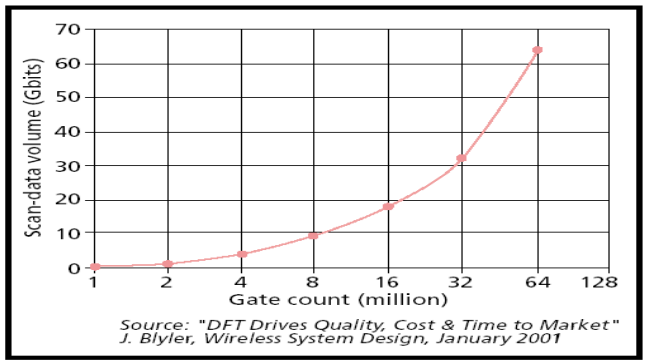
- Introduction
- FCSCAN Architecture
- Compression Analysis
- Improved FCSCAN
- Experimental Results
- Conclusions

Scan Test

- Scan-based Testing
  - Increases Controllability and Observability
  - Bedrock of DFT techniques

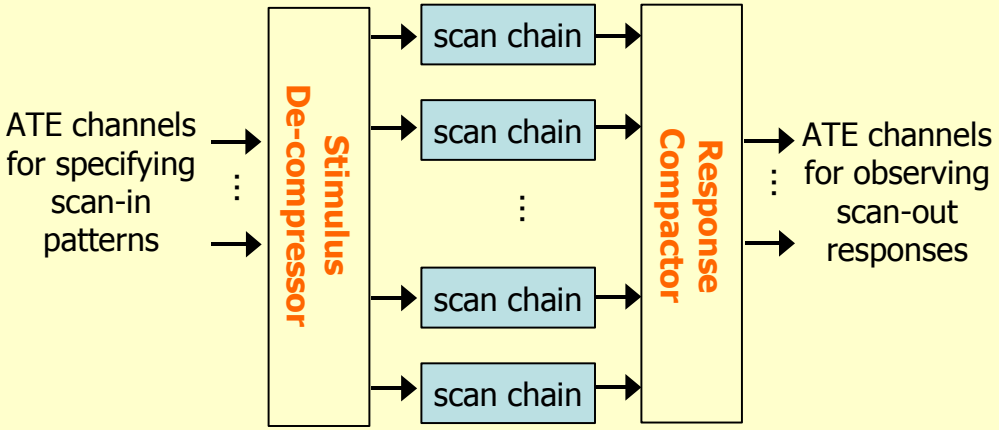


- Test Data Volume ↗
  - Increase test time and memory requirement ↗
  - Increase Test cost ↗↗



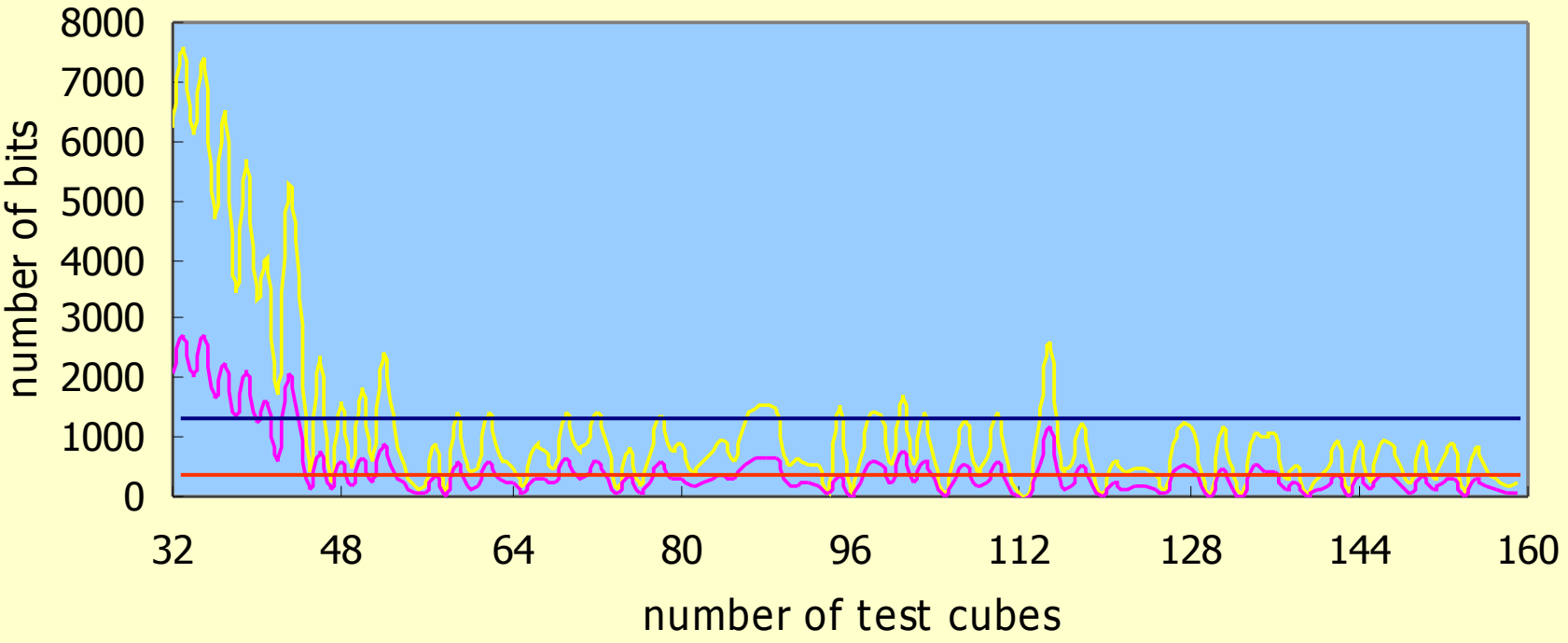
Test Data Compression

- Exploit low specified bit density
- Breaking long scan chains into short ones
- Use a smaller number of ATE channels to specify test stimulus and observe output responses

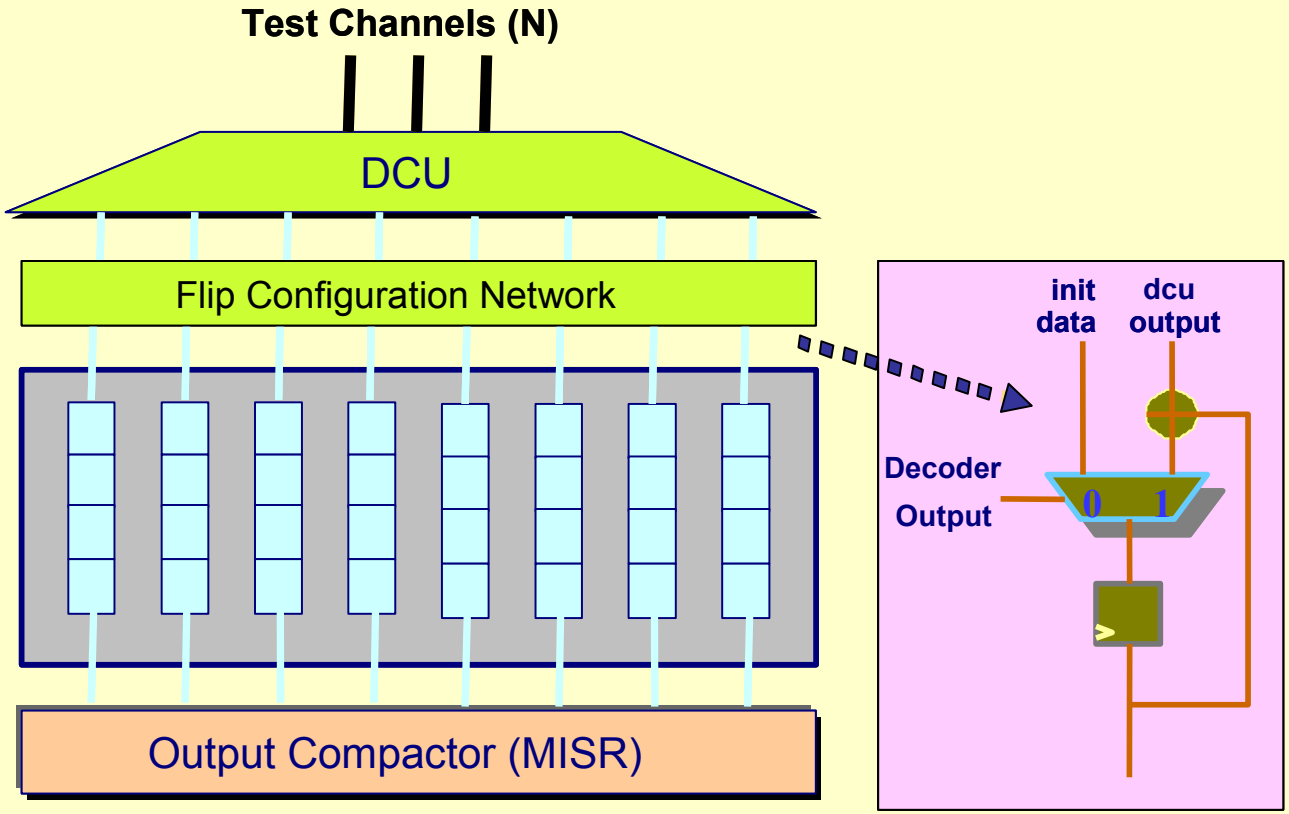


- Compression through Coding Schemes
  - Huffman Coding
  - Golomb Coding
  - Dictionary Coding
- Test Channel Reduction
  - Illinois Scan Architecture
  - Frugal Linear Network
  - CircularScan
- LFSR reseeding and combinational linear expansion

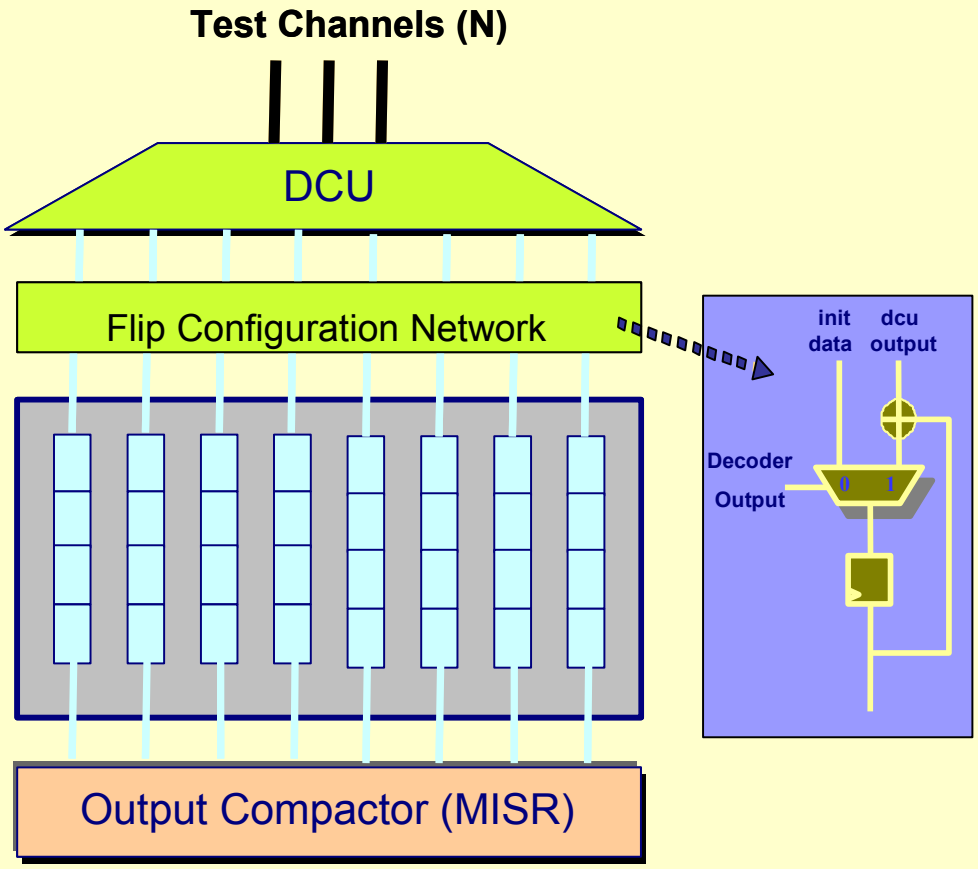
Test Cube Profile



FCSCAN Architecture



How Does It Work?



- **Broadcast Mode**
- **Configuration Mode**
  - Selected scan chain loaded through data input
  - Remaining scan chains sourced

- **Benefits**
  - Great compression
  - Regular test application

Compression Analysis

- Compressed Test Size

$$|T_E| = \sum_{i=1}^{N_v} \sum_{j=1}^{N_{sl}} M * (1 + n_{i,j})$$

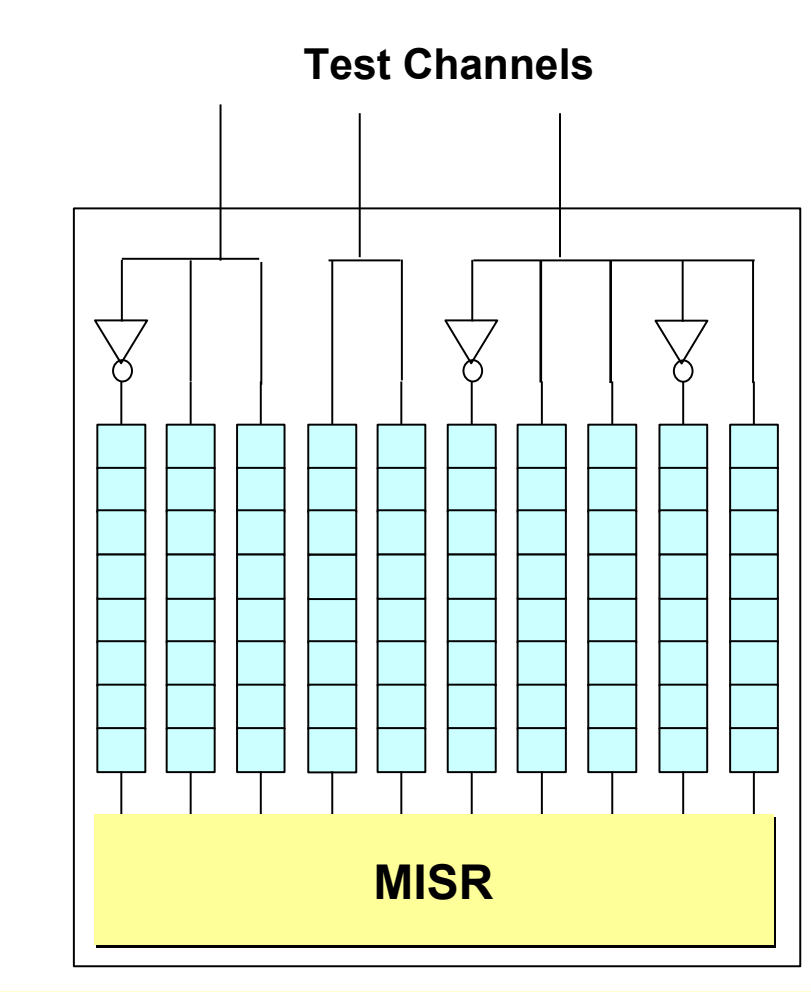
- Compression Ratio

$$\gamma = \sum_{i=1}^{N_v} \sum_{j=1}^{N_{sl}} \frac{M * (1 + n_{i,j})}{N_v * N_{sl} * N_{sc}} = \frac{M}{N_{sc}} + M * P_c$$

Compression Efficiency depends on two parameters: ***M*** and P_c

Minimizing Test Channels (*M*)

- Exploit the compatibilities among the internal scan chains
  - Compatible
  - Inverse Compatible
- Construct a fan-out decompression structure
- Benefits
  - Low hardware overhead
  - Capable of significant compression
  - Low Computation complexity $O(n^2)$



Reducing Coded Bits (P_c)

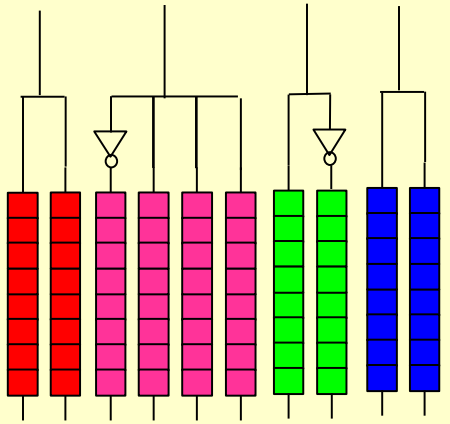
- Alter and reshape the space of scan inputs by inserting inverters

- Benefits
  - Low hardware overhead
  - Low computation complexity

Reducing Coded Bits (P_c)

C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
0	0	0	1	0	0	X	X	X	X
1	0	X	0	0	1	1	X	X	X
1	X	0	1	X	X	X	X	X	X
0	0	1	1	1	X	1	X	0	X
X	0	X	1	X	X	1	1	X	1
0	X	0	X	X	0	X	X	0	X
X	1	1	X	X	X	X	X	X	X
1	X	X	0	X	1	1	X	1	X

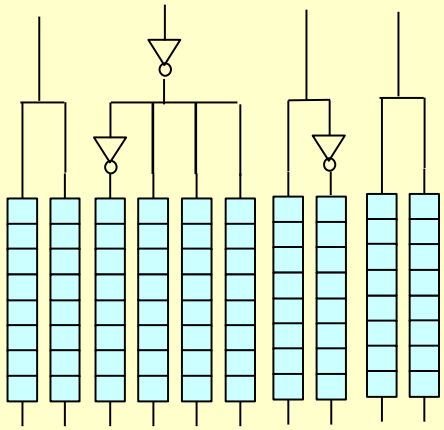
C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}
0	0	0	1	0	0	X	X	X	X
1	0	X	0	0	1	1	X	X	X
1	X	0	1	X	X	X	X	X	X
0	0	1	1	1	X	1	X	0	X
X	0	X	1	X	X	1	1	X	1
0	X	0	X	X	0	X	X	0	X
X	1	1	X	X	X	X	X	X	X
1	X	X	0	X	1	1	X	1	X



C_1	C_2	C_3	C_4
0	1	0	0
1	0	0	0
1	1	X	0
0	1	0	1
X	1	0	X
0	1	X	0
X	X	1	1
1	0	0	X

C_1	C_2	C_3	C_4
0	**1**	0	0
1	0	0	0
1	1	1	**0**
0	**1**	0	**1**
0	**1**	0	0
0	**1**	0	0
1	1	1	1
1	0	0	0

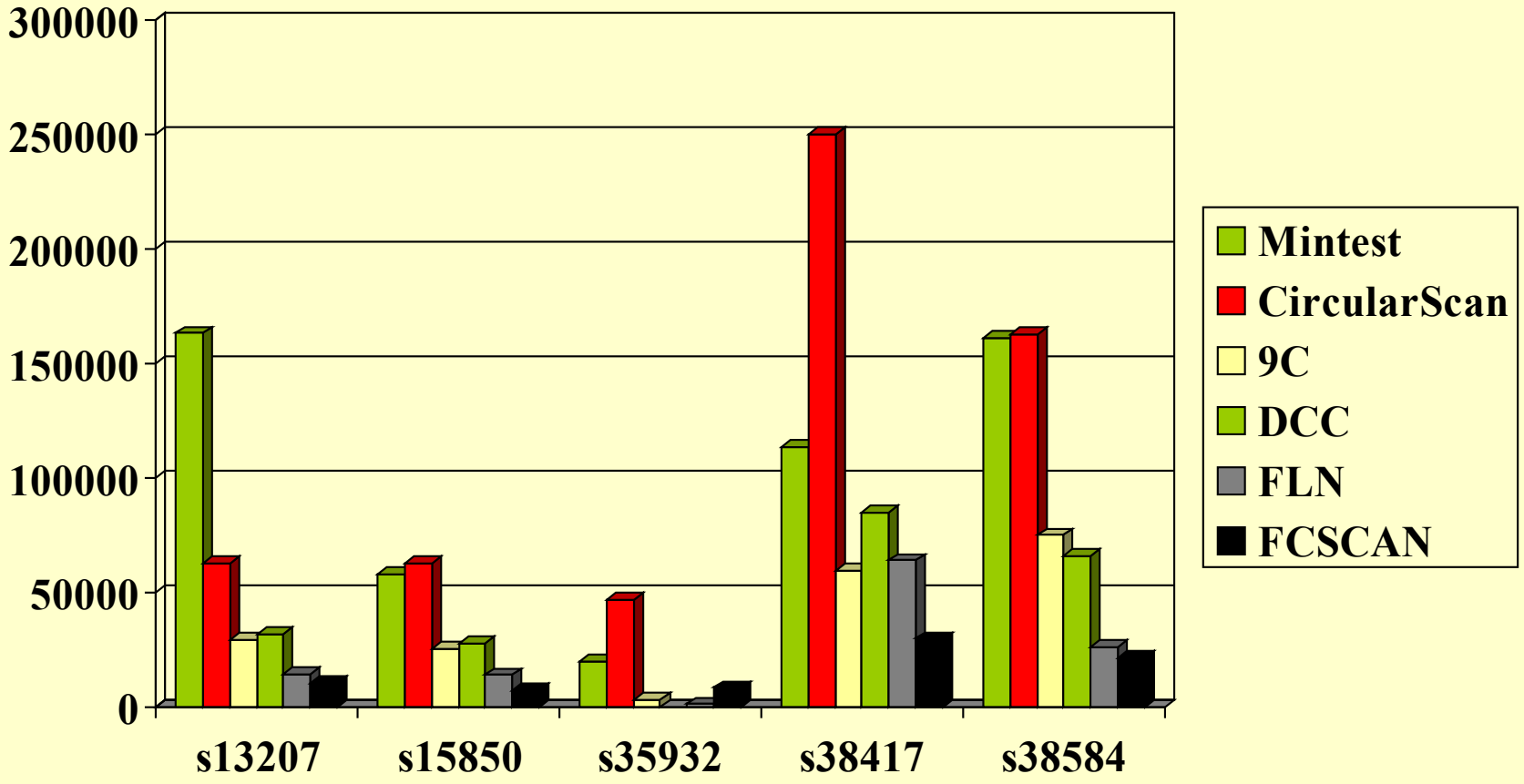
C_1	C_2'	C_3	C_4
0	0	0	0
1	**1**	0	0
1	0	0	0
0	0	0	**1**
0	0	0	0
0	0	0	0
1	1	1	1
1	1	**0**	1



Experimental Results

Circuits	FFs	N_V	T_D	P_S	N_{SC}	FCSCAN		Improved FCSCAN	
						M	T_E	M	T_E
s13207	700	251	175,700	4.36	50	6	30,564	6	29,520
					100	7	25,830	6	18,132
					200	8	26,304	5	10,290
s15850	611	148	90.428	12.40	50	6	24,024	6	20,766
					100	7	26,873	5	12,415
					200	8	30,056	4	7,072
s38417	1664	183	304,512	13.40	50	6	88,488	5	58,515
					100	7	92,120	6	53,382
					200	8	105,752	5	29,550
s38584	1464	288	421,632	6.01	50	6	84,726	5	53,740
					100	7	80,416	5	32,190
					200	8	85,896	4	21,020
ASIC1	8017	246	1,972,182	12	100	7	733,110	6	510,048
					200	8	806,448	6	391,842
					400	9	951,723	5	292,075

Comparison to Related Work



Conclusions

- A flexible DFT technique developed to reduce test cost
- Exploit the properties of ATPG-based test set
- Compression analysis
- Deterministically construct a linear decompression network for multiple scan architecture
  - Inverter/Interconnection based network structure exploring pair-wise linear relationship
  - Novel algorithm developed to construct network
  - Compaction taken into consideration during network construction
- Experimental data shows significant test data reduction by proposed scheme with low hardware overhead

Thank You!