A Memory Grouping Method for Sharing Memory BIST Logic

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Background

- Memory testing of SOC
  - Many different types of small-sized memories (the number of Memories > 1000)
  - To reduce test application time, we need BIST!
    - Memories can be tested in parallel
    - Test schedule under power constraint is needed
  - To reduce the area, we need BIST logic sharing!

Purpose

- To show a systematic way of memory BIST logic sharing under constraints
  - test application time
  - power
  - distance between memories

Outline

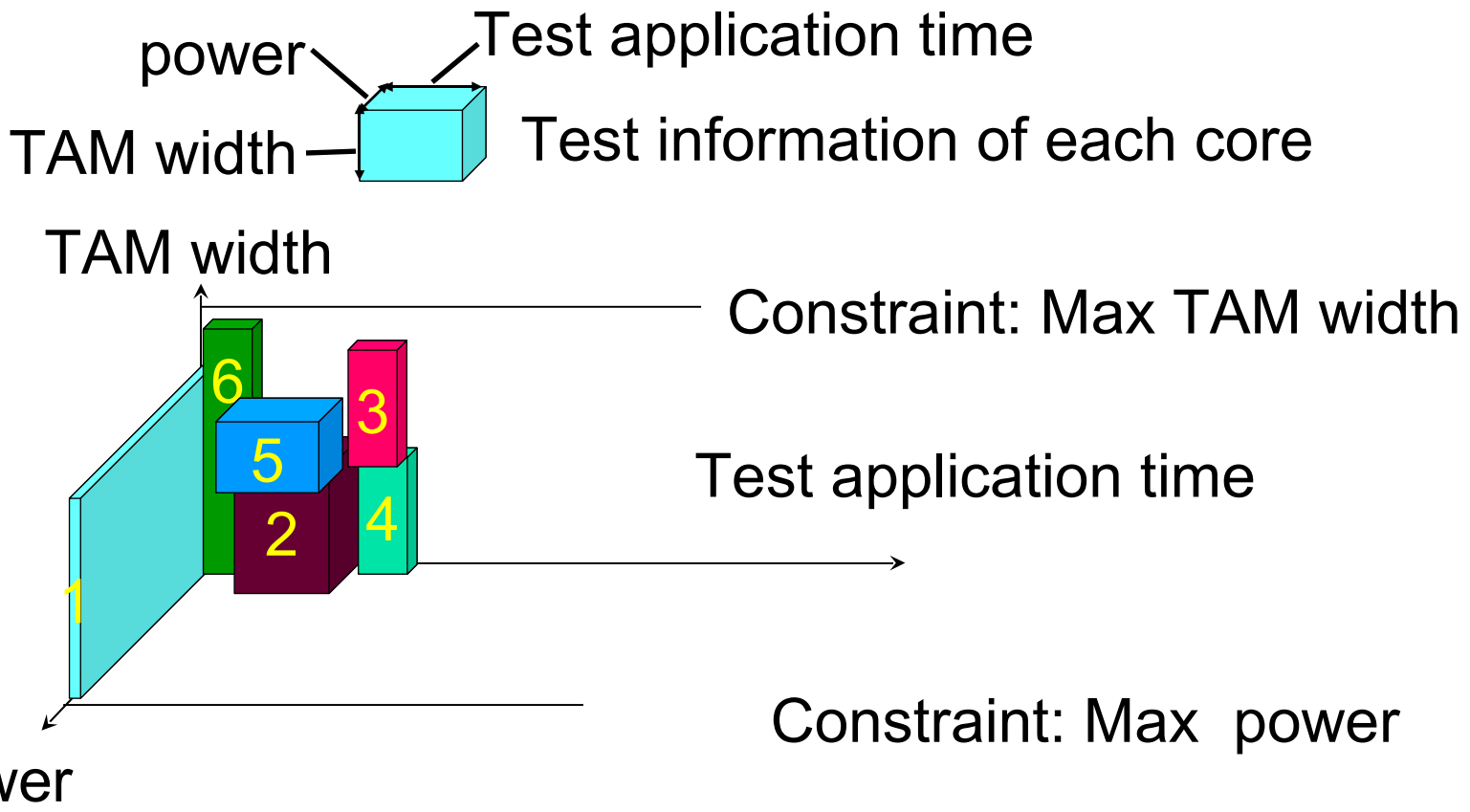
- Previous work
- Memory connection method
- Memory grouping problem formulation
- Memory grouping algorithm
- Experimental results
- Conclusion
- Future work

Previous work1: Test scheduling

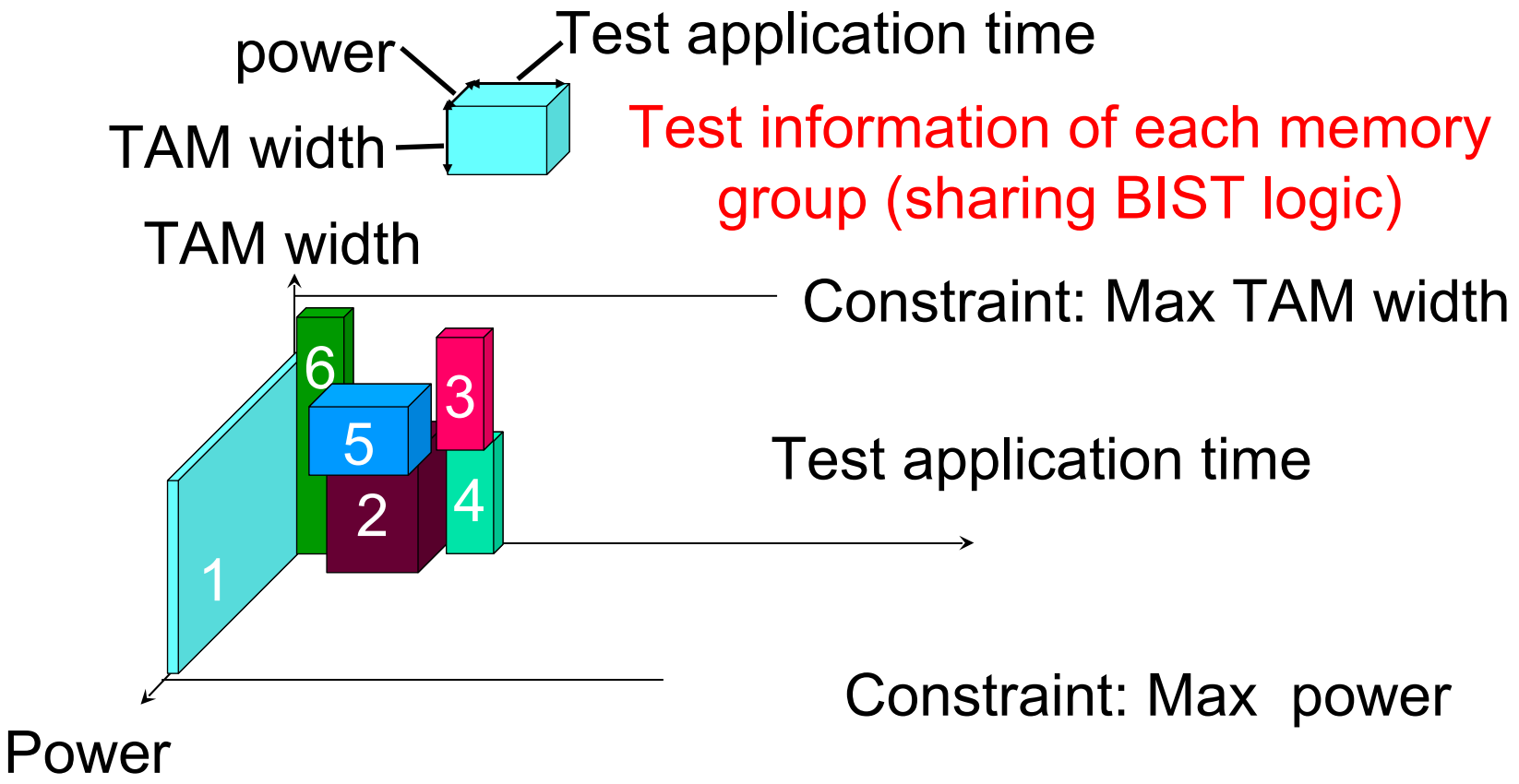
- Test scheduling under constraints:
  - Max TAM(Test Access Mechanism) width
  - Max power consumption
- Objective:
  - To minimize total test application time
- Rectangle packing method(ITC'02 : Huang et al)

Previous work1: Test scheduling

ITC'02 : Huang et al.

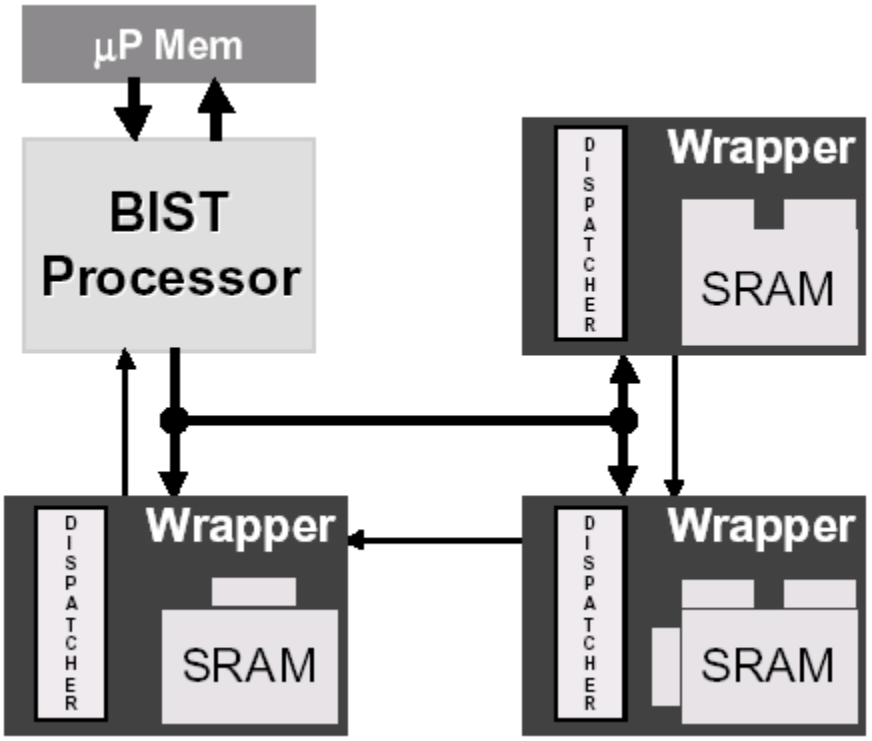


Previous work1: Test scheduling

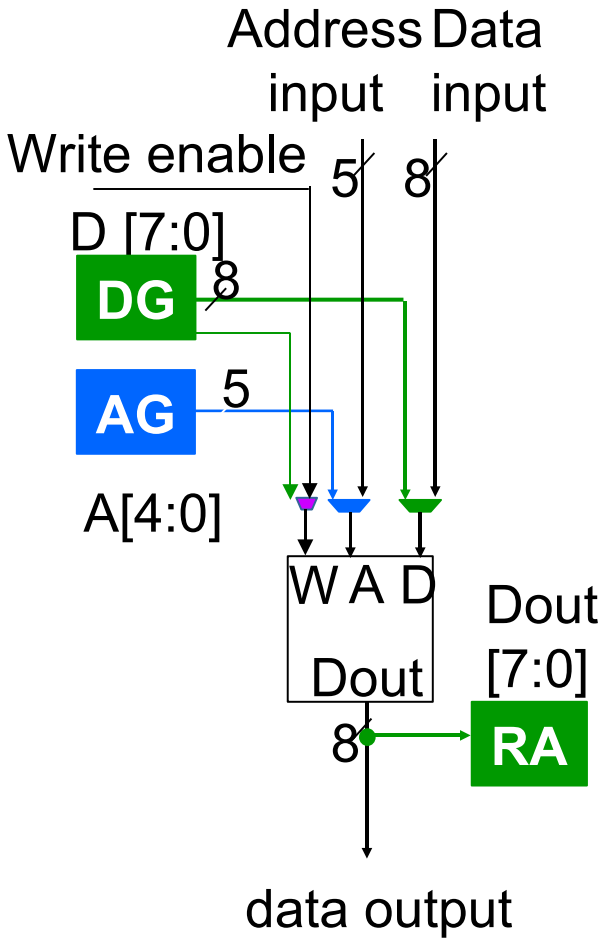


Previous work2: Memory BIST architecture

- Simplify Distributed SRAMs TEST (ITC'00:Benso et. al)
  - A BIST Processor
  - Memory wrappers
    (including BIST logic)
- Sharing a wrapper
  (same bit width, word depth



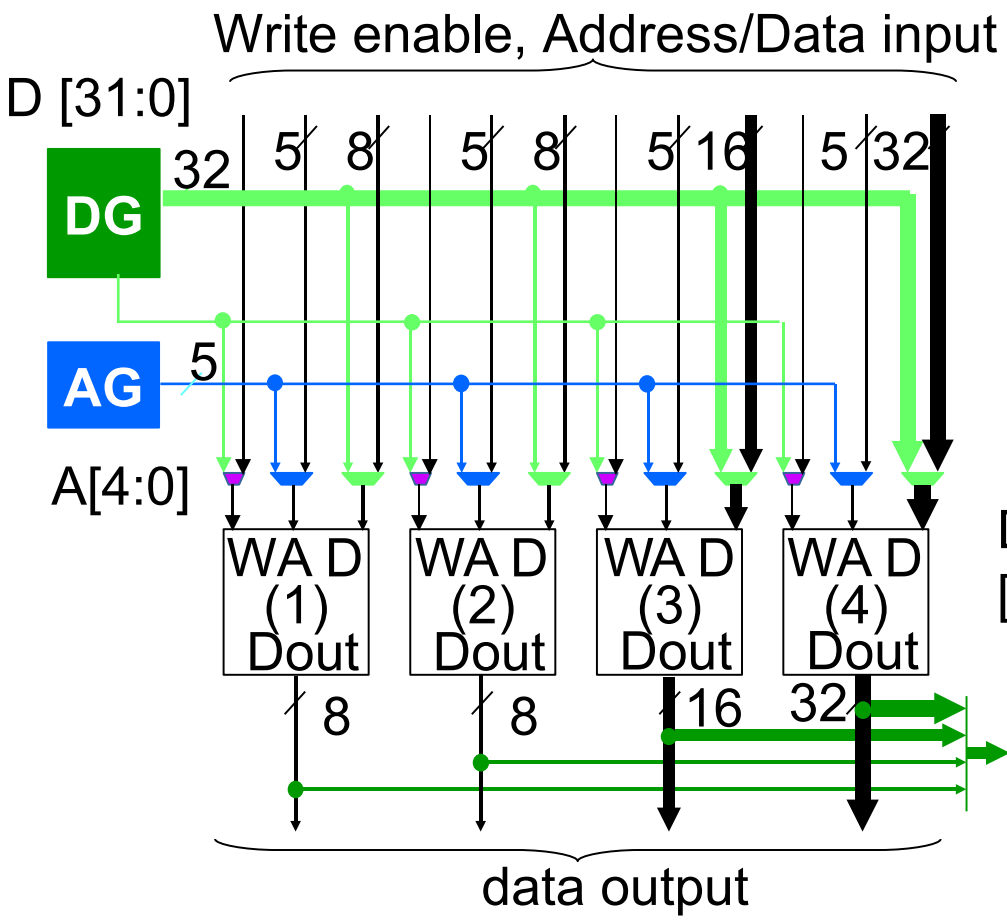
Memory BIST Logic components



8bit×32word Memory

8bit Data Generator(DG)
5bit Address Generator(AG)
8bit Response Analyzer(RA)

BIST Logic Sharing-Parallel connection



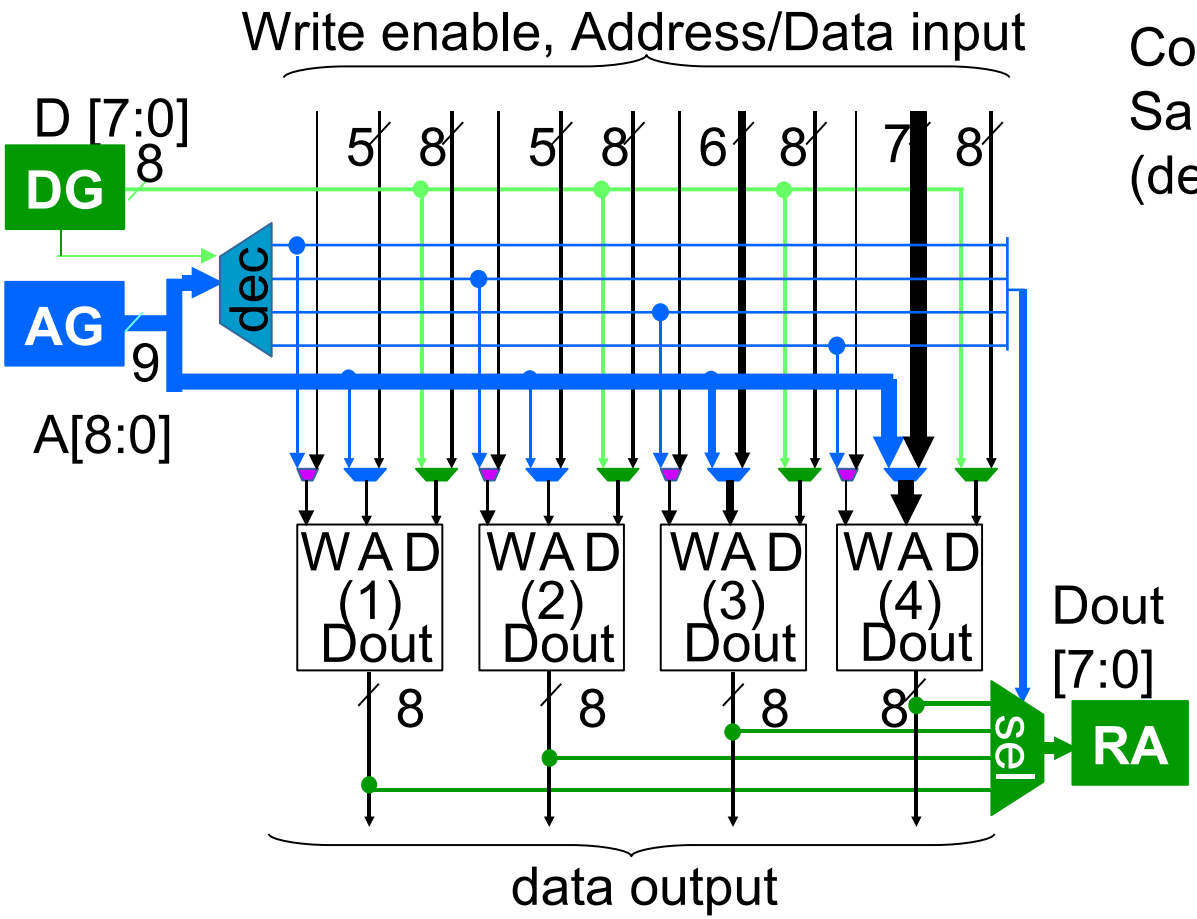
Condition:
Same address bit width

Without Sharing
DG:8+8+16+32 =64bit
AG:5×4 =20bit
RA:8+8+16+32 =64bit

Shared by
parallel connection
DG:32bit
AG: 5bit
RA:64bit

3DG,3AG are reduced!

BIST Logic Sharing-Serial connection



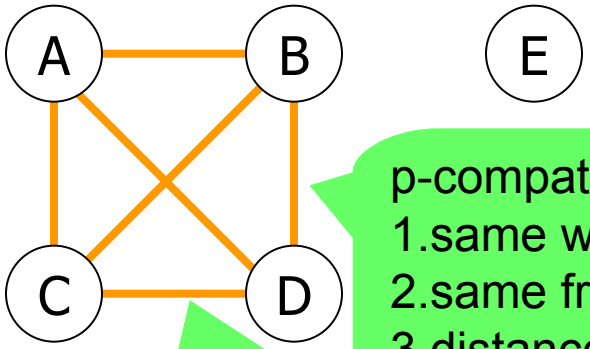
Condition：
Same data bit width
(depend on RA structure)

Without Sharing
DA:8×4=32bit
AG:5×4=20bit
RA:8×4=32bit

Shared by
Serial connection
DG:8bit
AG:9bit
RA:8bit

Compatibility graphs

p-compatibility graph

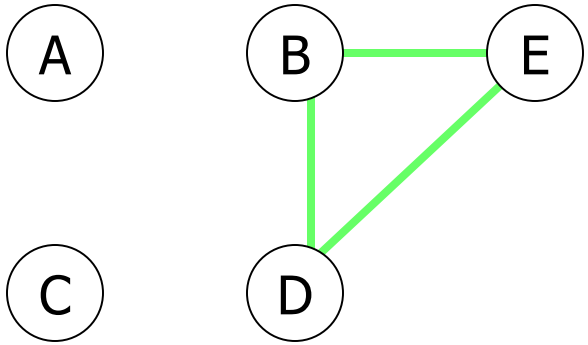


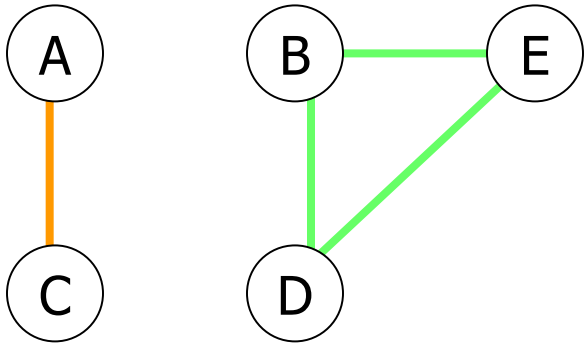
p-compatible
1.same word depth
2.same freq.
3.distance<const.

weight:
reduced bit
width by
connection

To [illegible] of
giv[illegible]
-all[illegible]
node [illegible] clique of
p-compatibility graph
or
s-compatibility graph

s-compatibility graph





Memory grouping problem formulation

Inputs:

A set of Memories and their information

data bit width,word depth,power,frequency,location

Outputs:

(1) A partition of given memories such that;
-all the blocks are node set of the clique of
p-compatibility graph or *s-compatibility graph*

(2) Connection type of each block (*p* or *s*)

(3) Test schedule

Memory grouping problem formulation

Constraints:

(1) Maximum allowed power consumption

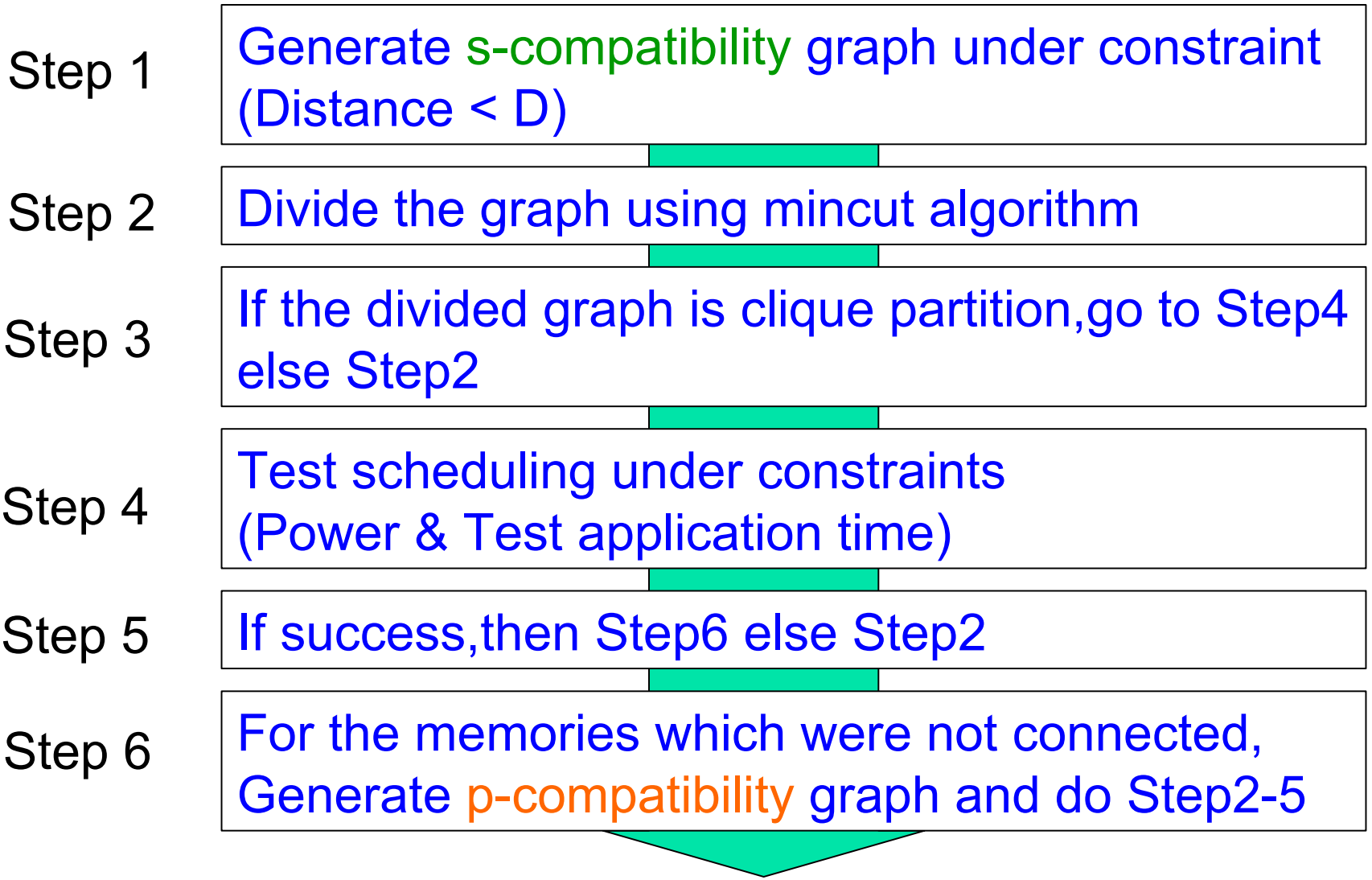
(2) Maximum test application time

(3) Maximum distance of connecting memories

Objective:

Minimize the area of Memory BIST logic

Memory grouping algorithm



Experiments

- Windows XP, 600MHz, 256MB memory
- 4 cases:

  Case 1: Not sharing

  Case 2: Parallel only

  Case 3: Serial only

  Case 4: Serial and Parallel

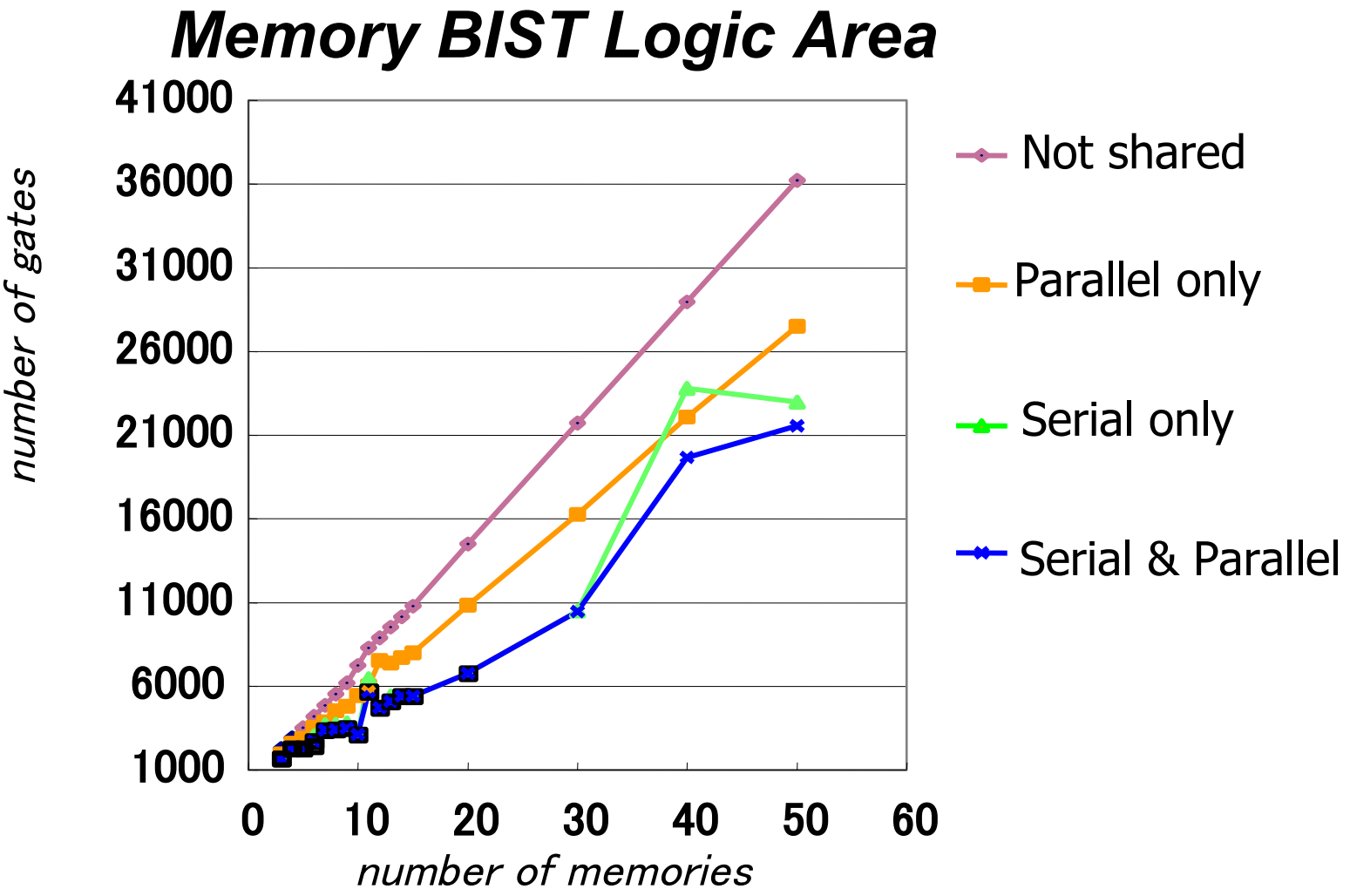
Memory Information and Constraints

No.	# data bit width	#Words	Frequency (MHz)	Power *1	Location	
					X	Y
1	16	128	133	100	10	10, 20, 30, 40, 50
2	16	128	133	100	20	
3	16	128	266	200	30	
4	16	128	266	200	40	
5	16	256	133	200	50	
6	16	256	133	200	60	
7	16	256	133	200	70	
8	16	256	133	200	80	
9	32	512	133	400	90	
10	32	512	133	400	100	

Constraints:
P=5000
T=0.3ms
D=40

*1 Relative values in which memory No.1 is assumed to be 100

Experimental results：



Conclusion

(1) Formulated a memory grouping problem

(2) Proposed an algorithm, which solves the memory grouping problem

(3) Showed effectiveness by experiments

- using two types of connection methods is able to reduce more area

Future work

(1) Improvement of the algorithm to achieve more good solution

(2) Problem formulation to minimize test application time