Signal-Path Driven Partition and Placement for Analog Circuit

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Agenda

- Research Background
- Overview of the analog placement researches
- Signal-Path Driven Analog Circuit Partition
- Algorithm of Core-Circuit Placement
- Algorithm of Bias-Circuit Placement
- Experiment and Conclusion

Research Background

- SOC integrates all of the circuits on one chip
- Analog circuits' design is still a manual process
- The fast changes of demands in ASIC market

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Researches about the analog placement automation

- The constructive placement techniques
  - M. Kayal--SALIM
- Iteratively combining min-cut partitioning and force-directed placement
  - E. Malavasi--Quick placement with geometric constraints
- simulated annealing and genetic algorithms
  - ILAC, KOAN/ANAGRAM II, PUPPY-A, LAYLA
- Topological representations (BSG, SP, CBL), which still adopts the optimization engines of *SA* or *GA* and implement symmetry constraints

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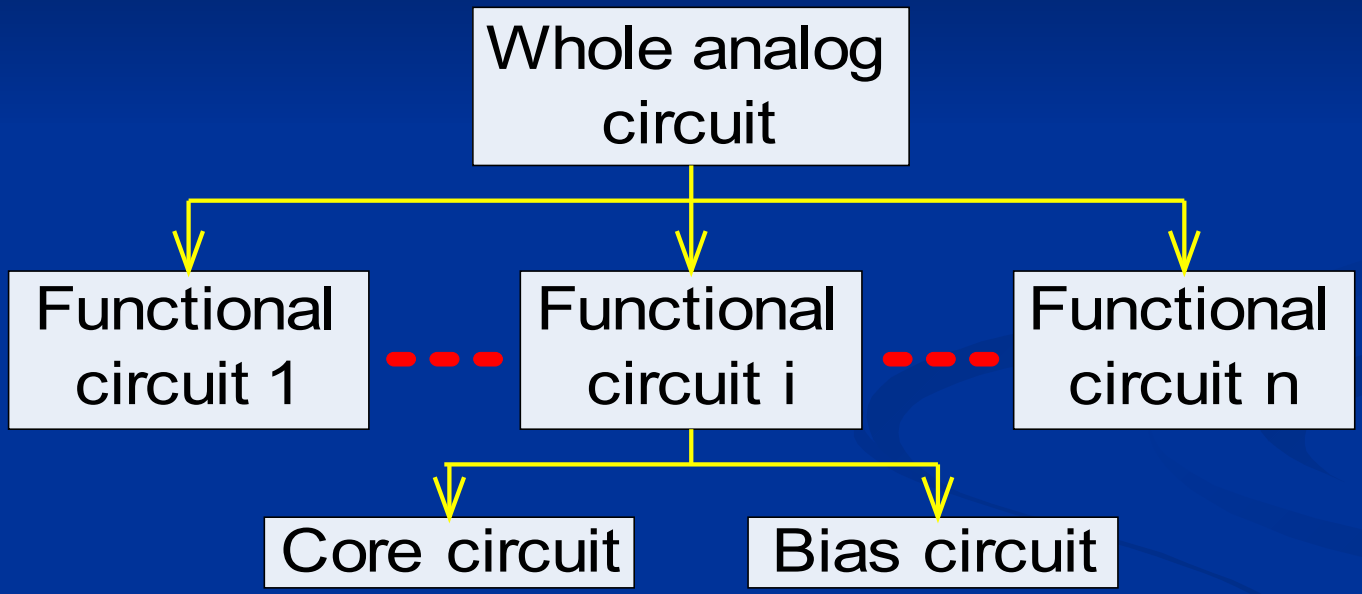
Observations of the Methodology

- hierarchical design for analog circuit
- structural feature of circuit based on signal-path
- requirements of matching/symmetry constraint and the reduction of parasitics

The methodology of hierarchical design and layout



Necessary Definition (1)

- **core-circuit**, which is the main circuit in each unit-functional circuit, is responsible for transporting and processing analog signal.
- **bias-circuit** is responsible for providing bias voltages and bias currents for some MOS transistors in core-circuit.

Necessary Definition (2)

- power-earth transistor chain is a chain composed of transistors satisfying the following conditions
  - The source/drain of each transistor in the chain must be connected to the power net or the earth net or the source/drain of another transistor in the same chain.
  - There is one and only one transistor in the chain, source/drain of which is connected to the power net and there is one and only one transistor in the chain, source/drain of which is connected to the earth net.

Necessary Definition (3)

- **signal-path is a special type of power-earth transistor chain, the generation algorithm of which is listed as follows:**

I: set of signal input nets

Γ_{pec}: set of all pecs

$Mj = \{ g_j, s_j, d_j \}$: set of transistor's gate net, source net and drain net

$\Phi = \{ Mj \mid Mj \cap \mathrm{I} \neq \phi \}$: set of initial input transistors

$\Psi_0 = \{ pec_i \mid pec_i \cap \Phi \neq \phi \}$: initial set of signal-paths can be defined

Necessary Definition (4)

- A loop procedure to generate the set of signal-paths

$$\Psi_{n+1} = \Psi_n \cup \Psi_{sd_n} \cup \Psi_{g_n}$$

$$\Psi_{sd_n} = \left\{ pec_i \mid \left(pec_i \not\equiv \Gamma_{pec} - \Psi_n \right) \Vdash \left(\exists pec \not\equiv \Psi_n \right) pec_i \cap pec \vdash \phi \right\}$$

$$\Psi_{g_n} = \left\{ pec_i \;\middle|\; \begin{array}{l} \left(pec_i \not\equiv \Gamma_{pec} - \Psi_n \right) \Vdash \left(\exists pec \not\equiv \Psi_n \right) \\ \left(\exists Mj \not\equiv pec_i \right) \left(\exists Mh \not\equiv pec \right) s_h = g_j \downarrow d_h = g_j \end{array} \right.$$

- The stop condition of the above loop procedure

$$\Psi_{sd_n} = \phi \Vdash \Psi_{g_n} = \phi$$

Comments on the sets

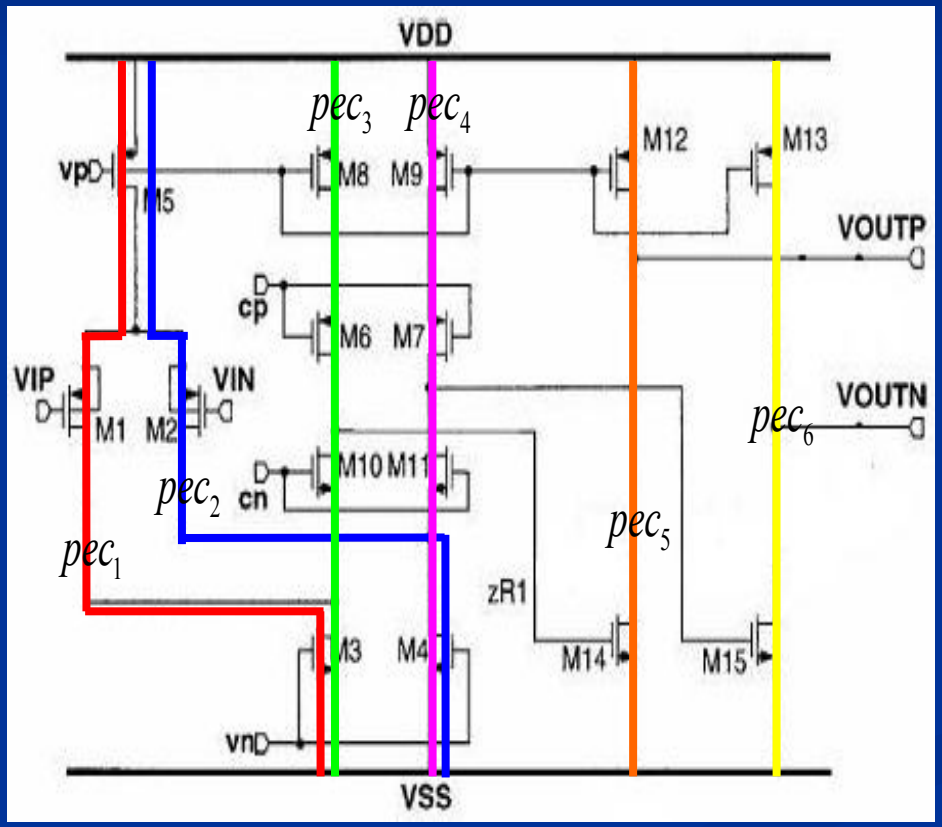
Ψ_{sd_n} : the current of pec_i in the set is controlled by the source/drain current of pec, which is the direct front-stage of pec_i

Ψ_{g_n} : the current of pec_i in the set is controlled by the source/drain voltage of pec, which is the direct front-stage of pec_i

Ψ_n is core-circuit and $\Gamma_{pec} - \Psi_n$ is bias-circuit

Example for signal-path generation (1)

- Schematics of full-differential Miller-compensated two-stage amplifier and the diagram of all pecs



$\Gamma_{pec} = \{pec_1, pec_2, ..., pec_6\}$ and $I = \{VIP, VIN\}$

so $\Phi = \{M1, M2\}$ and $\Psi_0 = \{pec_1, pec_2\}$

when $n = 0$, $\Psi_{sd_0} = \{pec_3, pec_4\}$ and $\Psi_{g_0} = \phi$

So $\Psi_1 = \Psi_0 \cup \Psi_{sd_0} \cup \Psi_{g_0} = \{pec_1, pec_2, pec_3, pec_4\}$

when $n = 1$, $\Psi_{sd_1} = \phi$ and $\Psi_{g_1} = \{pec_5, pec_6\}$

So $\Psi_2 = \Psi_1 \cup \Psi_{sd_1} \cup \Psi_{g_1} = \{pec_1, pec_2, pec_3, pec_4, pec_5, pec_6\}$

when $n = 2$, $\Psi_{sd_2} = \phi$ and $\Psi_{g_2} = \phi$, stop

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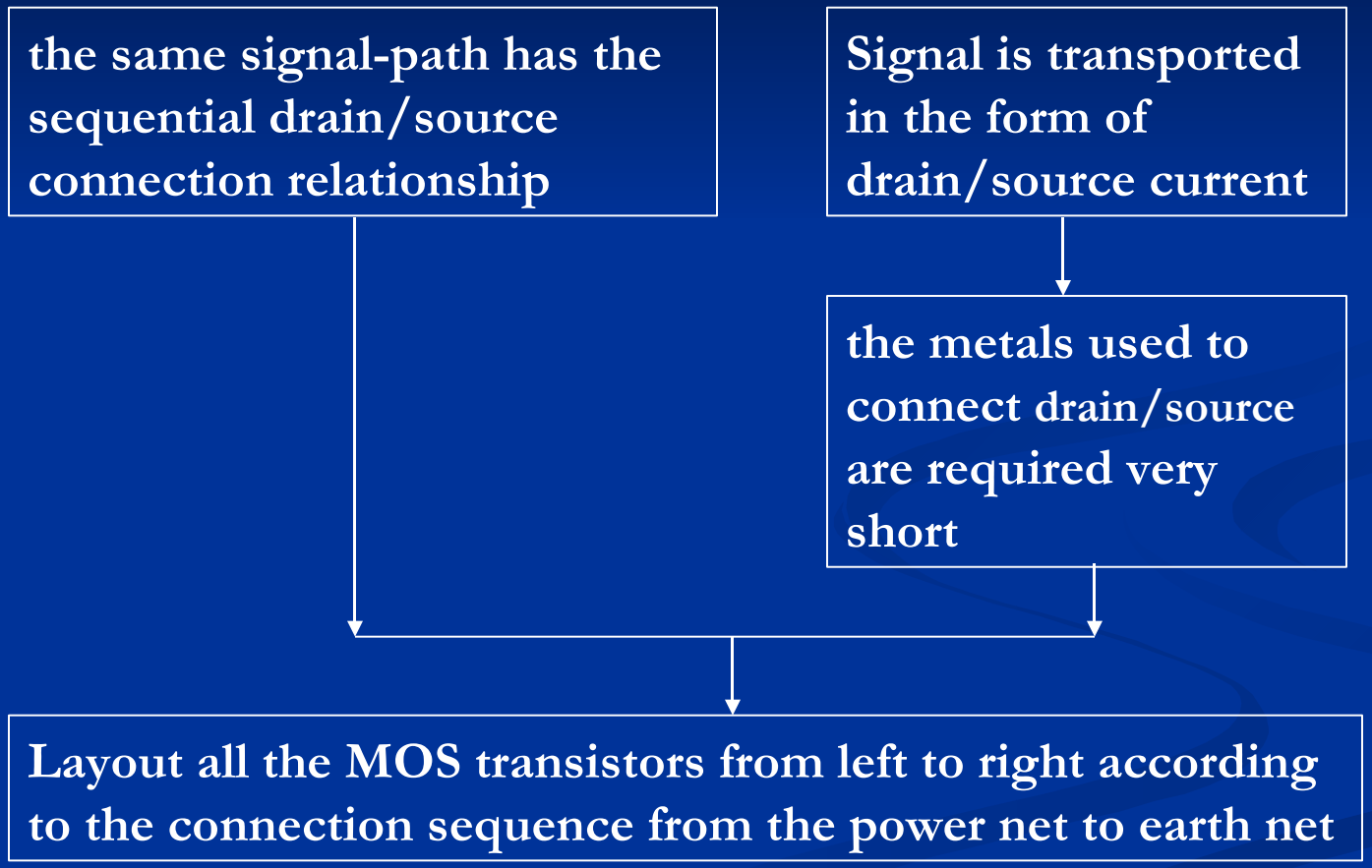
Inner placement of each signal-path



whole placement of the core-circuit

- **Consideration: metals used to connect the nets among signal-paths are to transport the voltage, so these metals are not required very short**

  assuming $\Psi_n = \{ pec_1, ..., pec_j \}$

  $\Psi_0, \Psi_{sd_0}, \Psi_{g_0}, ..., \Psi_{sd_{n-1}}, \Psi_{g_{n-1}}$ is arranged by generation sequence

- **core-circuit is full-symmetrical structure**

  Ψ_n is divided into $\Psi S_n = \{ pec_1, ..., pec_{j/2} \}$ and $\Psi M_n = \{ pec_{1+j/2}, ..., pec_j \}$

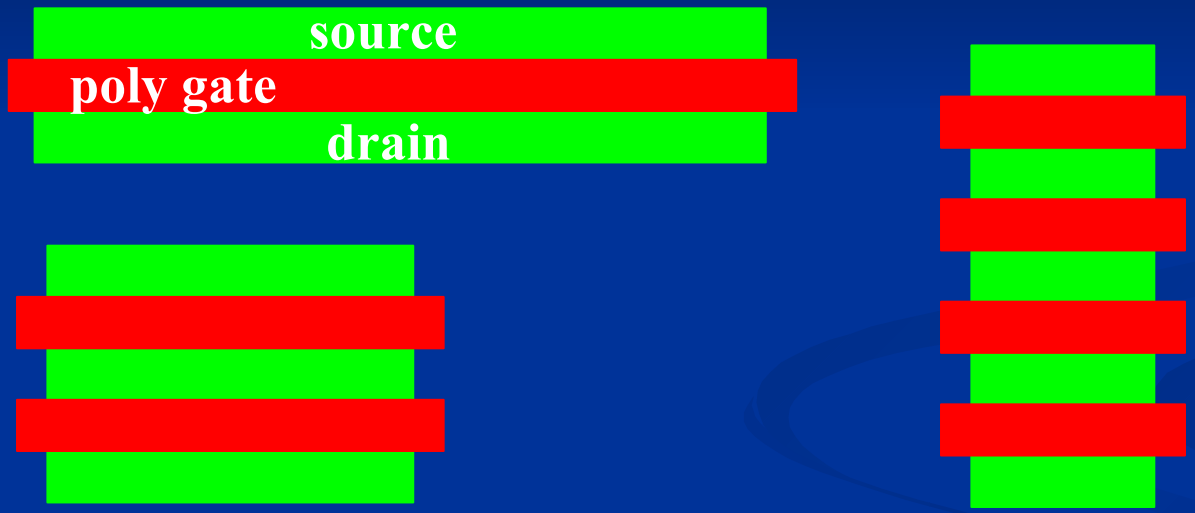
- **core-circuit is not full-symmetrical structure**

- **part but not all of transistors in pec_i have symmetry constraints with others in pec_j**

Objectives of the core-circuit placement

- minimizing the differences of the height of all MOS transistor layouts in the same signal-path;
- minimizing the differences of the width of all signal-paths in the core-circuit;
- minimizing the total capacitance parasitics of all the MOS transistors;
- maximizing the area utility.

Transistor's variants for objectives implementation



$$W_m \text{ I } F_m = W_n \text{ I } F_n$$

Cost function to be optimized

$$CP_{core} = \alpha H_{\max\_diff} + \beta W_{\max\_diff} + \gamma P_{cap} + \delta \left(1 - U_{area}\right)$$

$$H_{\max\_diff} = \max_{pec_k \in \Psi_n} \left[\max_{M_{k,i}, M_{k,j} \in pec_k} \left| height\left(M_{k,i}\right) - height\left(M_{k,j}\right) \right| \right]$$

$$W_{\max\_diff} = \max_{pec_i, pec_j \in \Psi_n} \left| width\left(pec_i\right) - width\left(pec_j\right) \right|$$

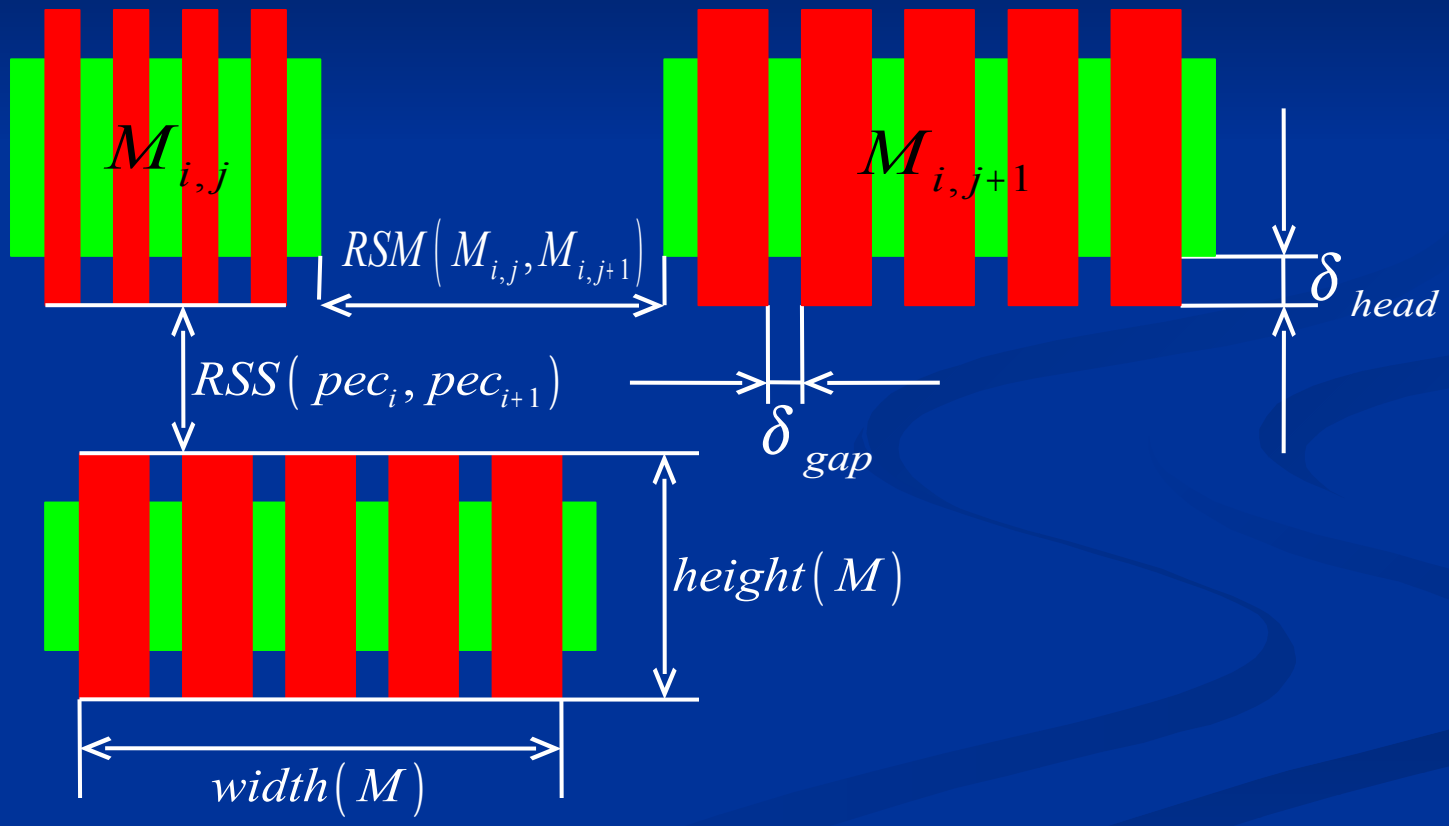
$$P_{cap} = \sum_{i=1}^{n} \sum_{j=1}^{h(i)} C_{jBSt}\left(F_{i,j}\right)$$

$$U_{area} = \frac{\sum_{i=1}^{l} \sum_{j=1}^{h(i)} height\left(M_{i,j}\right) \times width\left(M_{i,j}\right)}{\max_{pec_i \in \Psi_n} \left[width\left(pec_i\right) \right] \times \left[\sum_{i=1}^{l} \max_{M_{i,j} \in pec_i} \left[height\left(M_{i,j}\right) \right] \right] + \sum_{i=1}^{l-1} RSS\left(pec_i, pec_{i+1}\right)}$$

$$height\left(M_{i,j}\right) = W_{i,j} / F_{i,j} + 2\delta_{head}$$

$$width\left(pec_i\right) = \left[\sum_{j=1}^{h(i)} F_{i,j} L_{i,j} + \left(F_{i,j} + 1\right) \delta_{gap} \right] + \sum_{j=1}^{h(i)-1} RSM\left(M_{i,j}, M_{i,j+1}\right)$$

Calculation of distance between transistors



Calculation of source/drain bulk capacitance

$$C_{jSBt} = \frac{AC_j}{\left(1 - \frac{V_{BS}}{\phi_j}\right)^{m_j}} + \frac{PC_{js\omega}}{\left(1 - \frac{V_{BS}}{\phi_j}\right)^{m_{js\omega}}}, \text{ let } \alpha = \left(1 - \frac{V_{BS}}{\phi_j}\right)^{m_j} \text{ and } \beta = \left(1 - \frac{V_{BS}}{\phi_j}\right)^{m_{js\omega}}$$

$$C_{jSBt}(F) = \left(\alpha WL + \alpha W\delta_{gap} + 2\beta\delta_{gap}\right) + 2\beta\left(L + W\delta_{gap}\right)F + W\left(\alpha\delta_{gap} + 2\beta\right)\frac{1}{F}$$

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Objectives of the bias-circuit placement

- minimizing the total parasitic capacitance of all the MOS transistors belonging to the bias-circuit;
- minimizing the total length of routing metals;
- maximizing the area utility.

$$CP_{bias} = \omega P_{cap} + \theta L_{routing} + \lambda \left(1 - U_{area}\right)$$

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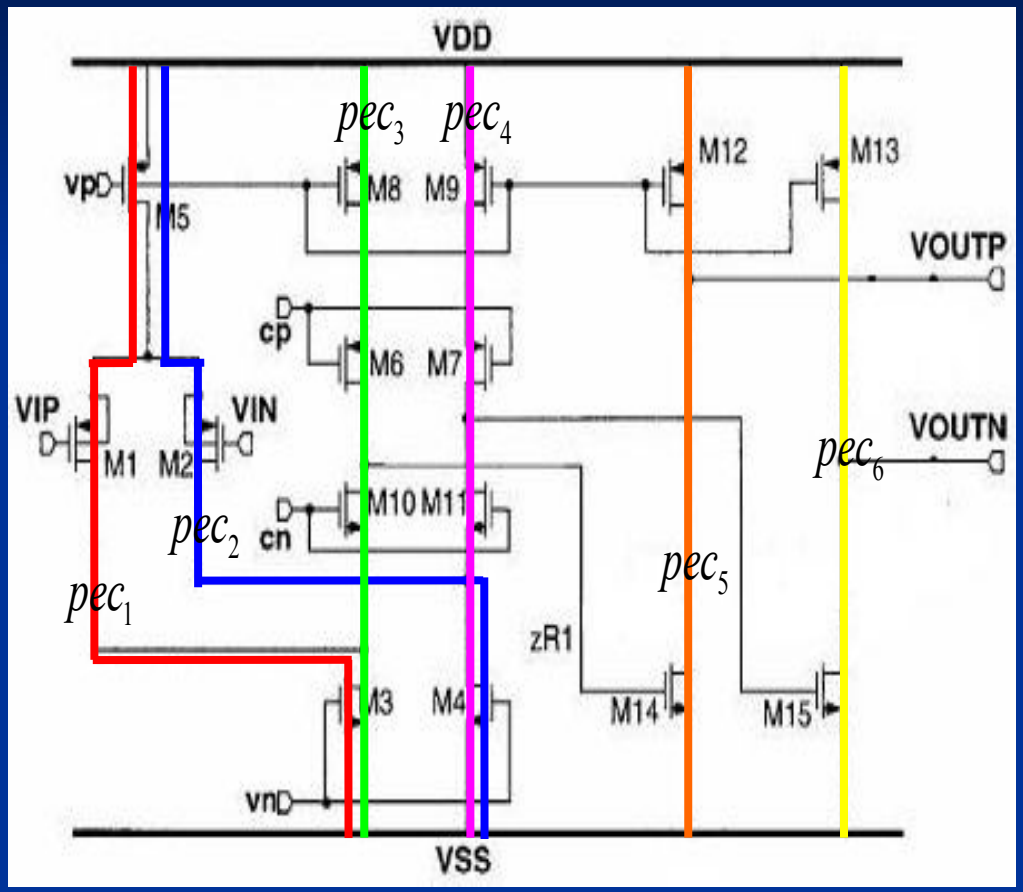
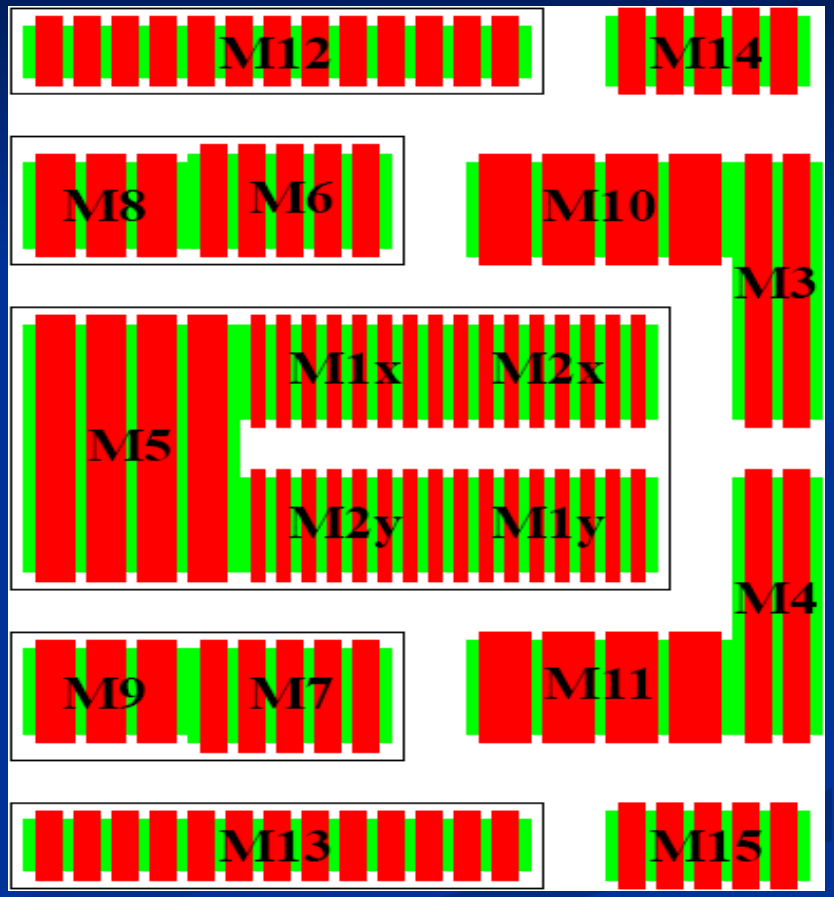
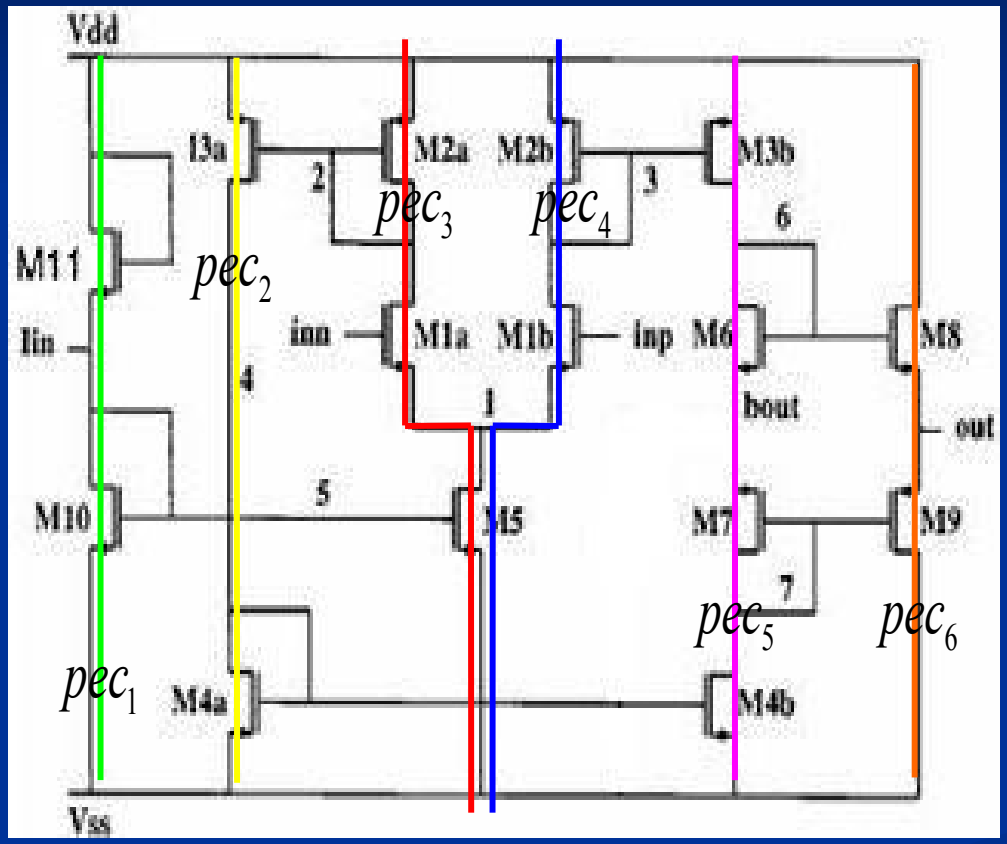
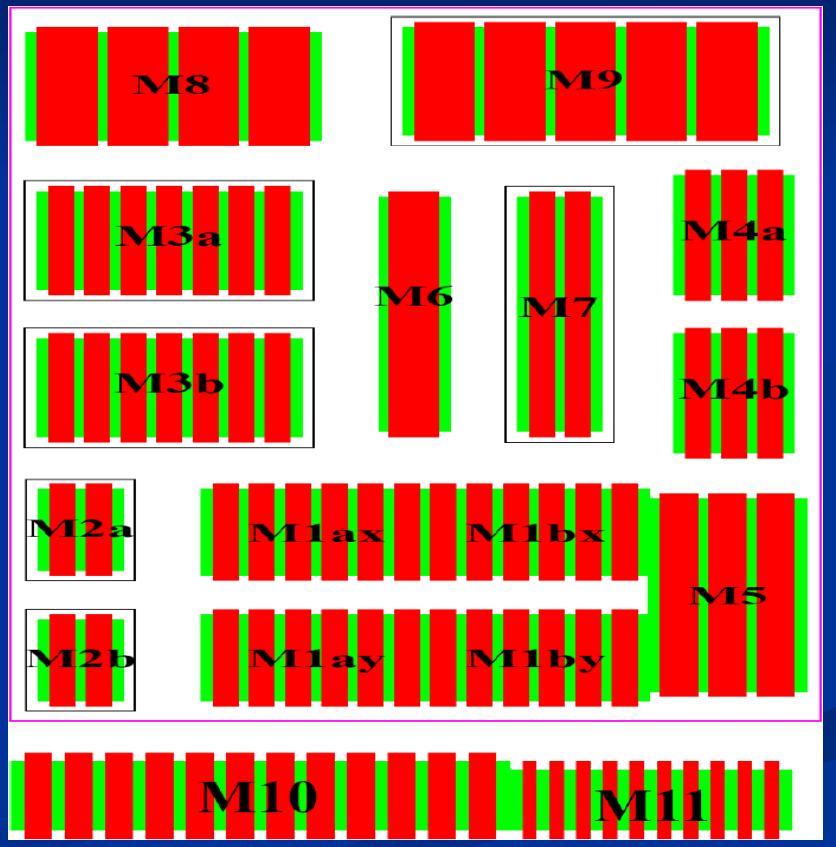
Case 1


VDD
VSS
vpD
M5
M8
M9
M12
M13
VOUTP
cp
M6
M7
VIP
VIN
M1
M2
VOUTN
M10
M11
cn
zR1
M3
M4
M14
M15
vnD
pec_1
pec_2
pec_3
pec_4
pec_5
pec_6

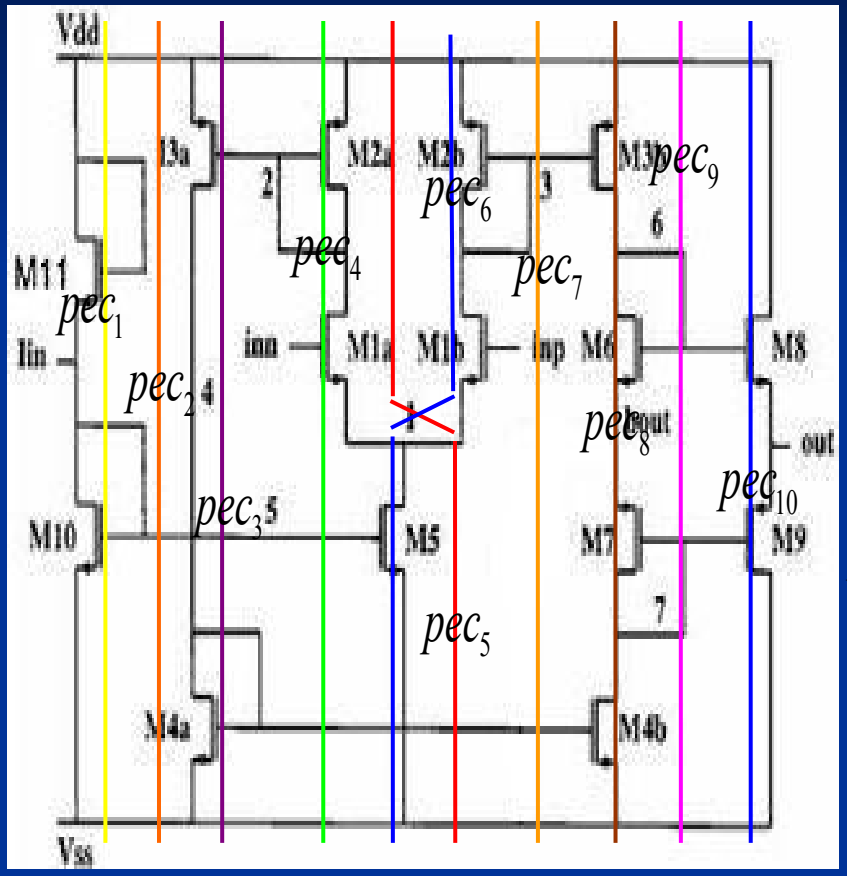

M12
M14
M8
M6
M10
M3
M1x
M2x
M5
M2y
M1y
M4
M9
M7
M11
M13
M15

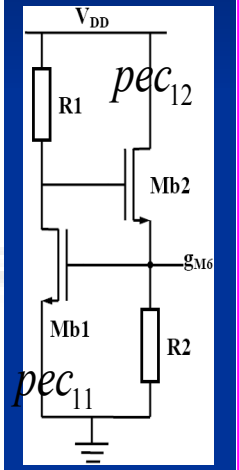
Case 2

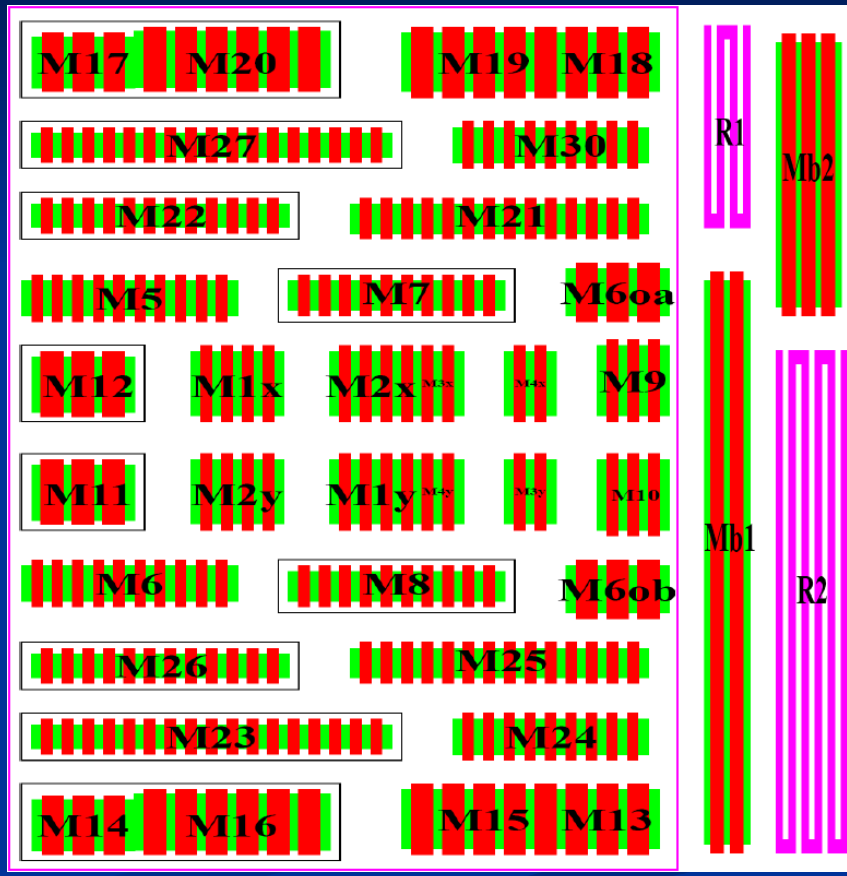

Vdd
I3a
M2a
M2b
M3b
2
3
6
M11
Iin
inn
M1a
M1b
inp
M6
M8
4
1
bout
out
M10
5
M5
M7
M9
7
M4a
M4b
Vss


M8
M9
M3a
M6
M7
M4a
M3b
M4b
M2a
M1ax
M1bx
M5
M2b
M1ay
M1by
M10
M11

Case 3


Vdd
M13a
M2a
M2b
M3b
M11
pec1
pec9
pec6
2
3
6
pec4
pec7
iin
inn
M1a
M1b
inp
M6
M8
pec2
4
pec8
pout
out
pec10
M10
pec3
5
M5
M7
M9
pec5
7
M4a
M4b
Vss


VDD
R1
pec12
Mb2
gM6
Mb1
R2
pec11


M17
M20
M19
M18
M27
M30
M22
M21
M5
M7
M60a
M12
M1x
M2x
M9
M11
M2y
M1y
M10
M6
M8
M60b
M26
M25
M23
M24
M14
M16
M15
M13
R1
Mb2
Mb1
R2

Conclusions

- a new methodology of signal-path driven partition and placement for analog
  - the thinking of hierarchical design
  - structural feature of analog circuit based on signal-path
  - variants of MOS transistors.
- Layout is compact with high performance and it is universal and effective.

Thank you