An Approach to Topology Synthesis of Analog Circuits Using Hierarchical Blocks and Symbolic Analysis

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Outline

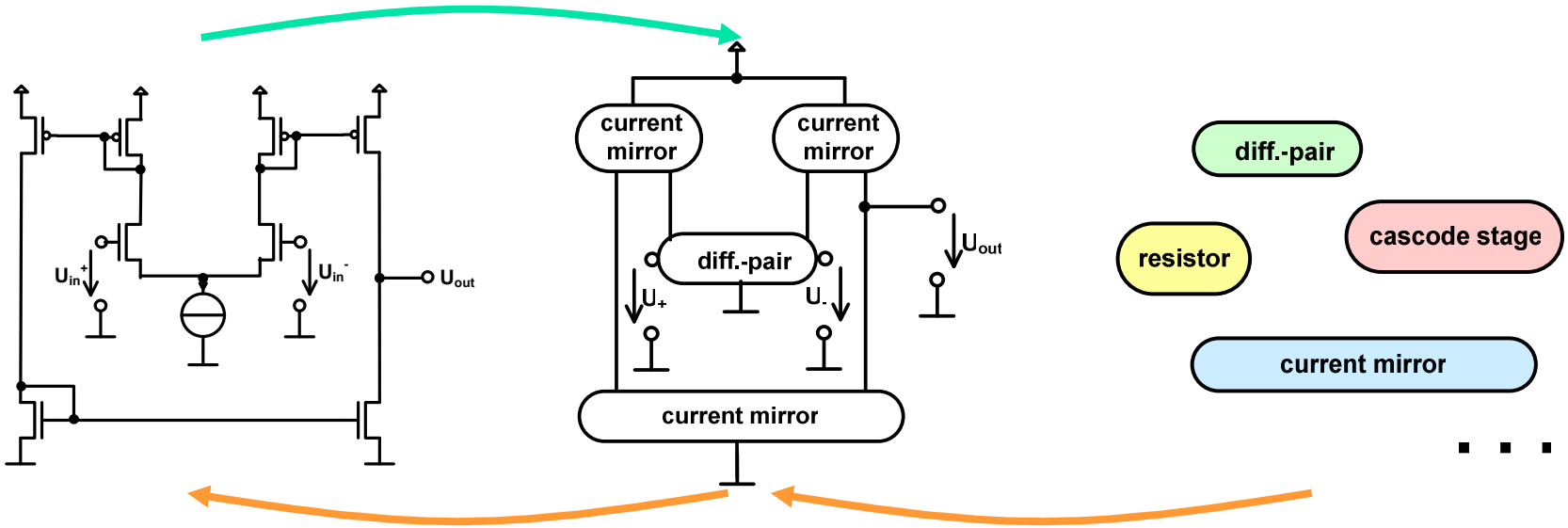
- Introduction
- Topology generation
  - Hierarchical blocks
  - Synthesis rules
- Topology selection
  - Symbolic analysis
- Synthesis results
- Conclusion

Motivation

- Automatic design of analog circuits
  - Support for designer
  - Reduce time to market

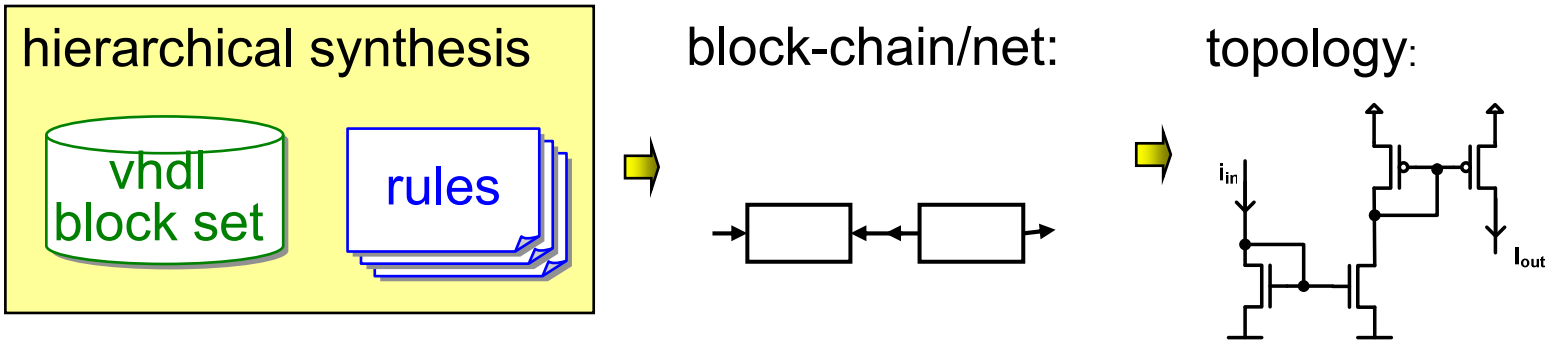
- Exploration of structural design space
  - Find appropriate circuits methodically and systematically
  - Analyze and evaluate performances quickly

Hierarchical View of Circuits



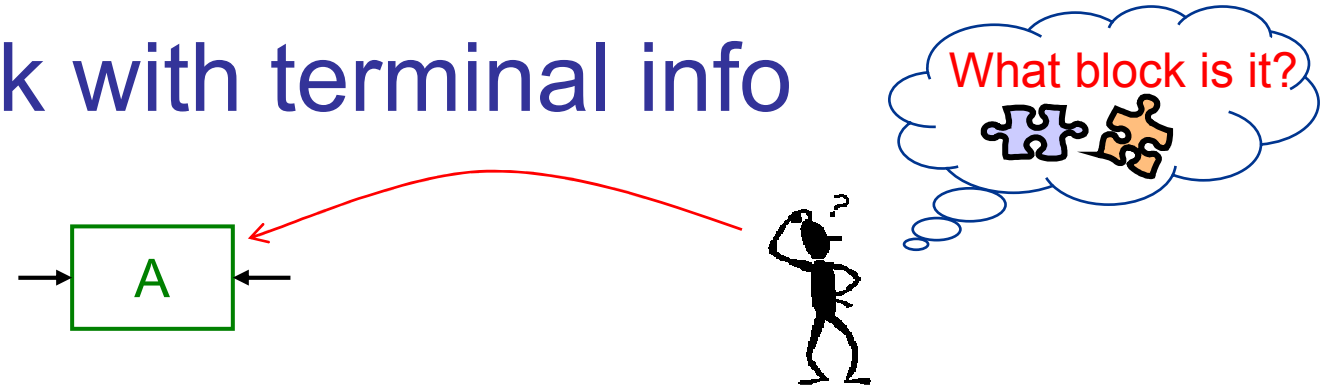
- Sizing tools (e.g. WiCkeD)
- Topology synthesis, e.g.:
  - Rutenbar et al. (OASYS): topology library
  - Dastidar et al.: genetic algorithm
  - Our: rules-based algorithm

Hierarchical Topology Synthesis

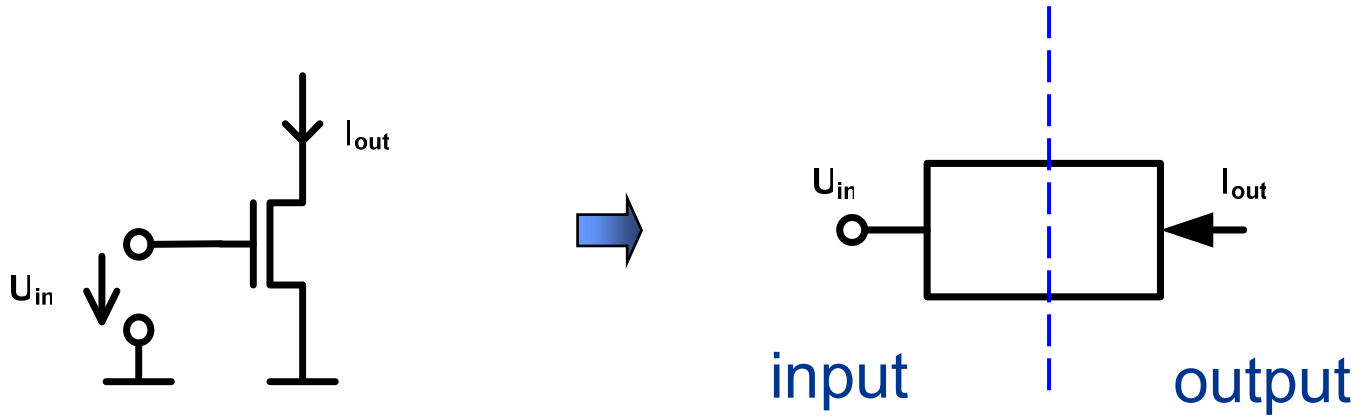


- A set of well defined blocks with specialized signal information of terminals
- Synthesis rules for combination between blocks
- Block-chains/nets can represent the topology of circuits

Block with terminal info

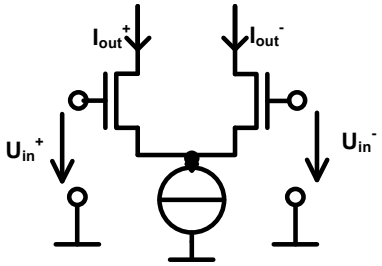


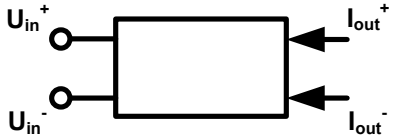
- Type of signal: *voltage (U)* or *current (I)*
  - Current direction: determined by the bias current
- Type of terminal: *input* or *output*
- Impedance: *low* or *high*



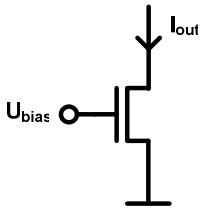
Examples of blocks

- Differential pair

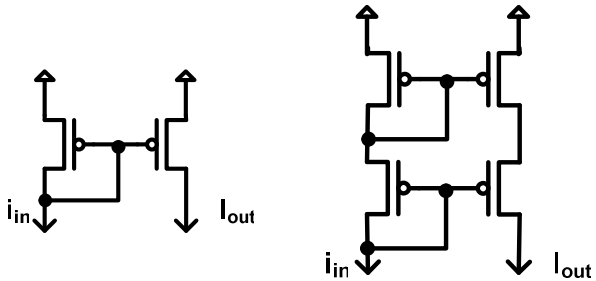




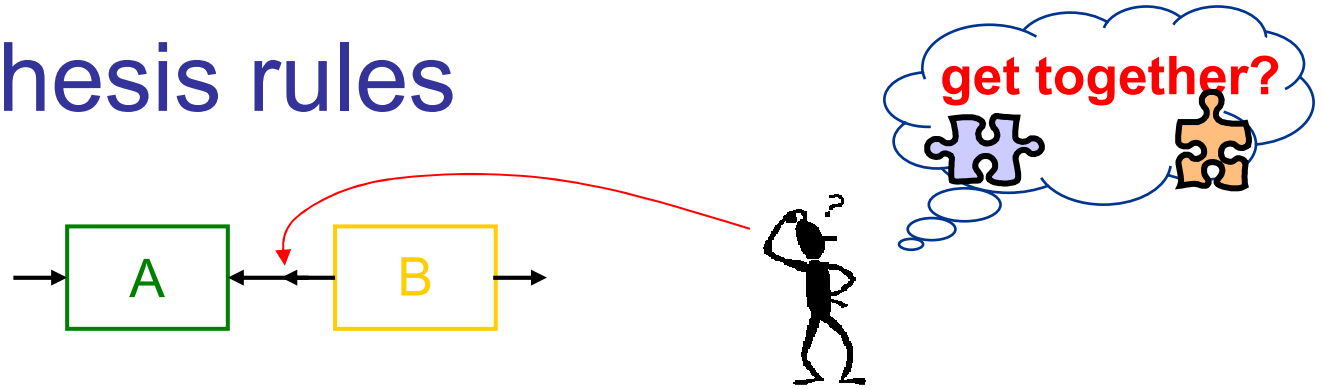
- Current source



- Current mirror (basic & cascode)



Synthesis rules

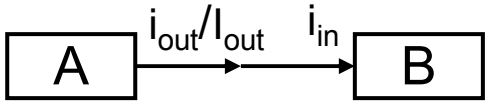


- General rules
  - Connection between two blocks
  - One dimension
- Current source rule
  - Adding Current source between two blocks
  - Quasi-one dimension
- Split & combination rules
  - Expanding the connection between blocks
  - Two dimensions

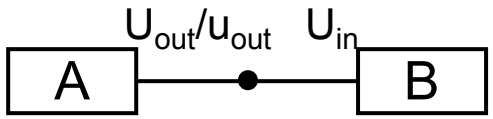
General rules

- Signal type rule
  - current to current, voltage to voltage

- Current rule
  - Matched bias current direction
  - Low input impedance of block B

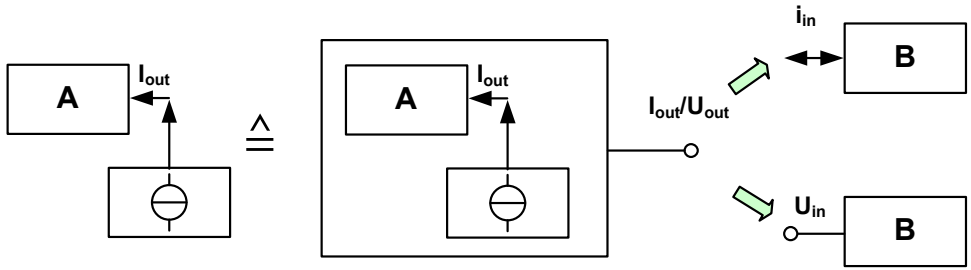


- Voltage rule
  - High input impedance of block B

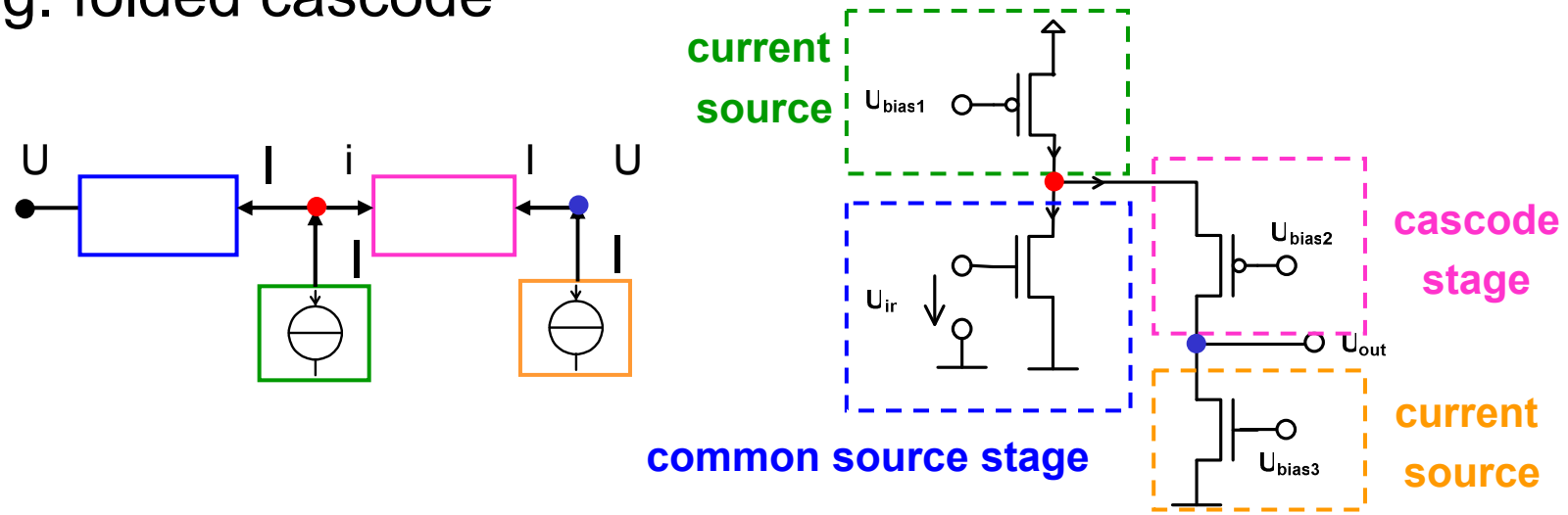


Current Source Rule

- Block A with current source can be treated as a block with either current or voltage output.

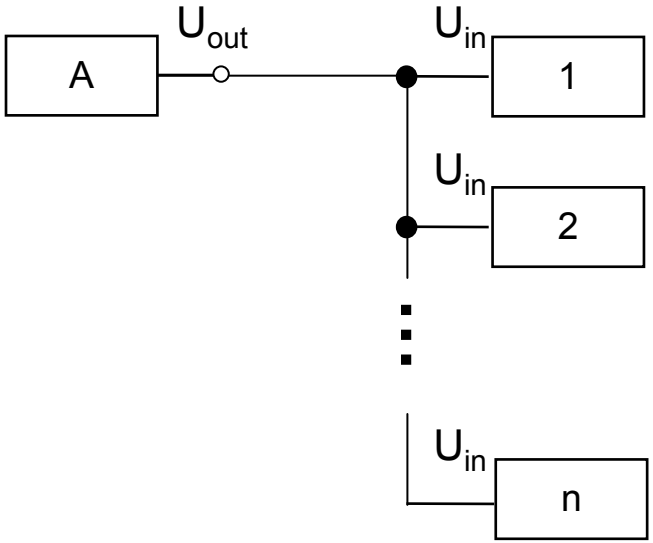


- E.g. folded cascode

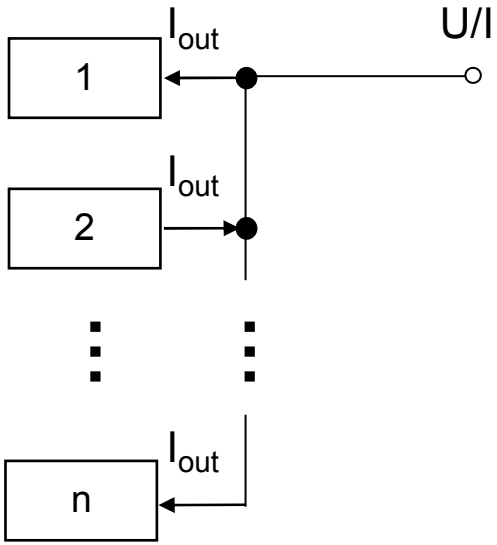


Split & Combination Rules

- Split rule (voltage)

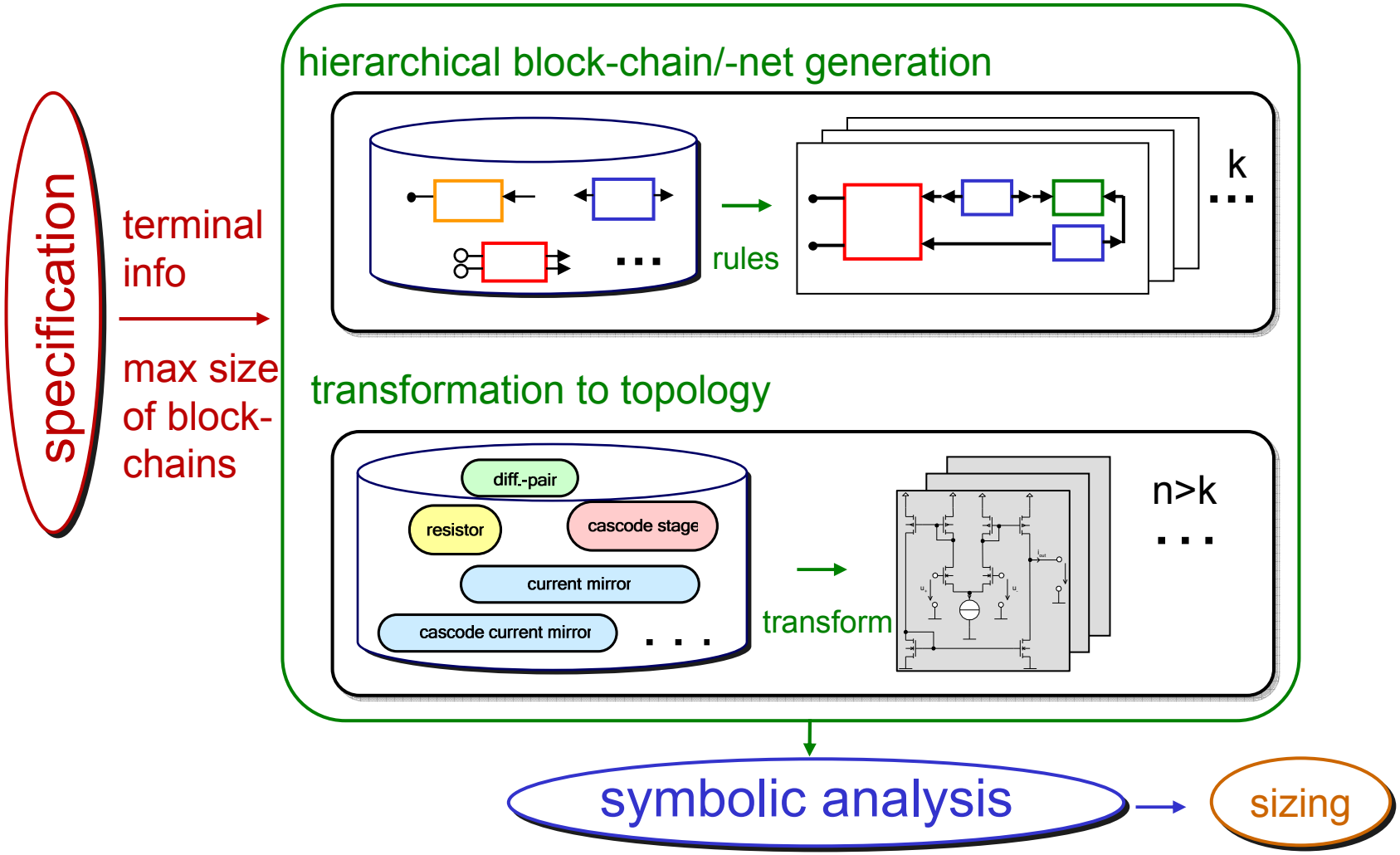


- Combination rule (current)



- Typical application area: differential pair

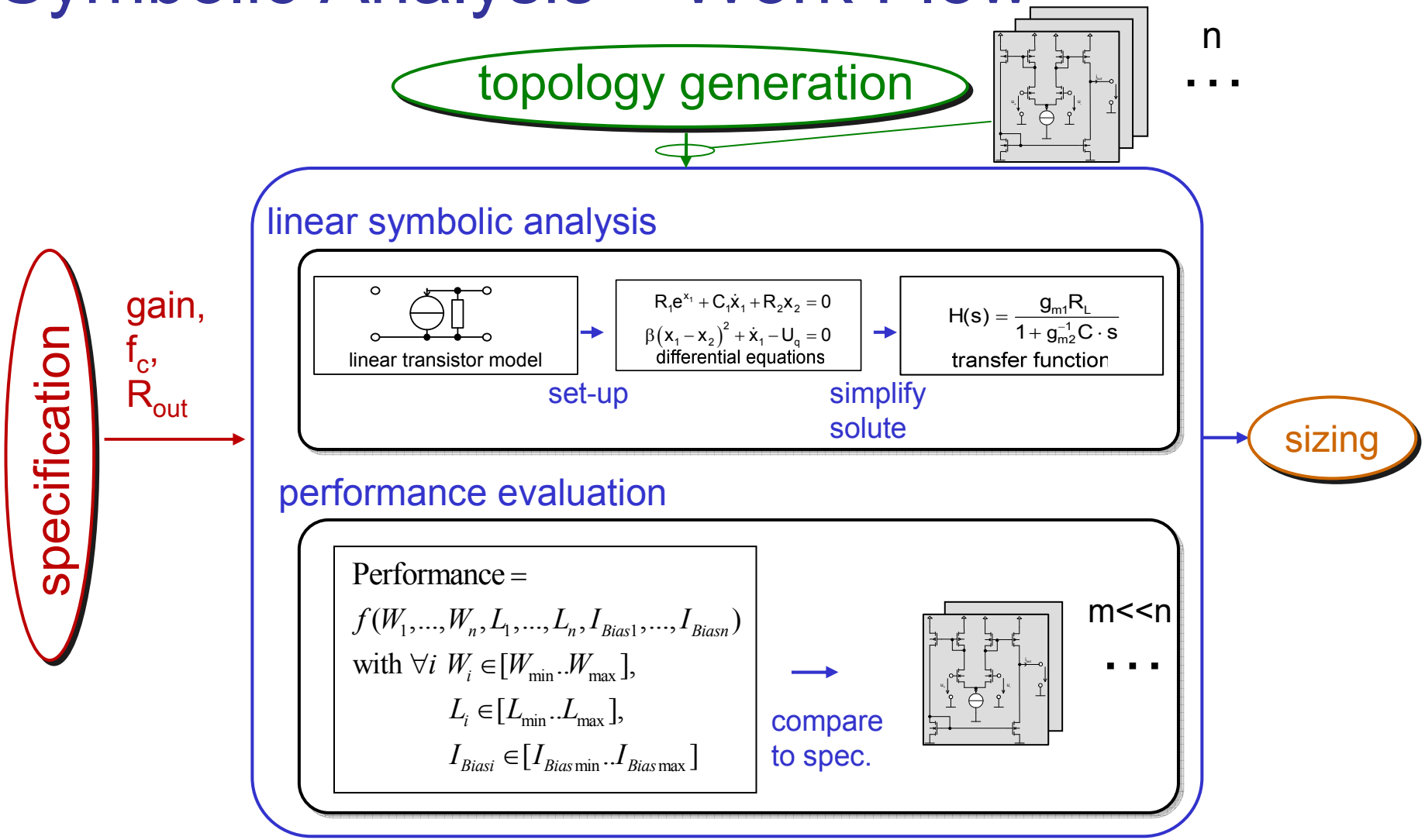
Topology Generation – Work Flow



Topology Selection – Symbolic Analysis

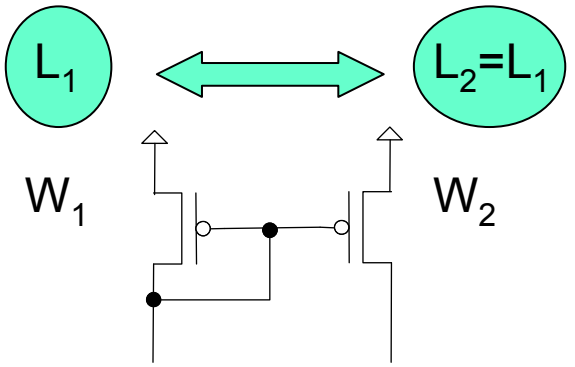
- Goal of topology selection
  - Reduce high number of synthesized circuits
  - Short run time
- Symbolic analysis
  - Fast performance estimation
  - Performance $\Leftrightarrow$ parameter dependencies
  - Simple design equations $\Rightarrow$ Initial sizing

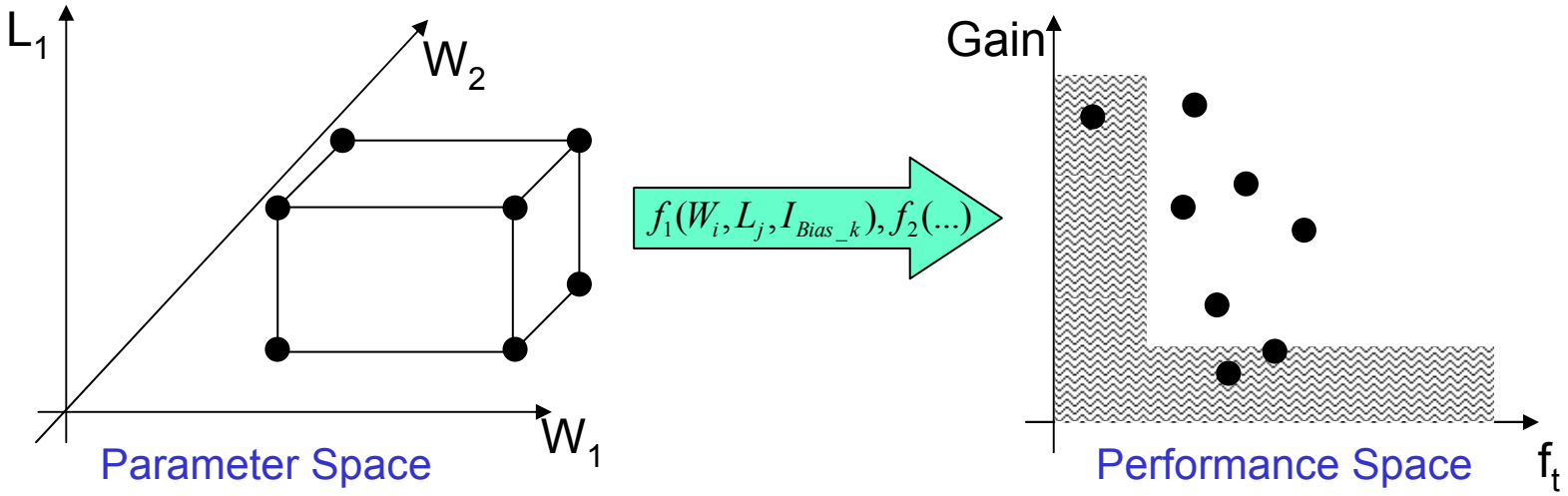
Symbolic Analysis – Work Flow



Performance Estimation

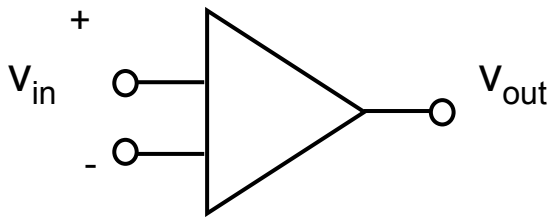
- Linear performances
- Structural constraints
- Parameter dependencies given by symbolic expressions



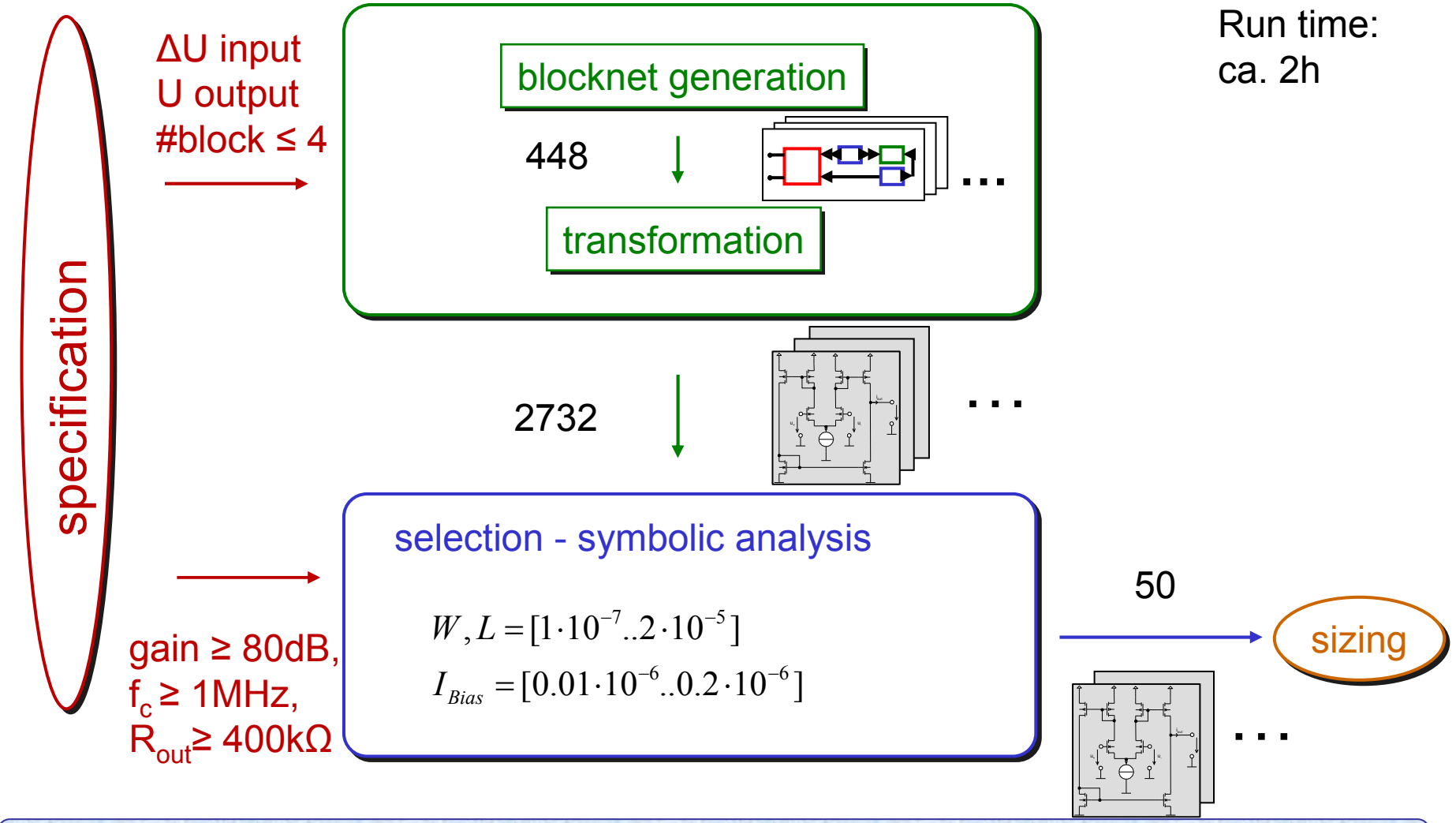


Results – Unbuffered Op Amp (I)

- Op amp without a buffered output stage
- Terminal information:
  - Differential voltage input with high impedance
  - Voltage output with high impedance



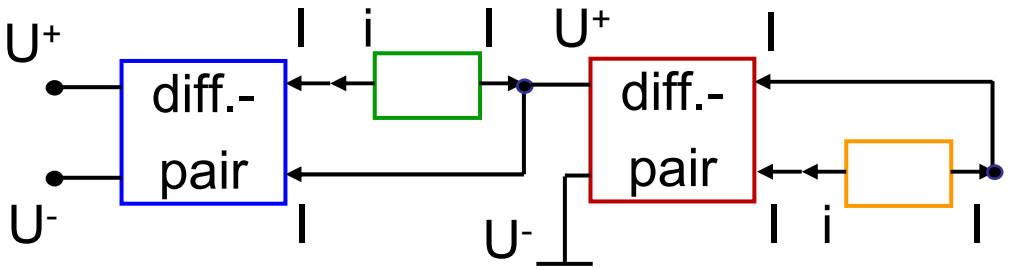
Results – Unbuffered Op Amp (II)



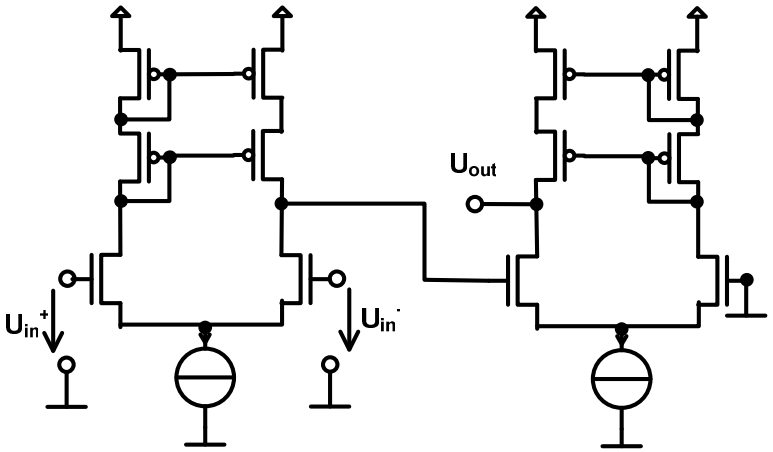
Run time:
ca. 2h

Results – Unbuffered Op Amp (III)

- 1 of 50 results: block-net



- Schematic



- Estimated performances
  - gain = 81.3 dB
  - f_c = 1.01MHz,
  - R_{out} = 5MΩ

Conclusion

- A new concept of circuit synthesis
  - Exhaustive exploration of structural space with respect to
    - Predefined hierarchical blocks
    - Structural restrictions by rules
    - Limited size of block chain
  - Symbolic analysis
    - Fast performance evaluation
  - First results for standard linear circuits

Future work

- Circuit classes
  - Mixer, output stage
  - …
- Automatic Sizing

Thank you!