Yield-preferred Via Insertion Based on Novel Geotopological Technology

Yongbo Jia

Nannor Technologies, Inc.

ASPDAC, January 27, 2006

What's the problem?

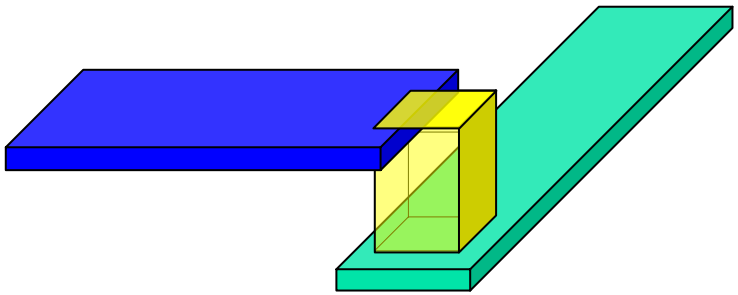
- The feature size continues scaling down
- The design size continues increasing
  - 2003, 0.13um, 180 million transistors
  - 2004, 90nm, 220 million transistors
  - 2007, 65nm, 457 million transistors
- More metal layers and more vias
  - over 15 million vias/design
- Via reliability increasingly becomes important
  - 0.13 um, 16 million vias, Via failure ratio: 1.8/billion
  - Almost 3% yield loss

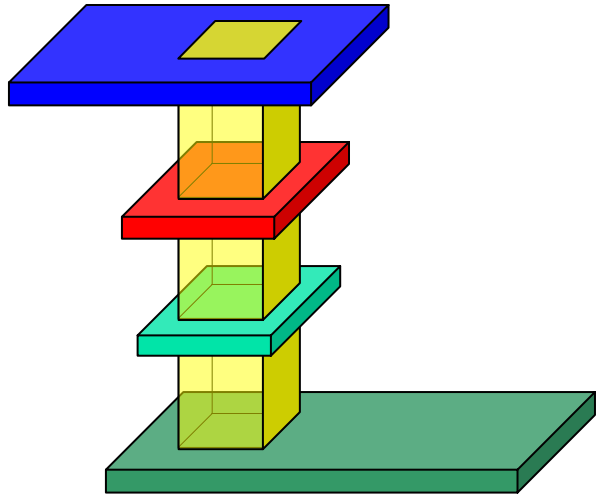
Via failures

- Random cut failures in Copper
  - Voids in Cu migrate under thermal stress towards vias
  - When enough voids accumulate at a via, it causes a bad interconnection
    - High resistance
    - Complete open
  - Worse in 90nm, 65nm process technology and below
    - Smaller vias

Via failures

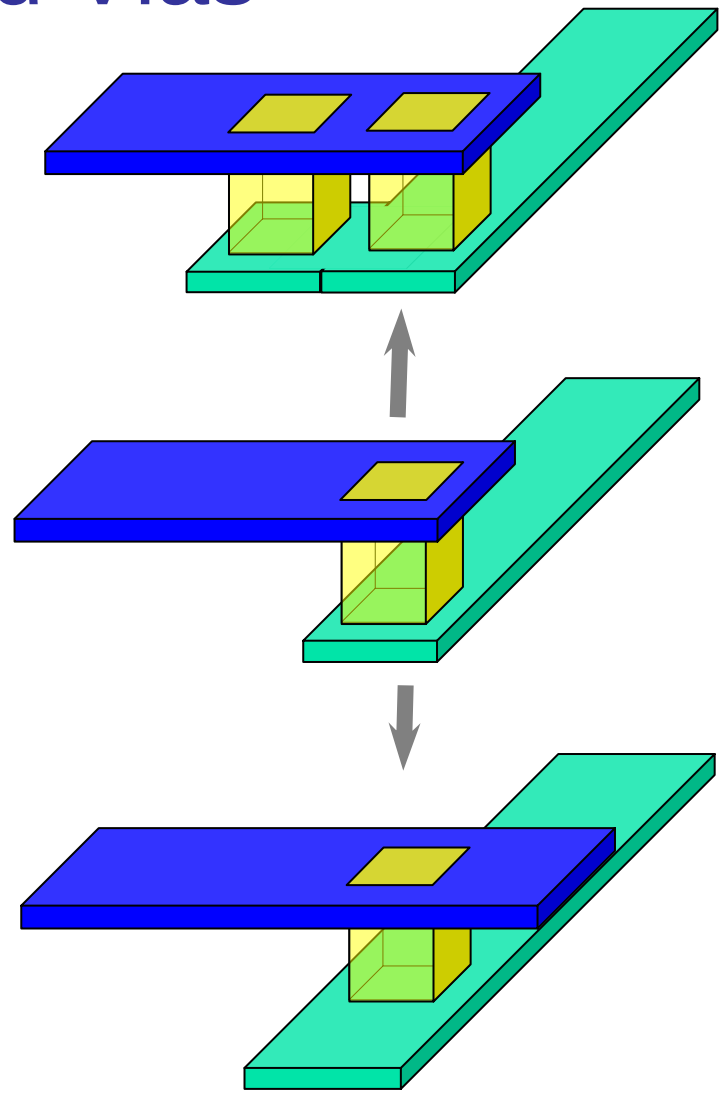
- Systematic failures
  - Misalignment
  - Cut partially or completely falls outside of the metal coverage
  - Worse for stack vias





Remedy: Yield-preferred Vias

- Redundant-cut via:
  - At least one redundant cut
  - Not required in functionality
  - Reduce via failure
- More metal coverage
- Major foundries are already encouraging the usage of yield-preferred vias



Existing approaches

- Detail Routers
  - Headache in making a routable design
  - Headache in meeting timing/SI requirements
  - Headache in handling complex 90nm/65nm design rules
  - More headaches …
  - ONE MORE headache : yield-preferred vias
    - Various yield-preferred via configurations
    - Hard to make the online decisions:
      - Where to apply
      - Which one is the best
      - Priority decision
    - Potential to increase die size

Existing approaches

- GDSII Based Tools
  - Very slow
  - Lowest rate, extremely limited local adjustment
  - Lose control of the design at the tapeout stage
  - Can not feedback the optimized layout to previous stages

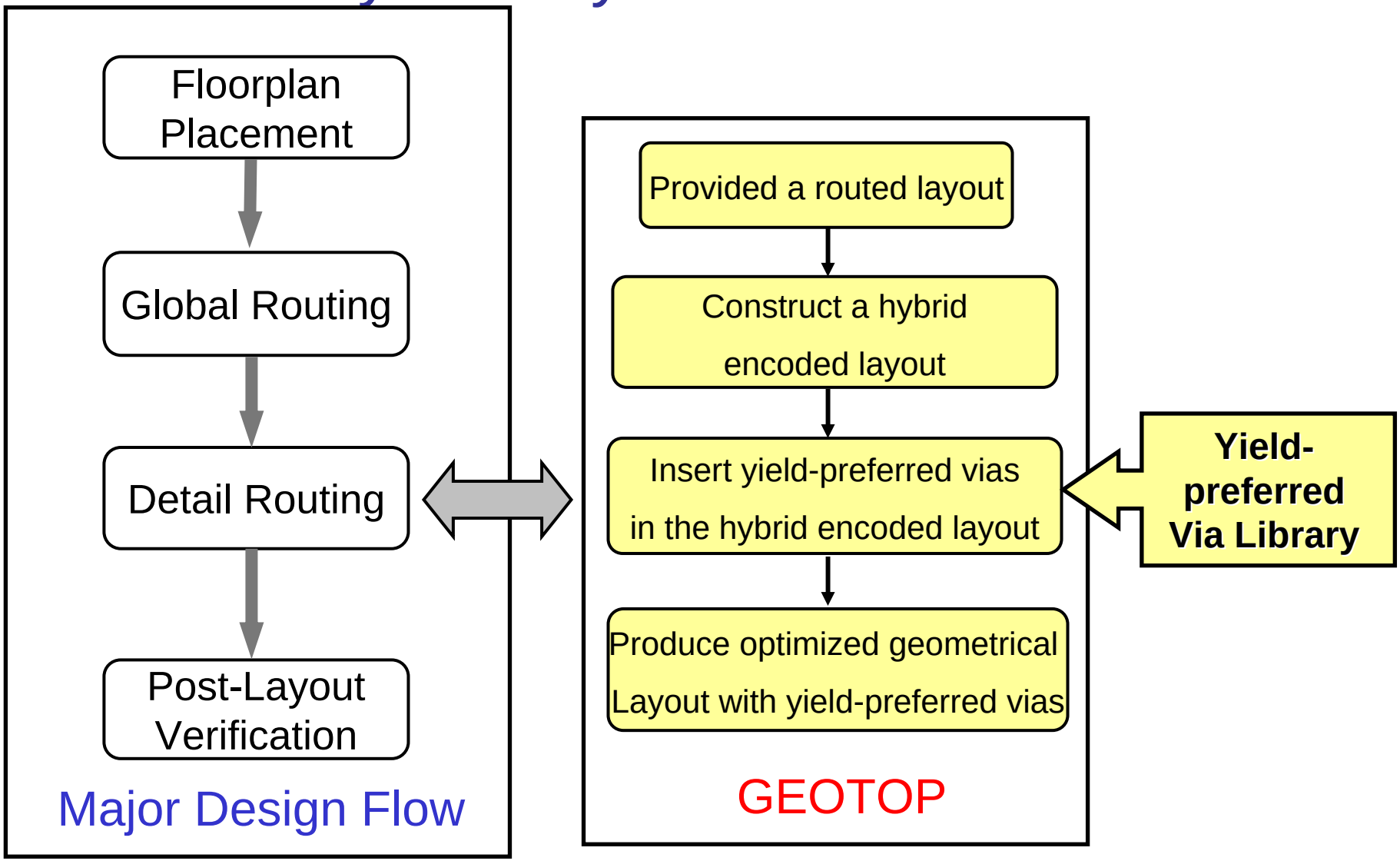
Our Goal

- Help designers to get the best yield benefit by applying yield-preferred vias in the design
- Keep the design target
  - Timing, power……
- Keep the die size unchanged
- Fast running time
- Compatible with major design flows
  - Plug-in and play
  - Verification after optimization

GEOTOP: GEOmetry-TOPology Hybrid Encoding Technology

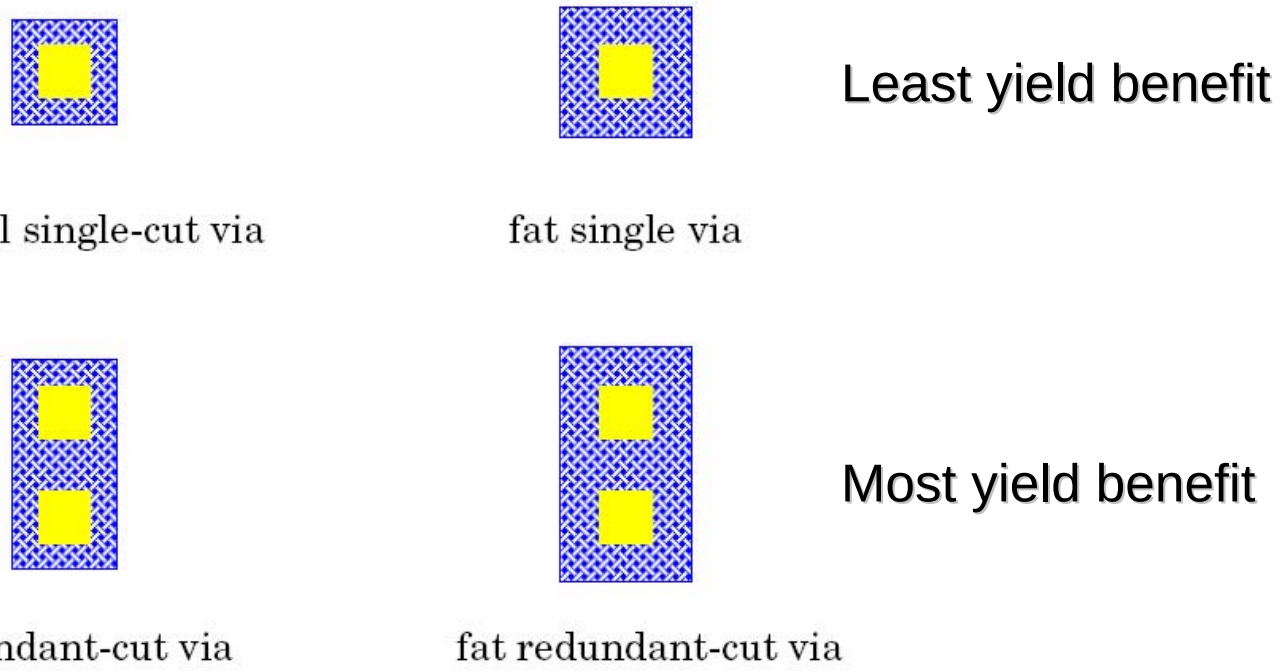
- Topological encoding technology
  - Naturally powerful, flexible in manipulating the layout
  - May suffer from losing consistence to the original layout
- GEOTOP: Enhanced topological encoding technology
  - Keeps the necessary geometrical information in the topological encoded layout
    - Preserve the geometrical paths of desired nets
    - Topologically encoding the rest
  - Combines the flexibility of topological encoding technology and the consistence to the original layout

Yield-preferred Via Insertion Based on GEOTOP Hybrid Layout



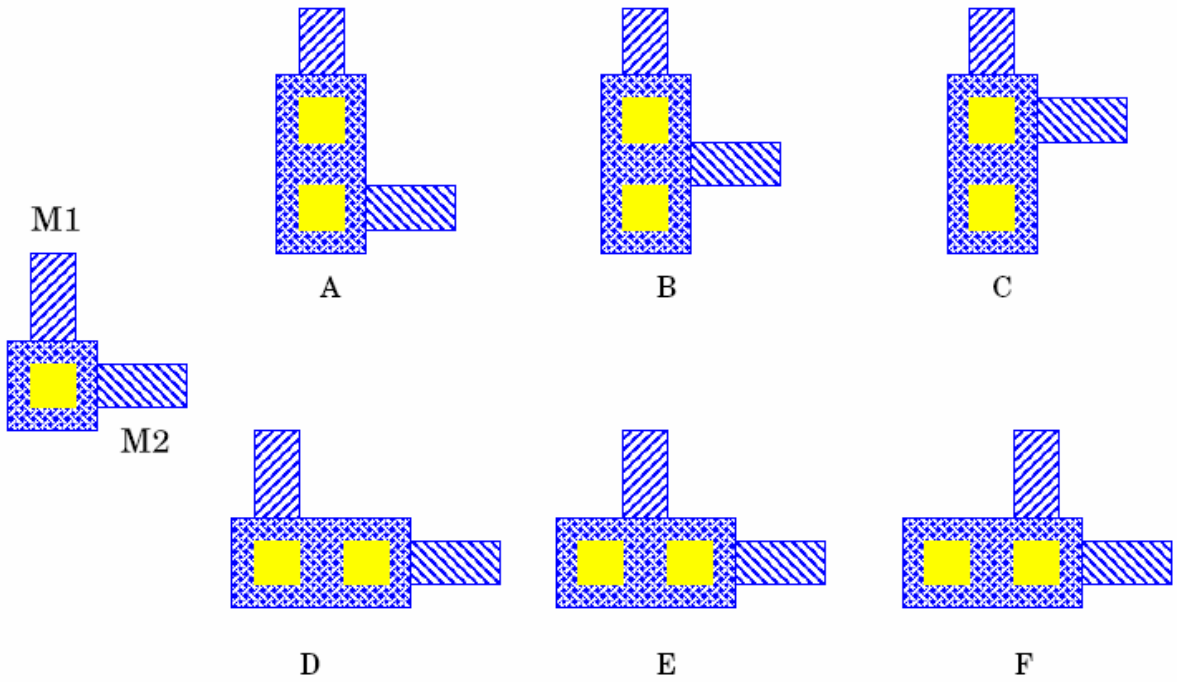
Yield-preferred Via Insertion

- Use yield-preferred via where applicable
  - The more, the better
- Use the most suitable one
  - the one with the most yield benefit

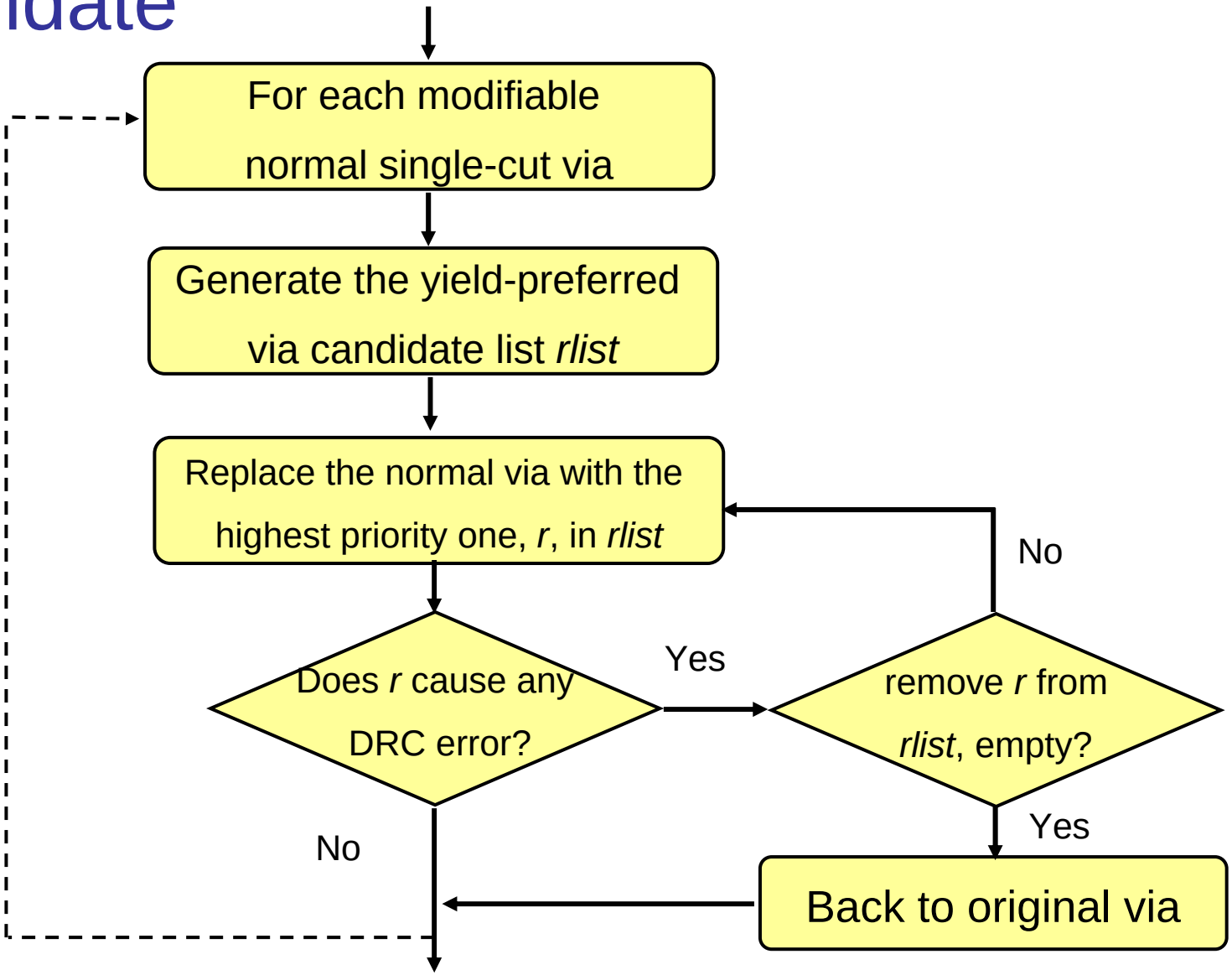


Yield-preferred Via Insertion

- Use the most suitable one
  - The one with the least disturbance to the layout
  - Priority: A > B > C > D > E > F



Choose the Best Yield-preferred Via Candidate



Experiments

Design	routing layers	nets	gates
Case1	2	5k	22k
Case2	3	7.8k	35k
Case3	4	15k	44k
Case4	4	17k	58k
Case5	3	24k	83k
Case6	3	37.8k	285k
Case7	7	64.7k	256k
case8	3	115k	1020k

- 2 P4 2.8G CPUs
- 2G memory
- Linux box

Results

Design	Total vias	Yield-prefferd vias	Insertion rate
Case1	25.1k	24.2k	96.4%
Case2	45k	40.2k	89.3%
Case3	74.7k	68.0k	91.4%
Case4	87.3k	80.8k	92.6%
Case5	149.1k	143.1k	95.95%
Case6	280.1k	251.5k	89.8%
Case7	890.8k	813.2k	91.3%
case8	1146k	1028k	89.7%

Results

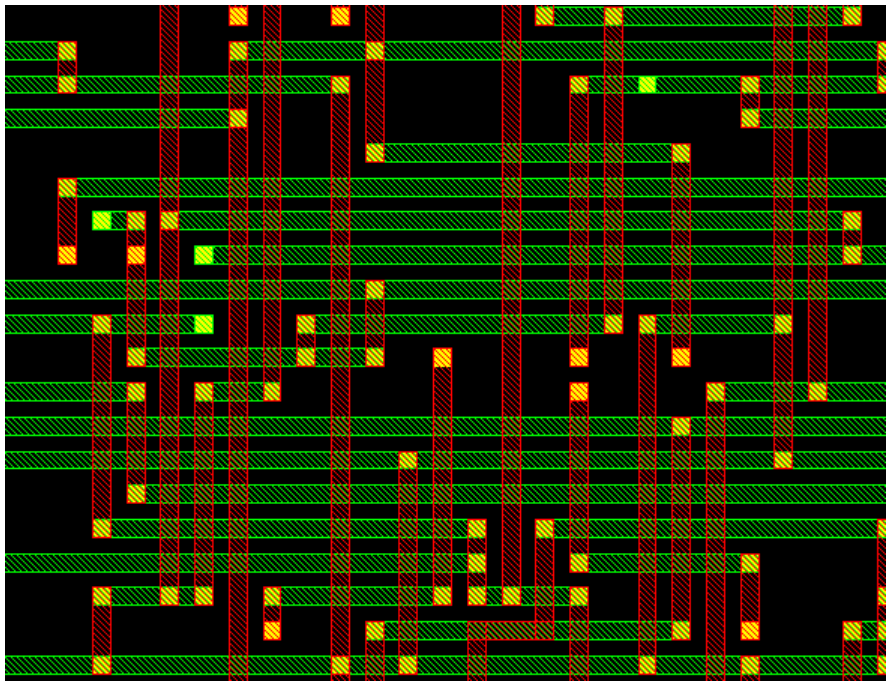
- High insertion rate
  - Over 89% in the most dense design
- Fast
  - Case 8, 1 million gates
  - Total running time is about 1 hour and a half
- Keep the same die size
- Preserve design performace

Comparison with Routers

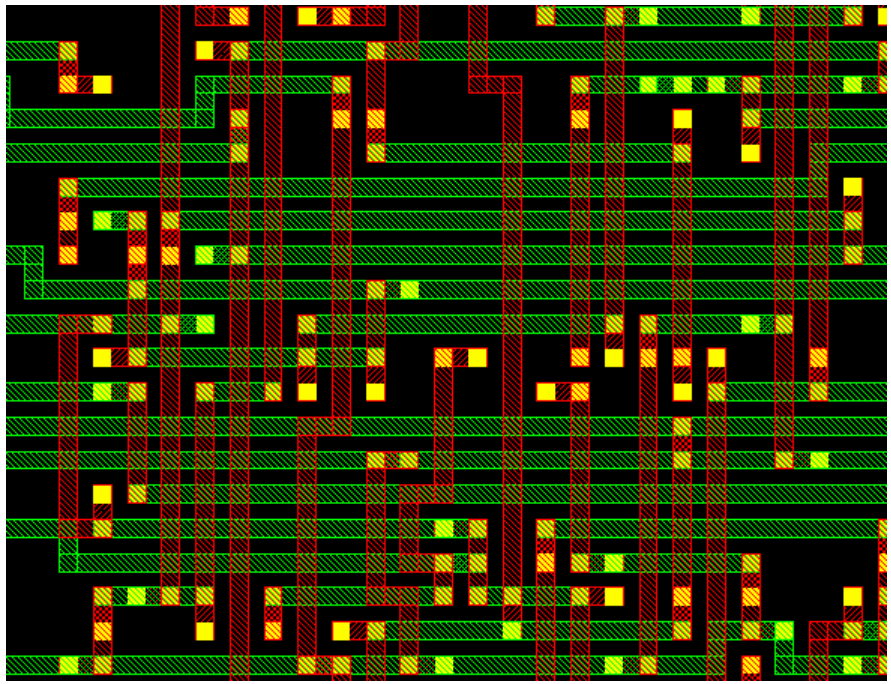
- Case 9
  - One block of industry design, 1.2M gates, 1.2M vias, 8 metal layers
  - 90nm technology
  - 58% redundant cut vias by detail router
- Direct insertion
  - 92k more redundant cut vias, rise to 66%
- Restore and then insert
  - 84% insertion rate

Layout with Yield-preferred Vias

- Case 6, 2 layers shown



Before



After

Thank You