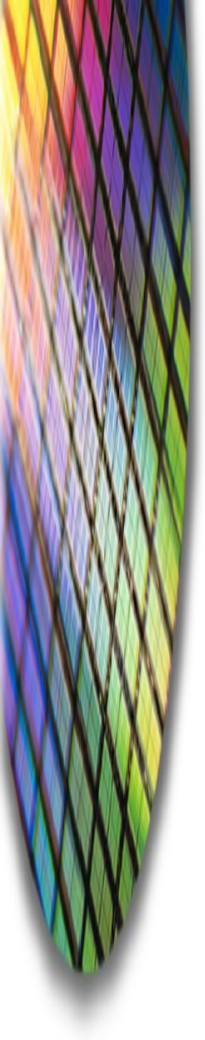

Fast Substrate Noise-Aware Floorplanning with Preference-Directed Graph in Mixed-SOCs

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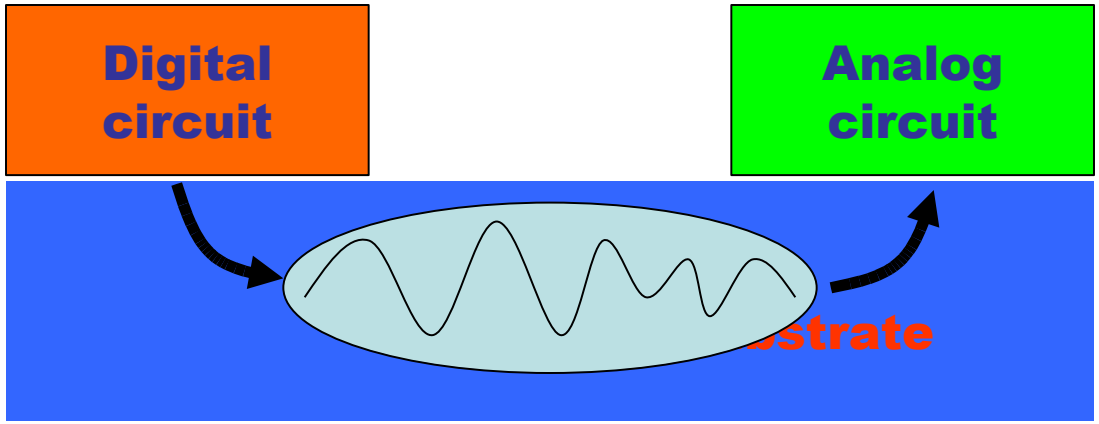
Outline

- Introduction & Previous Works
- Proposed Substrate Noise-Aware Floorplanning
  - Block Preference Directed Graph (BPDG)
  - Sequence Pair with BPDG
- Experimental Results
- Conclusion

Mixed-signal SOC

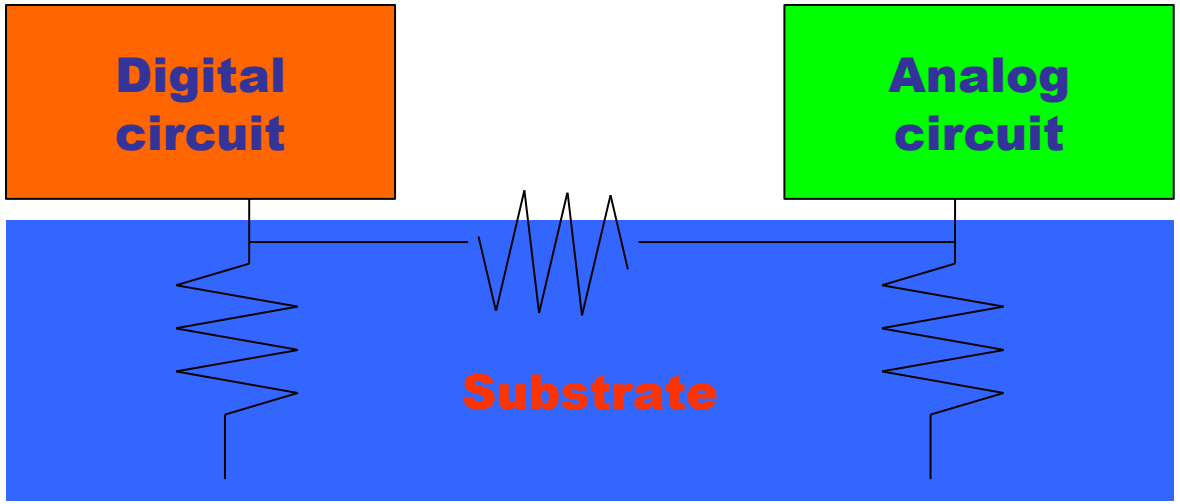
- Mixed-signal SOC - digital and analog circuits on the same substrate
- Becomes more and more popular
  - RF circuit
  - Reduced area, reduced cost and low power
- But, suffers from noise due to high complexity of integration

Substrate Noise Overview



- Substrate noise from digital circuit to analog circuit - the performance of analog circuit is degraded
- Expensive over-design to meet the specs under noisy condition

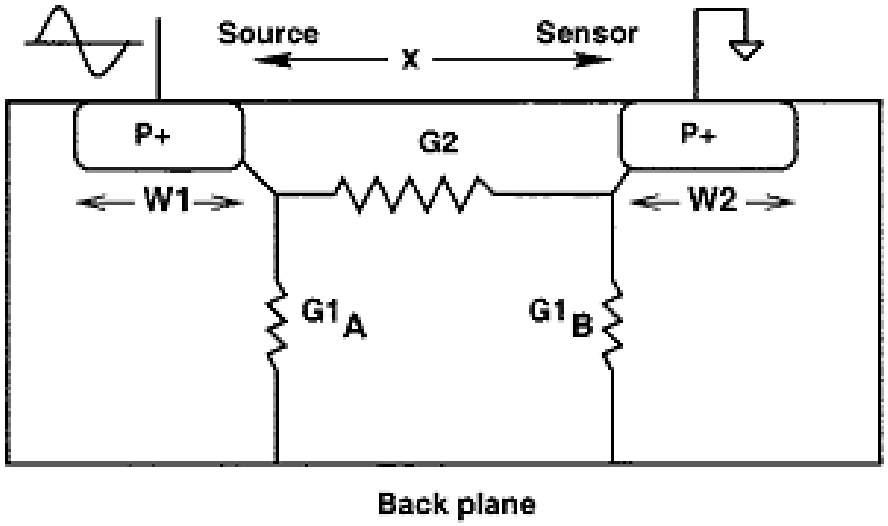
Compact Substrate Noise Model

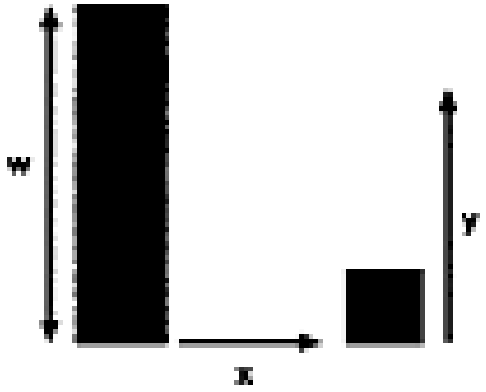


[K. Mayaram et al JSSC05]

- Noise is injected from digital circuit to substrate
- Noise propagates through substrate which can be modeled as resistive network
- Noise affects analog circuit, based on analog circuit's sensitivity to the noise

How to compute SN





$$Z_{11} = \frac{1}{K_1 Area + K_2 Perimeter + K_3}$$

$$Z_{12} = [ay^2 + by + c]\, e^{-\beta(x - x_a)}$$

[K. Mayaram et al JSSC00]
[K. Mayaram et al CICC02]

How to compute SN

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \frac{1}{\triangle} \begin{bmatrix} G_D + G_{DA} & G_{DA} \\ G_{DA} & G_A + G_{DA} \end{bmatrix}$$

$$CG_{i,j} = \frac{R_A}{R_A + R_{DA}} = \frac{G_{DA}}{G_{DA} + G_A} = \frac{Z_{12}}{Z_{22}}$$

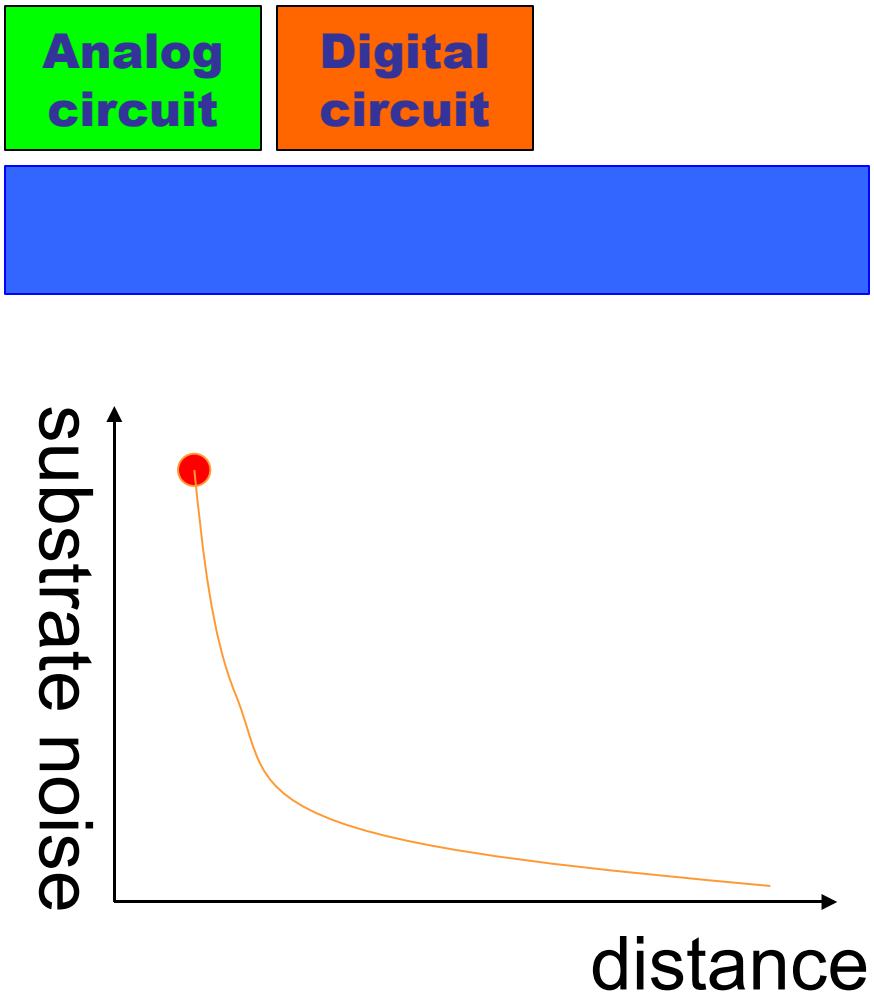
$$N_{i,j} = (CG_{i,j}) \cdot \sqrt{\int_0^\infty (S_i(f) \cdot H_j(f))^2 df}$$

$$N_{total} = \sum_i \sum_j N_{i,j}$$

[K. Mayaram et al CICC02]

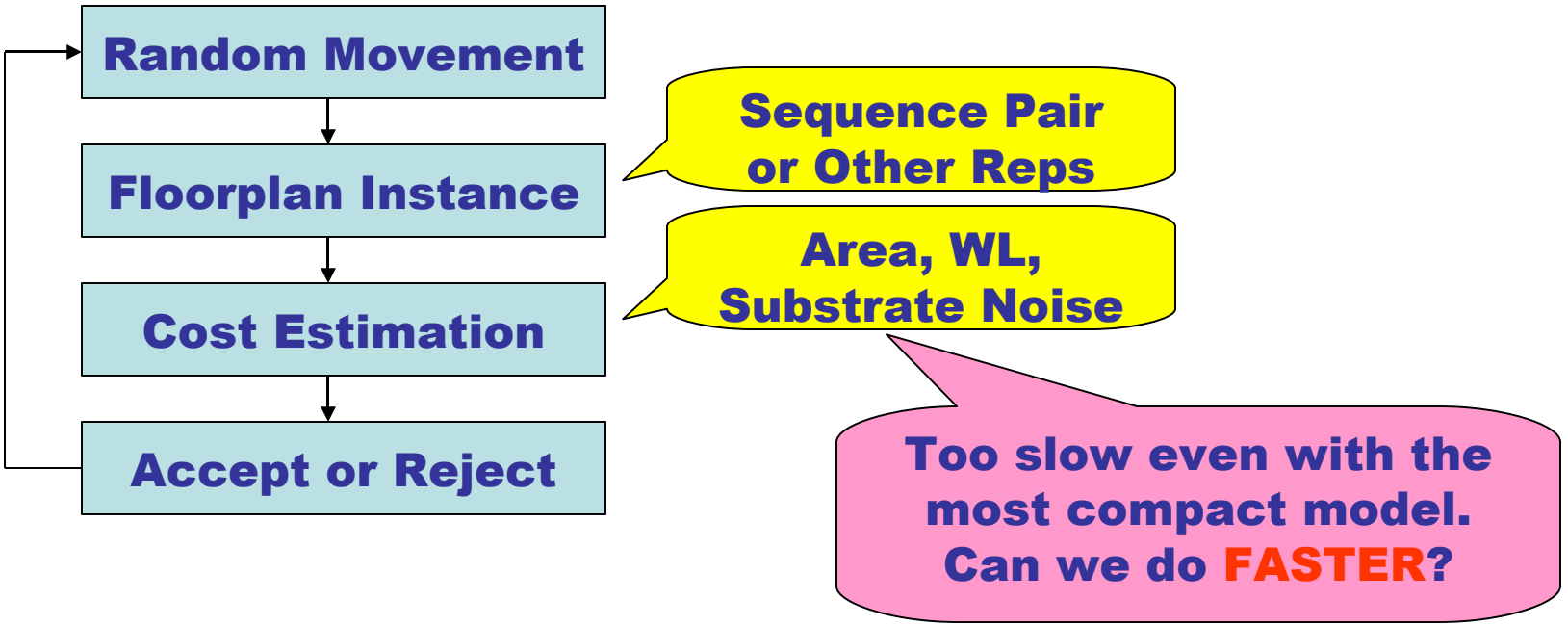
How to optimize Substrate Noise?

- As distance between digital and analog circuit increases, substrate noise decreases exponentially
- Efficient optimization can be done during floorplanning



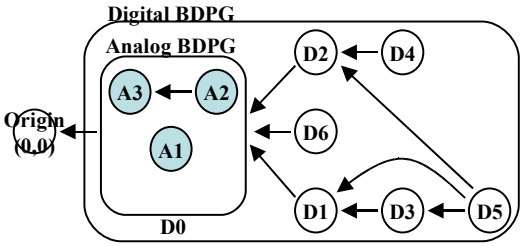
Previous Works

- Placement - Kao (Cadence) et al, ISCAS03
- Floorplanning - G. blakiewicz et al, ASPDAC05



Our Contribution

Block Preference Directed Graph (BPDG)



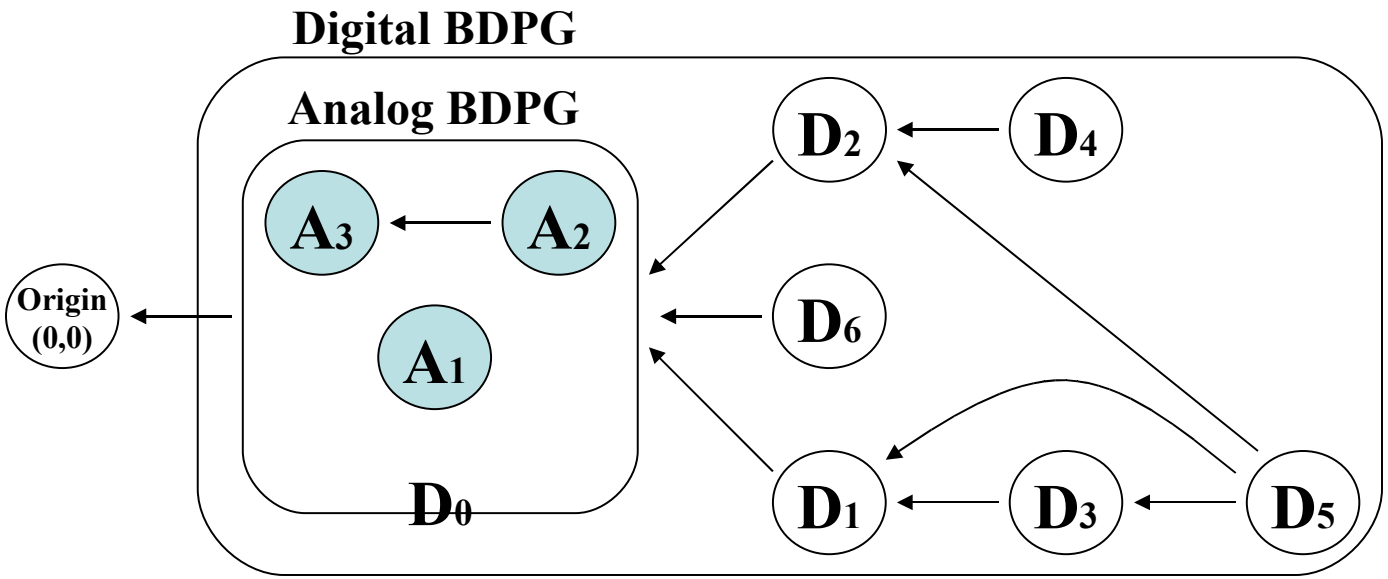
Sequence Pair Instance (D1D2D3D4..., D4D2D1D3...)

Compare

The number of preference violations = the amount of substrate noise

- Fast substrate noise estimation can be done by comparing BPDG and sequence pair

Block Preference Directed Graph



- Block Preference Directed Graph (BPDG) represents preferred relative location of blocks.
- Each edge is corresponding to each preference

BPDG Construction - Table

$$N_{i,j} = (CG_{i,j}) \cdot \sqrt{\int_0^\infty (S_i(f) \cdot H_j(f))^2 df}$$

	D1	D2	D3	D4	D5	D6
A1	5	2	6	3	10	1
A2	2	1	3	10	8	5
A3	3	8	7	11	9	12

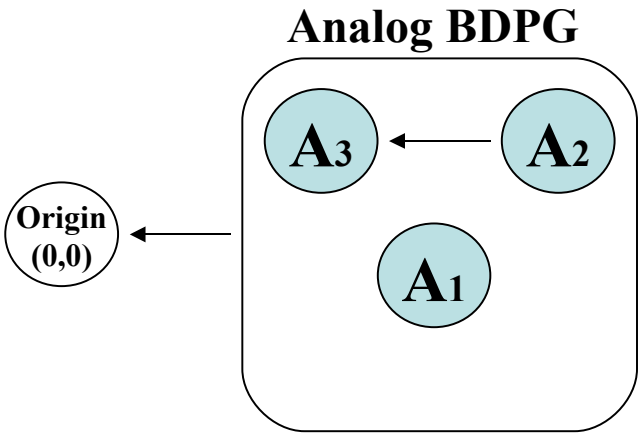
- Calculate the substrate noise for each pair of digital and analog circuit at nominal distance

Analog BPDG

- Analog BPDG
  - Analog ordering
  - Find common orders
  - Build BPDG
- Push the more sensitive analog circuits away from digital circuits

	D1	D2	D3	D4	D5	D6
A1	5	2	6	3	10	1
A2	2	1	3	10	8	5
A3	3	8	7	11	9	12

D1 : A1 ← A3 ← A2 , D2 : A3 ← A1 ← A2
D3 : A3 ← A1 ← A2 , D4 : A3 ← A2 ← A1
D5 : A1 ← A3 ← A2 , D6 : A3 ← A2 ← A1

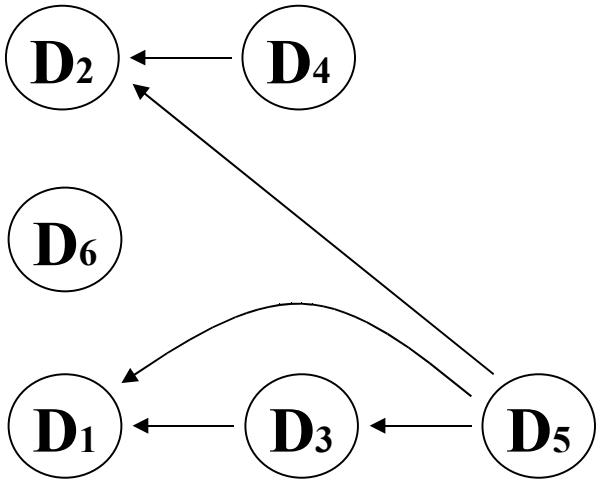


Digital BPDG

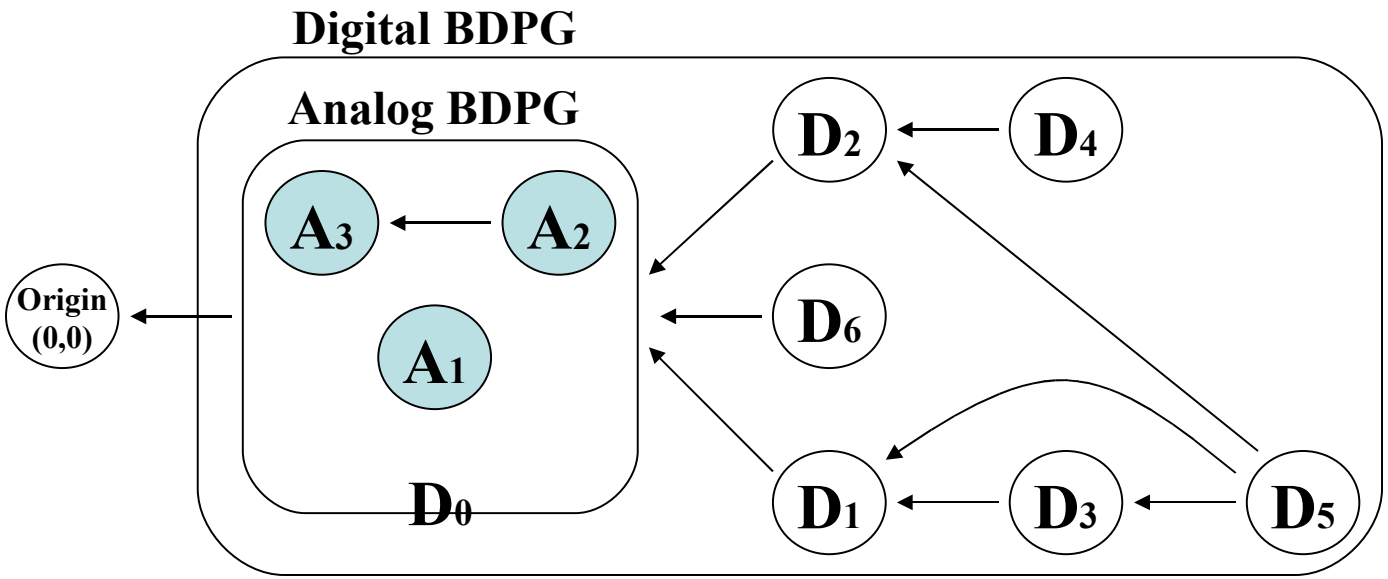
- Digital BPDG
  - Digital ordering
  - Find common orders
  - Build BPDG
- Push the more aggressive digital circuits away from analog circuits

	D1	D2	D3	D4	D5	D6
A1	5	2	6	3	10	1
A2	2	1	3	10	8	5
A3	3	8	7	11	9	12

A1 : D6 ← D2 ← D4 ← D1 ← D3 ← D5
A2 : D2 ← D1 ← D3 ← D6 ← D5 ← D4
A3 : D1 ← D3 ← D2 ← D5 ← D4 ← D6



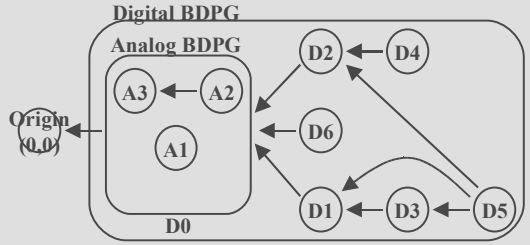
Final BDPG



- Analog BPDG becomes a virtual digital block to force analog blocks get together

Proposed Substrate Noise Aware F-planning

Pre-computed Block Preference Directed Graph (BPDG)



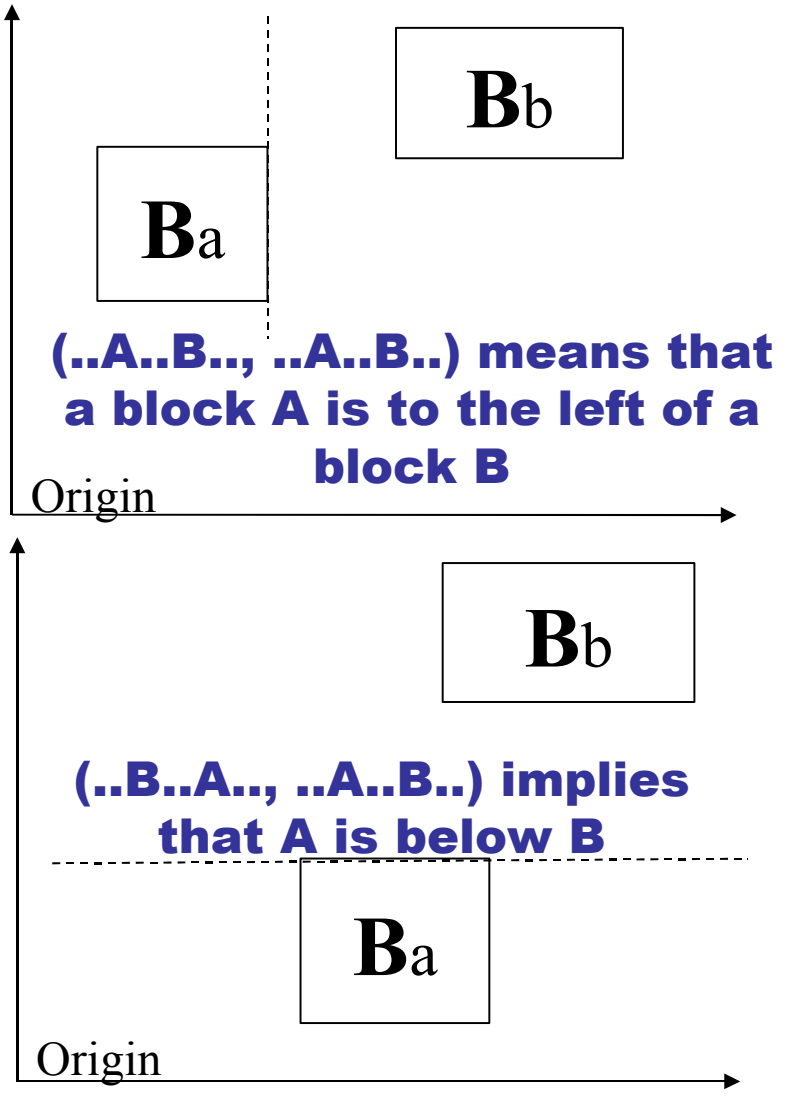
Sequence Pair Instance (D1D2D3D4..., D4D2D1D3...)

Compare

The number of preference violations = the amount of substrate noise

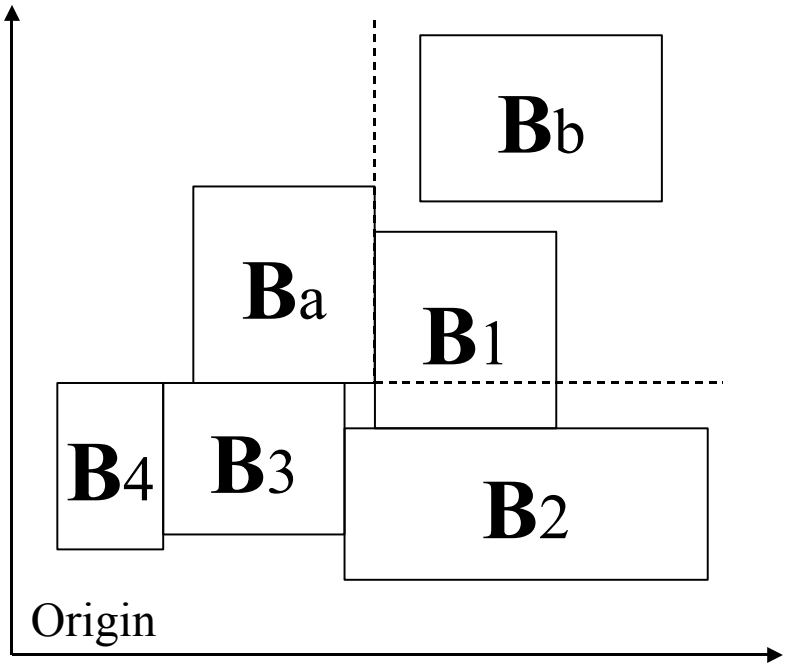
Sequence Pair

- Murata et al, TCAD96
- One of the most popular floorplan representations
- A pair of sequences of n elements representing a list of n blocks, specifying the geometric relations between each pair of blocks.



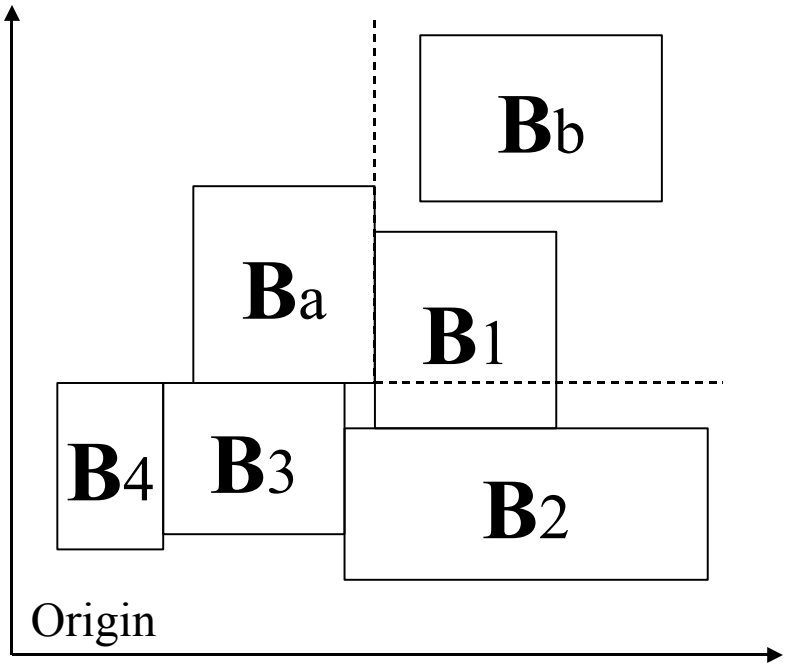
Seq. Pair – Strictly ahead

- *Strictly ahead* – when there is no block between two blocks.
  - Ba is strictly ahead of B1,B2,B3 and B4.
  - Longest common string (LCS) can be used to test *strictly ahead* condition [Tang and Wong DAC02]
  - strictly ahead is a necessary condition for two to be abutted (only B1 and B3 are abutted to Ba).

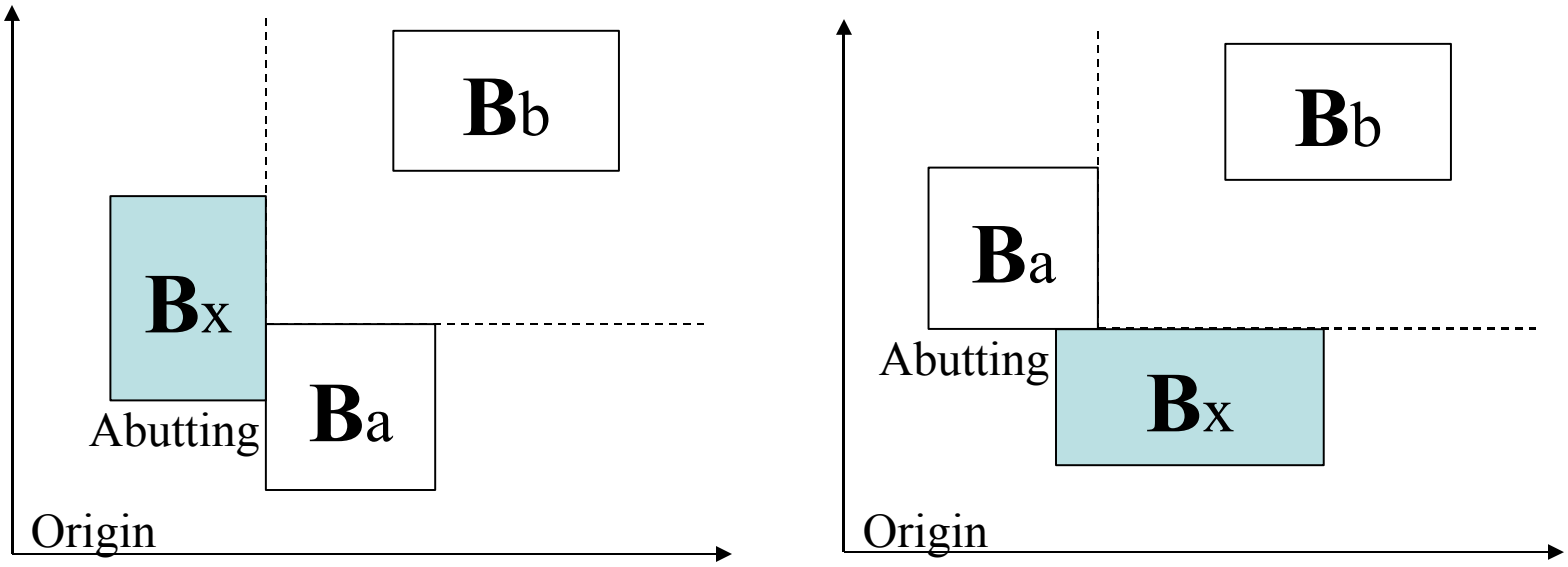


Seq. Pair – Reference Block

- B2,B3 and B4 are **strictly below set** of Ba, because they are strictly ahead of Ba as well as below Ba.
- B3 is **a reference block** of Ba, as it is in the **strictly below set** of Ba and abutting to Ba.



Sequence Pair with BPDG

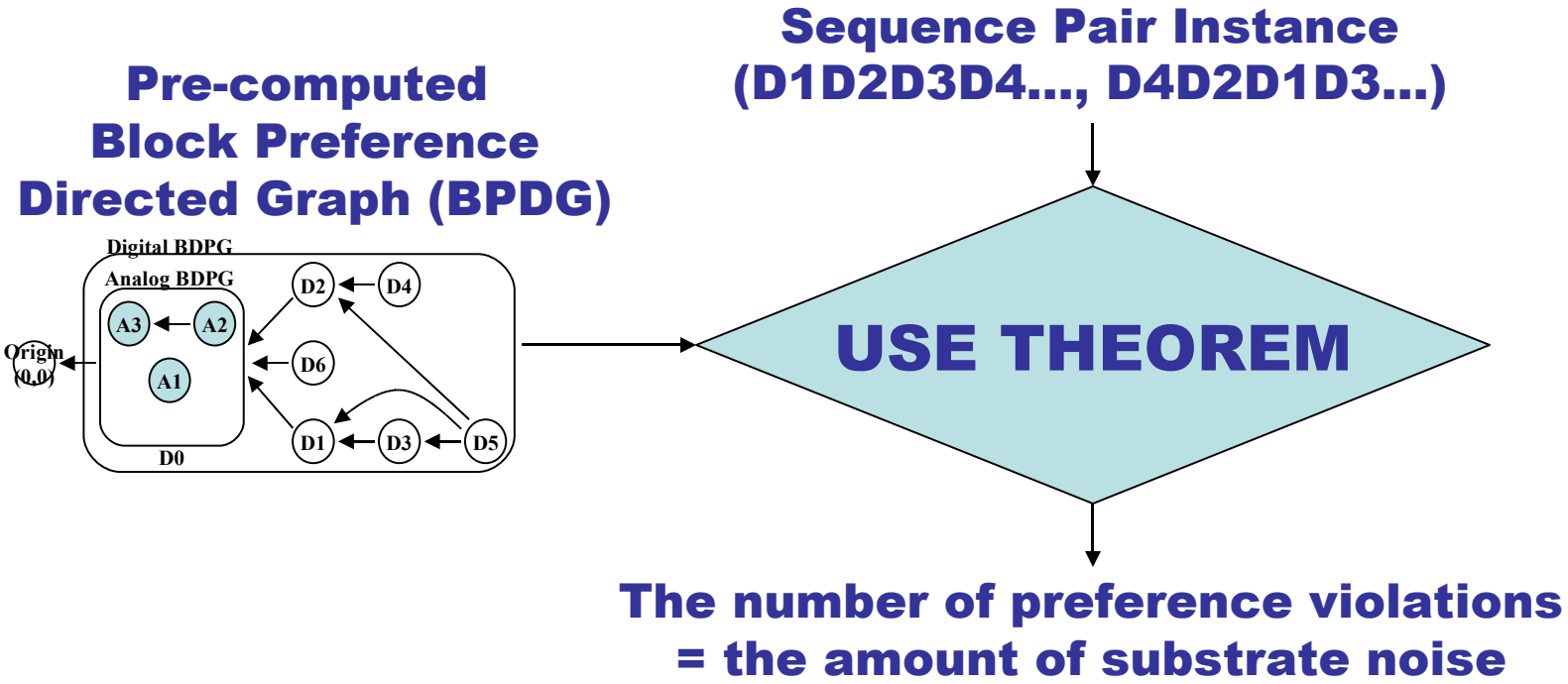


- Fast substrate noise estimation with BPDG
- Bitwiase-OR can be used, instead of LCS

Theorem for Seq. Pair and BPDG

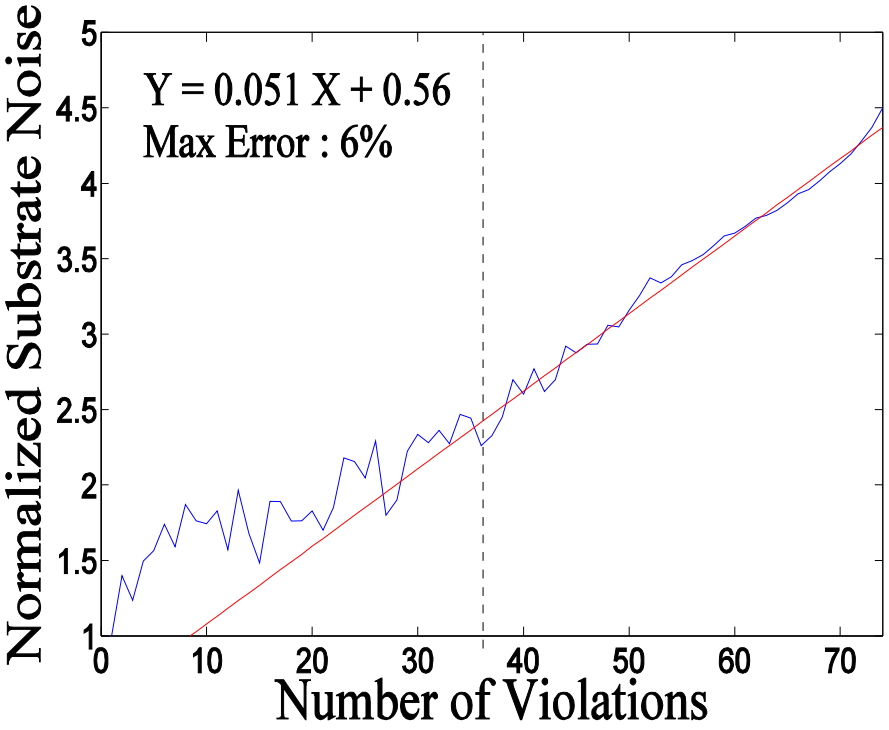
- Let Sb be a strictly below set of Ba and Sl a strictly left set of Ba. A block Ba is guaranteed to have shorter distance to the left bottom corner than a block Bb under a completely packed floorplan, if either of following conditions is satisfied.
- Theorem 1:
  - For any block Bs in Sb,a sequence pair (P,N) is (..BaX1BbX2Bs..,..BsY1Ba..Bb..).
  - For any block Bs in Sl, a sequence pair (P,N) is (..BsX3BbX4Ba..,..BsY2Ba..Bb..).
- Theorem 2:
  - there is no block Bs satisfying LCS(X1, Y1)=φ in a sequence pair (P,N)=(..BaX1Bs..Bb..,..BsY1Ba..Bb..).
  - there is no block Bs satisfying LCS(X2, Y2)=φ in a sequence pair (P,N)=(..Bb..BsX2Ba..,..BsY2Ba..Bb..).

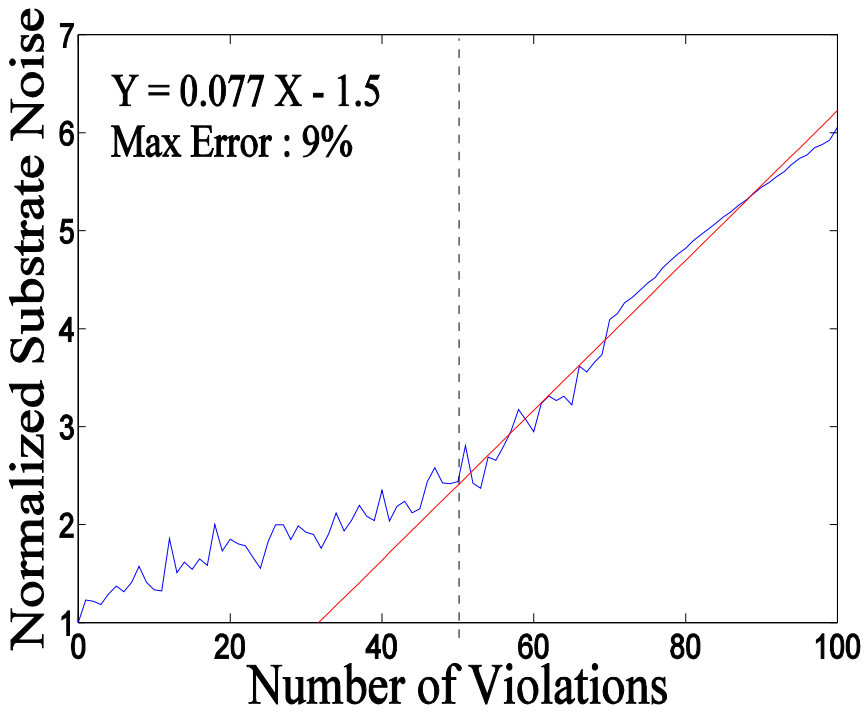
BPDG based SN Estimation



- Each edge in the BPDG can be checked by the proposed theorem
- The number of preference violations can be translated into substrate noise

Fidelity of BPDG SN Estimation





- High Fidelity to substrate noise by the number of violations is observed

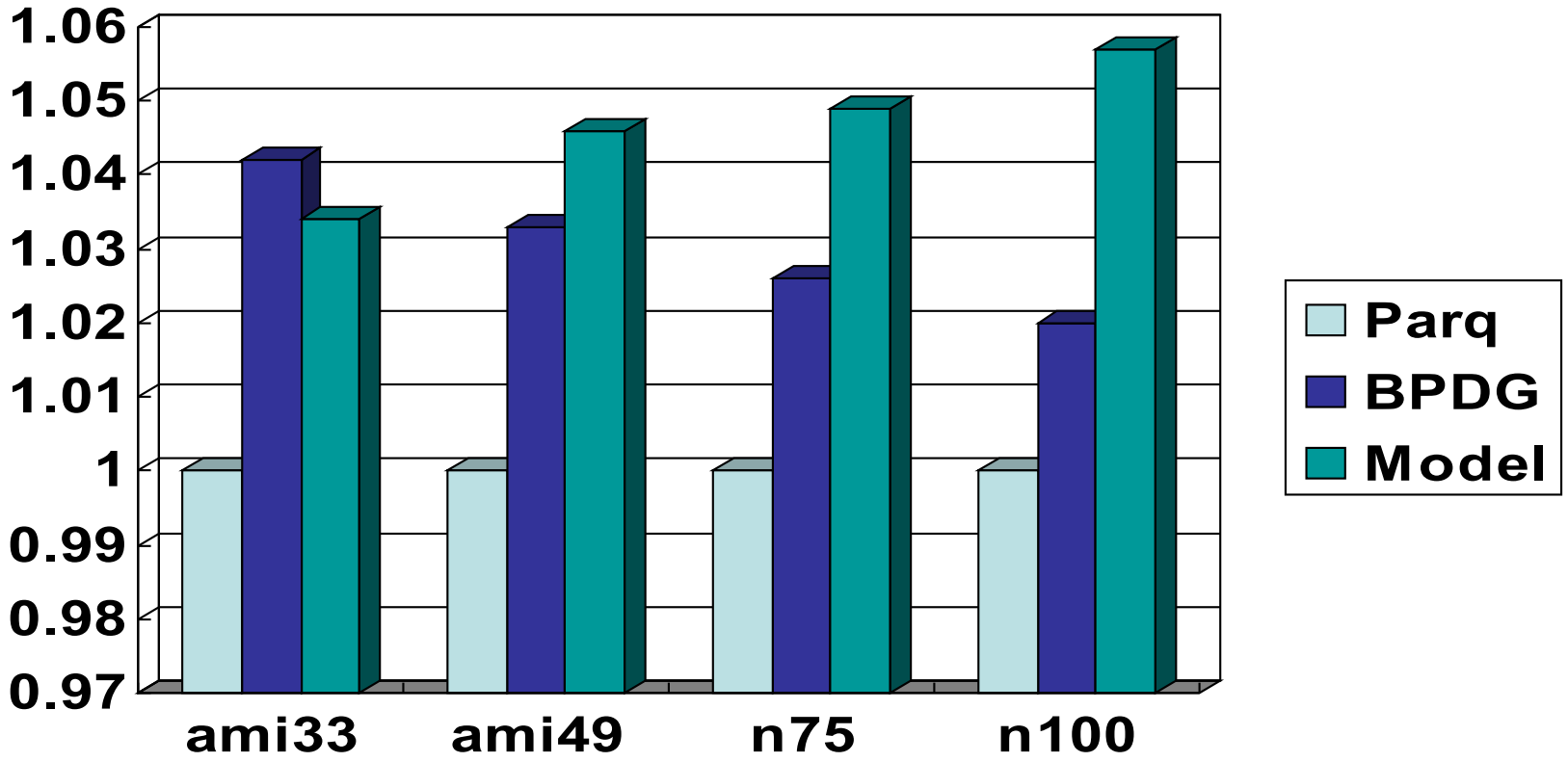
Overall Floorplanning

- Create Analog BPDG *Ag*, Digital BPDG *Dg*
- Do floorplanning with analog blocks with *Ag*
- Inflate the analog block floorplan
- Make the analog floorplan as a virtual block *Bv*
- Do floorplanning with digital blocks and *Bv* with *Dg*

Experimental Setup

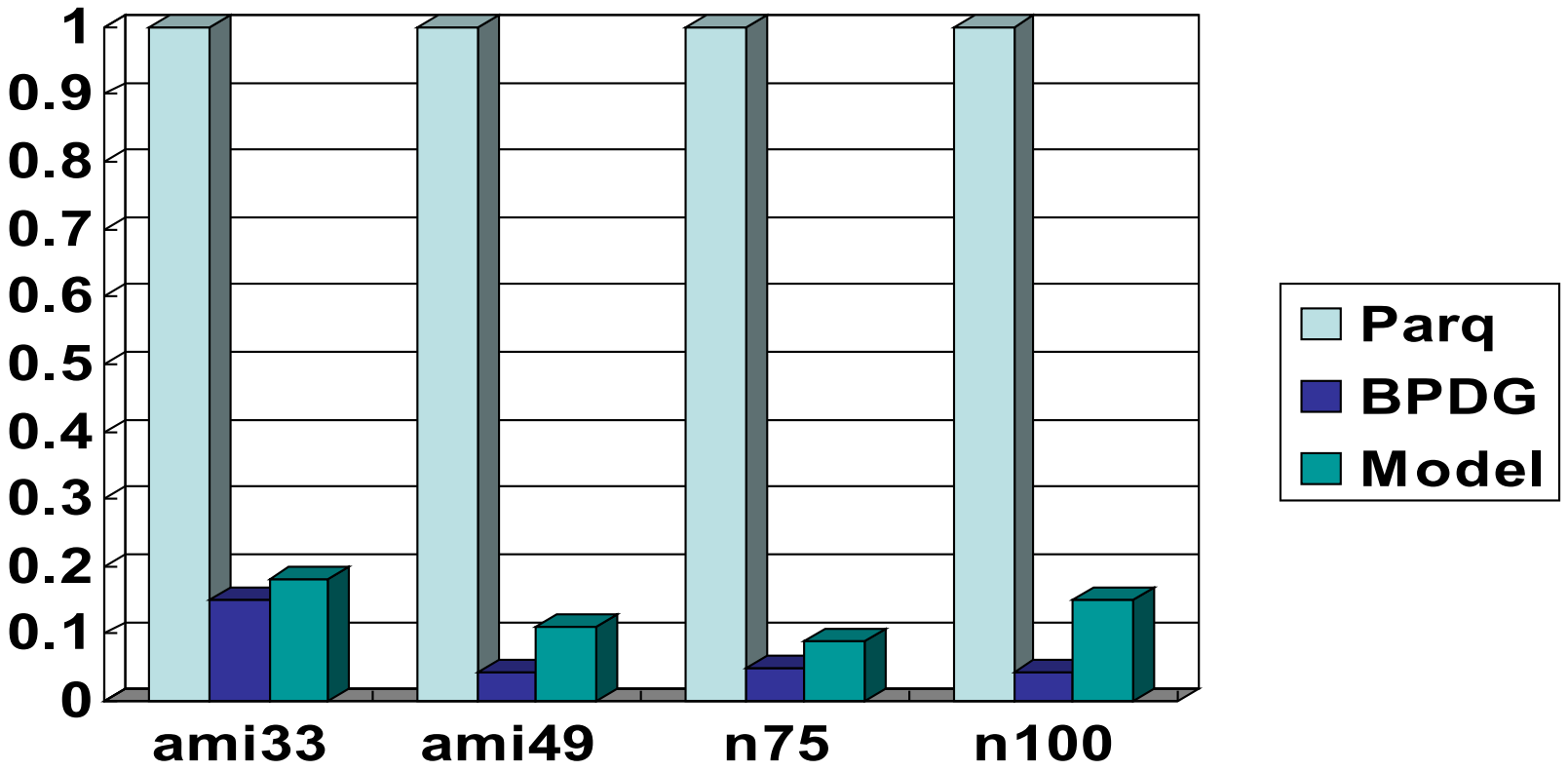
- MCNC benchmarks are carefully modified for analog blocks
- Parquet floorplanner is used [Adya and Markov TVLSI03]
  - Cost function is modified for substrate noise estimation
- Comparison algorithms
  - Parq – Pure parquet with Sequence Pair
  - BPDG – BPDG with Sequence Pair
  - Model – Model with Sequence Pair

Area Comparison



- Small area overhead for substrate noise-aware floorplannings

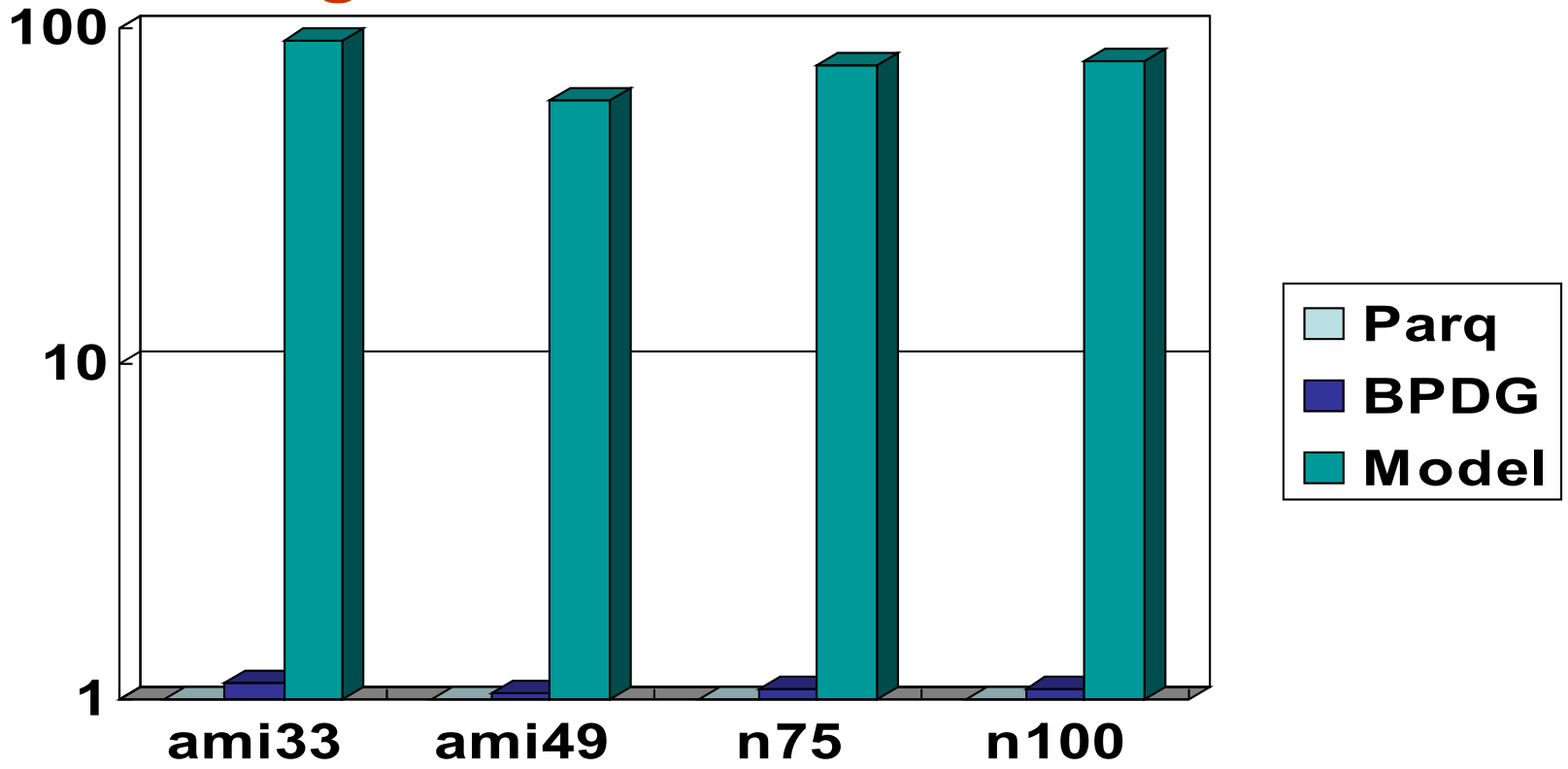
Noise Comparison



- Effective substrate noise reduction in both substrate noise-aware floorplannings (BPDG, Model)

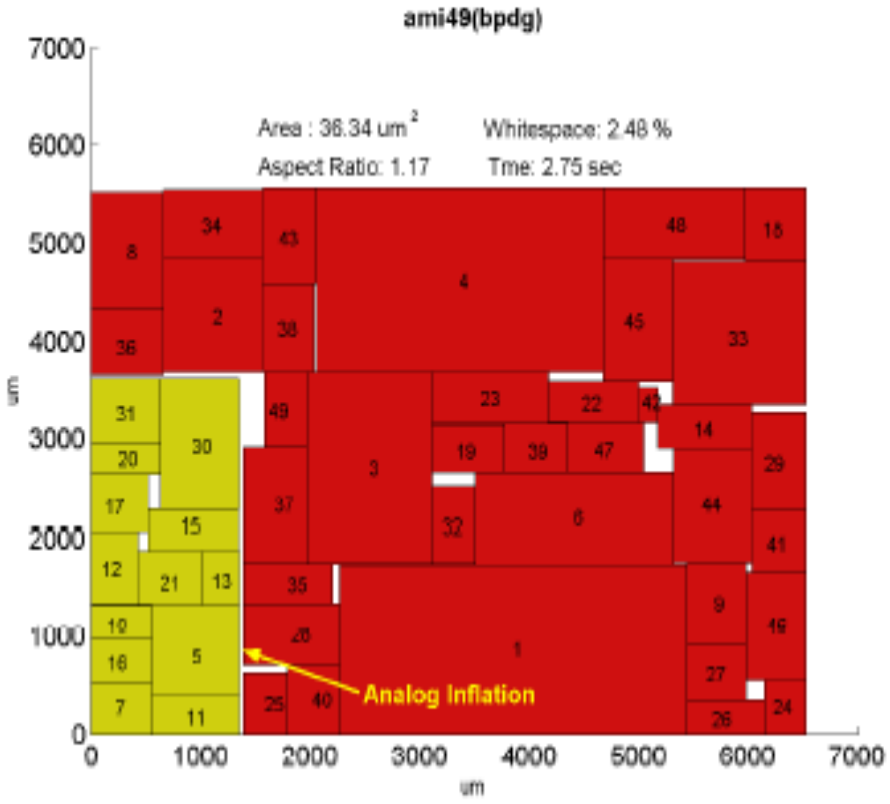
Runtime Comparison

Y axis in log scale

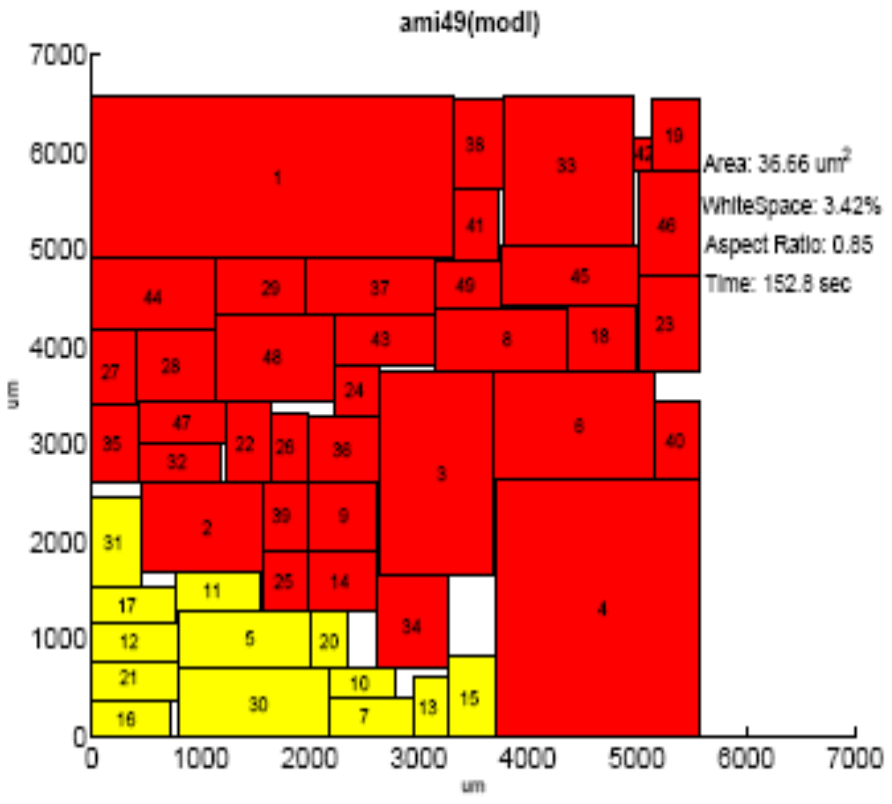


- Significant speed-up in substrate noise-aware floorplanning based on BPDG & Sequence Pair

Floorplan Example



(a) With proposed approach(bpdg)



(b) With model-based simulation approach(modl)

Conclusion

- Substrate noise is a critical issue in mixed-signal SOCs
- Novel concept of BPDG combined with Sequence Pair for ultra-fast substrate noise estimation with high fidelity
- The model can be effectively used during SN-aware floorplanning for mixed-signal SOC designs (over 60x speed-up)