A Fixed-die Floorplanning Algorithm Using an Analytical Approach

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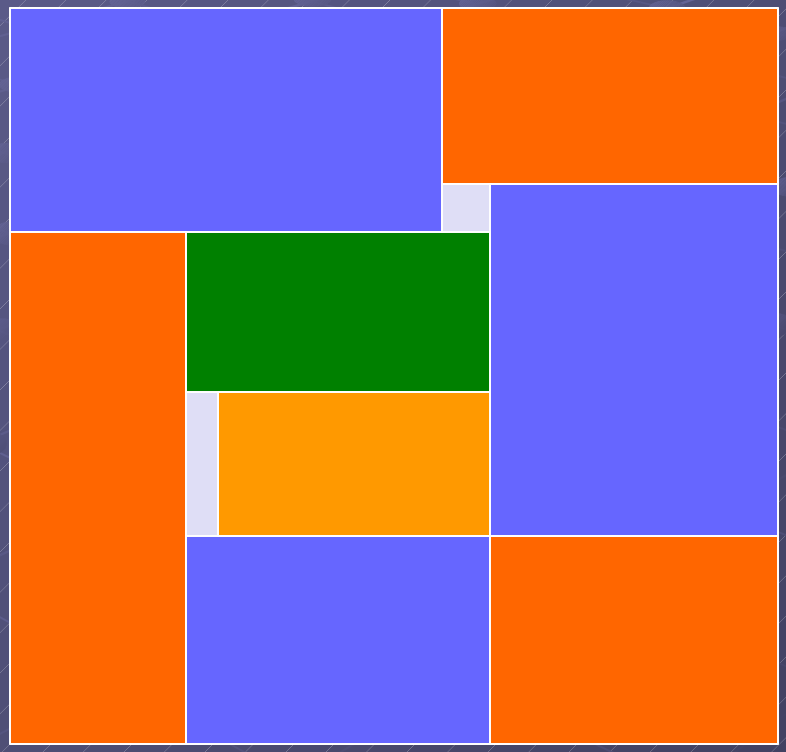
Outline

- Background
- Problem formulation
- An analytical fixed-die floorplanning algorithm
- Experimental results
- Conclusions

Fixed-die Floorplanning Problem



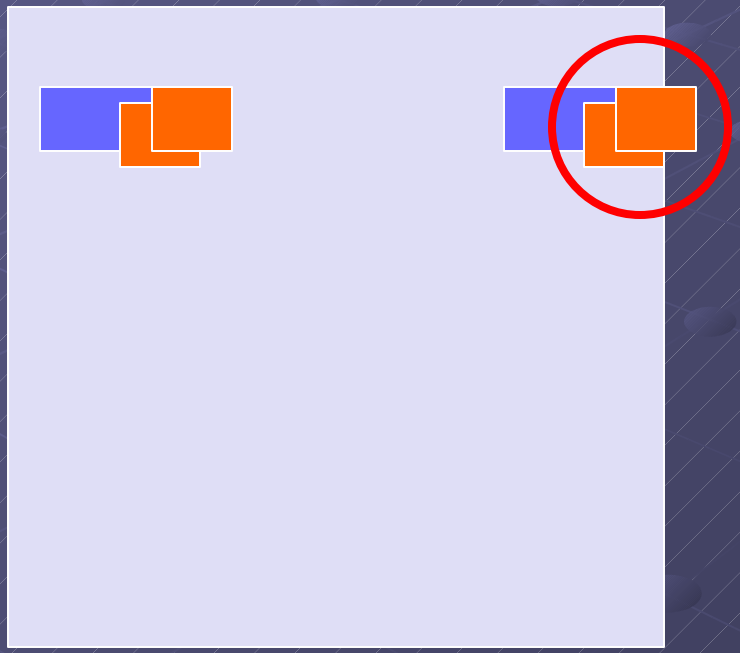
- Fixed outline
- Place and size the modules such that there is no overlap
- Minimize some delay metric, e.g., wire length

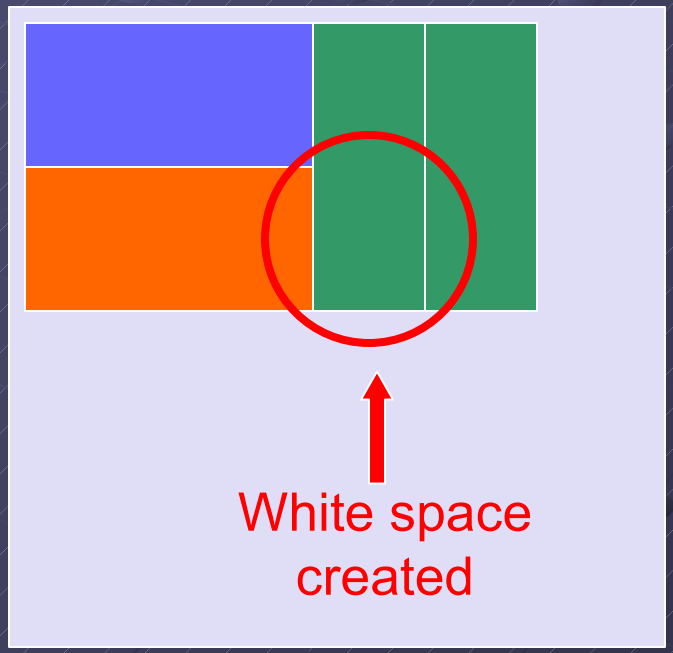
Previous Works

- Simulated annealing based approach
  - Adya and Markov, Trans. VLSI 2003
  - Chen and Chang, ISPD 2005
- Partition based approach
  - Cong, Romesis, and Shinnerl, ASPDAC 2005
- Analytical approach
  - Kahng and Wang, ISPD 2004 (Placement)

Difference between Placement and Floorplanning

- Significant difference in module width and height
- Large module size





Problem Formulation

Die Size L_x , L_y , Area and Max Aspect Ratio A_i , R_i

Connectivity between Modules

Analytical Floorplanner

An Overlap Free Floorplan that Minimizes the Total Wire Length

Overall Floorplanning Procedure

- Rough floorplanning to spread modules uniformly with good control of total wire length (ref: Kahng and Wang, ISPD 2004)
- Optimization based overlap reduction and final legalization

Rough Floorplanning

Total Wire Length

Penalty for Non-Uniform Module Spreading

$$\min \quad WL + \alpha \cdot P_D$$

$$\text{such that} \quad 0 \le x_i \le L_x$$

$$0 \le y_i \le L_y$$

Module Location Constraints

Module Aspect Ratio Constraints

$$\sqrt{\frac{A_i}{R_i}} \le w_i \le \sqrt{A_i R_i}$$

$$i = 1,2,\ldots,n$$

Transformation to the Unconstrained Optimization Problem

$$\begin{aligned} \min \quad & WL + \alpha \cdot P_D \\ \text{such that} \quad & 0 \le x_i \le L_x \\ & 0 \le y_i \le L_y \\ & \sqrt{\frac{A_i}{R_i}} \le w_i \le \sqrt{A_i R_i} \\ & i = 1,2,\ldots,n \end{aligned}$$

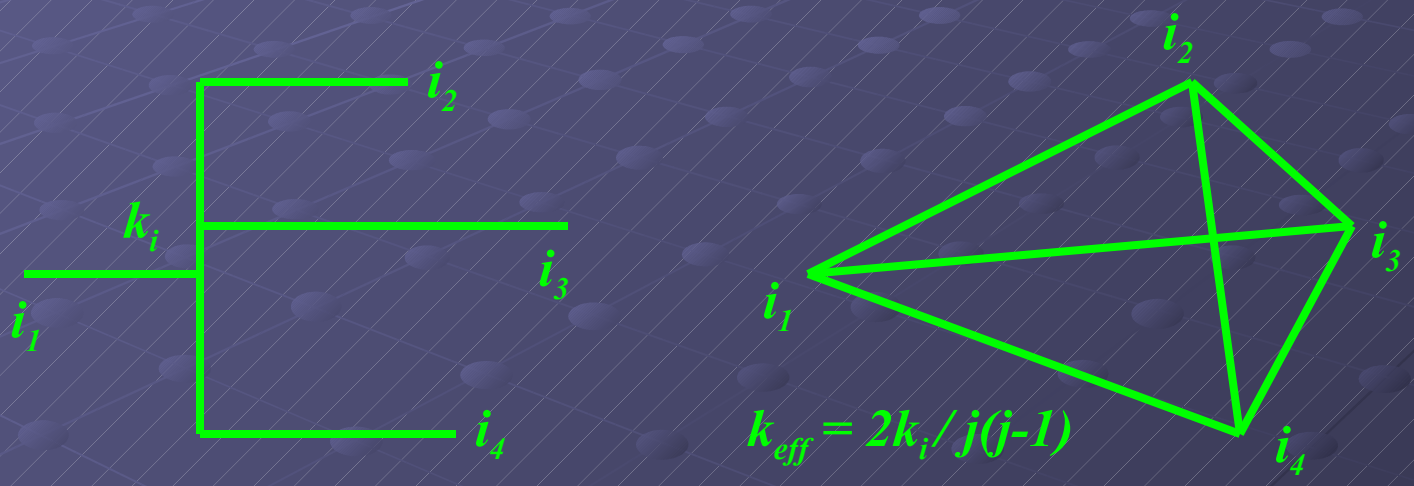
$$\min \quad WL + \alpha \cdot P_D + \beta \cdot B$$

Barrier Term

$$B = \sum_{i=1}^{n} \frac{1}{x_i} + \sum_{i=1}^{n} \frac{1}{L_x - x_i} + \sum_{i=1}^{n} \frac{1}{y_i} + \sum_{i=1}^{n} \frac{1}{L_y - y_i} + \sum_{i=1}^{n} \frac{1}{w_i - \sqrt{A_i / R_i}} + \sum_{i=1}^{n} \frac{1}{\sqrt{A_i R_i} - w_i}$$

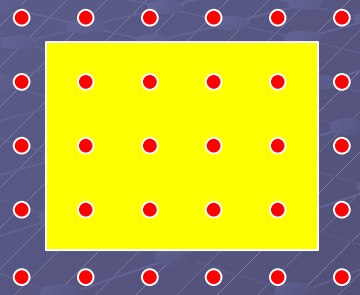
Calculation of the Total Wire Length

- Clique model and quadratic wire length



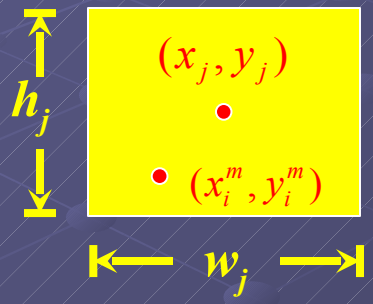
$$WL = \sum_{i,j} k_{ij}[(x_i - x_j)^2 + (y_i - y_j)^2]$$

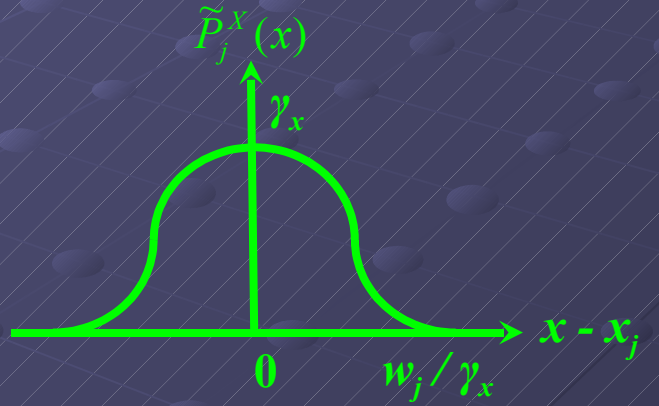
Calculation of the Module Spreading Term



$$P_D = \sum_{i \in C_{in}} (D_i - \overline{D})^2 + \sum_{i \in C_{out}} D_i^2$$

$$\overline{D} = (\sum_{i=1}^{n} A_i)/(L_x L_y) \qquad D_i = \sum_{j=1}^{n} \widetilde{P}_j(x_i^m, y_i^m)$$





$$\widetilde{P}_j(x,y) = \widetilde{P}_j^X(x) \times \widetilde{P}_j^Y(y)$$

Kahng and Wang, ISPD 2004

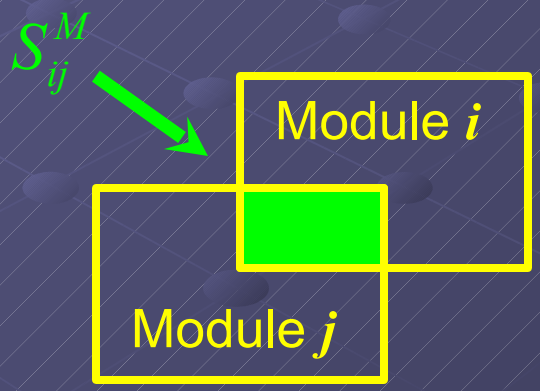
$$\widetilde{P}_j^X(x) = \begin{cases} \gamma_x \times \left(1 - \dfrac{2(x - x_j)^2}{(w_j/\gamma_x)^2}\right) & \text{if } 0 \le |x - x_j| \le w_j/2\gamma_x \\ \gamma_x \times \dfrac{2(|x - x_j| - w_j/\gamma_x)^2}{(w_j/\gamma_x)^2} & \text{if } w_j/2\gamma_x \le |x - x_j| \le w_j/\gamma_x \end{cases}$$

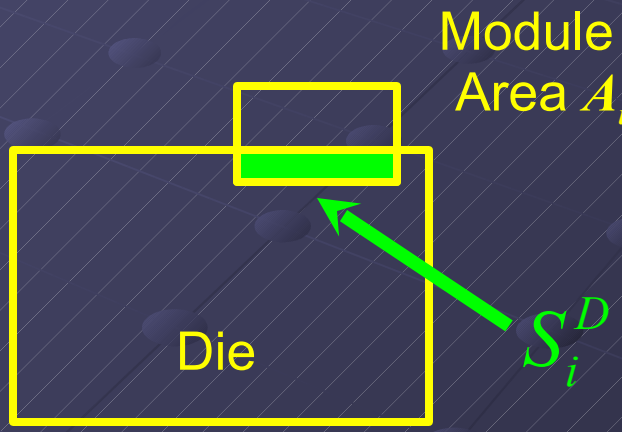
Overlap Reduction

$$\min \quad WL + \eta \cdot P_O + \beta \cdot B$$

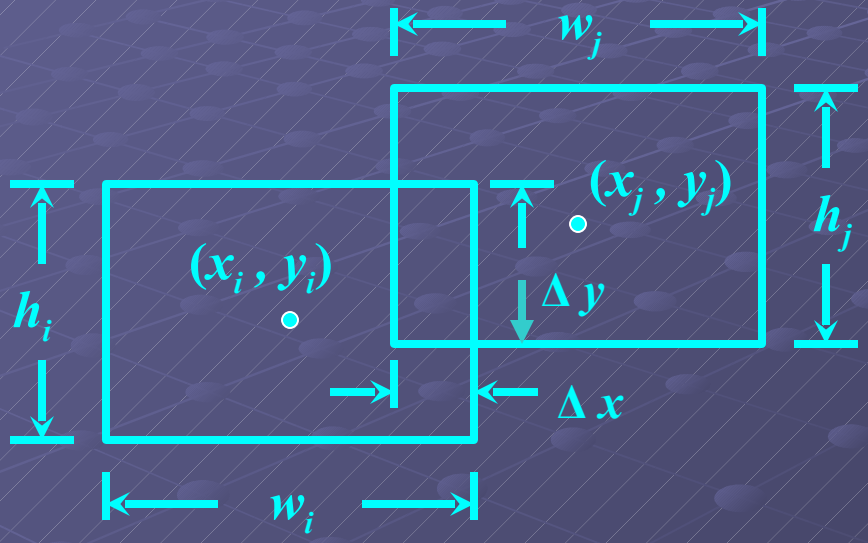
Total Wire Length | Overlap Penalty | Barrier Term

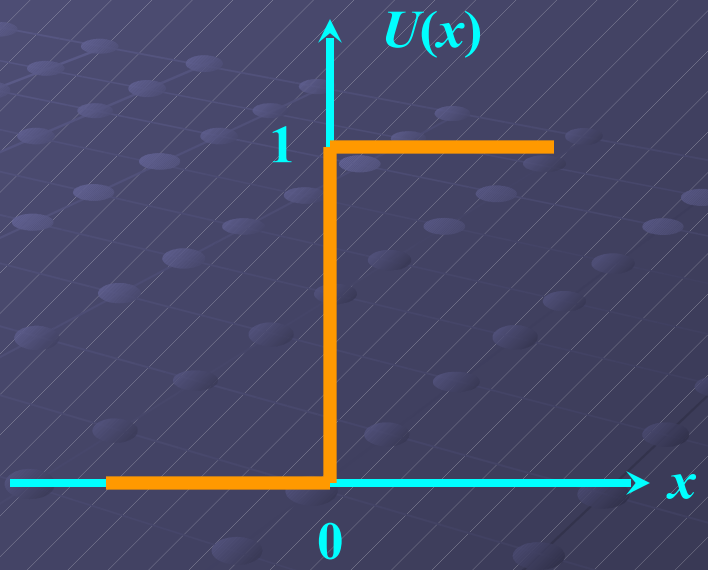
$$P_O = \sum_{i=1}^{n-1} \sum_{j=i+1}^{n} S_{ij}^{M} + \sum_{i=1}^{n} (A_i - S_i^{D})$$





Calculation of the Overlap Area

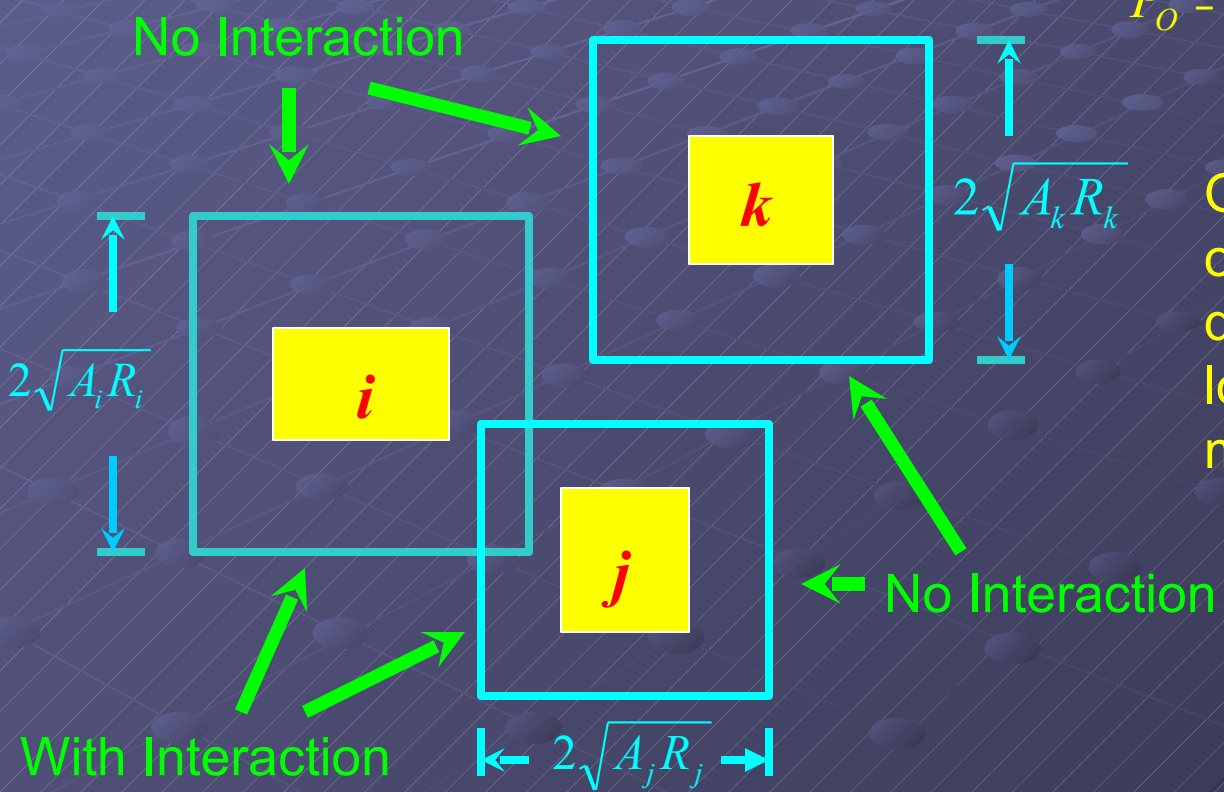




$$\Delta x = (\min\{x_i + 0.5w_i, x_j + 0.5w_j\} - \max\{x_i - 0.5w_i, x_j - 0.5w_j\})$$
$$\times\, U(\min\{x_i + 0.5w_i, x_j + 0.5w_j\} - \max\{x_i - 0.5w_i, x_j - 0.5w_j\})$$

$$\min\{x, y\} \approx \frac{x \cdot e^{k(y-x)} + y \cdot e^{k(x-y)}}{e^{k(x-y)} + e^{k(y-x)}}, \quad \max\{x, y\} \approx \frac{x \cdot e^{k(x-y)} + y \cdot e^{k(y-x)}}{e^{k(x-y)} + e^{k(y-x)}}, \quad U(x) \approx \frac{1}{2}(1 + \tanh(k'x))$$

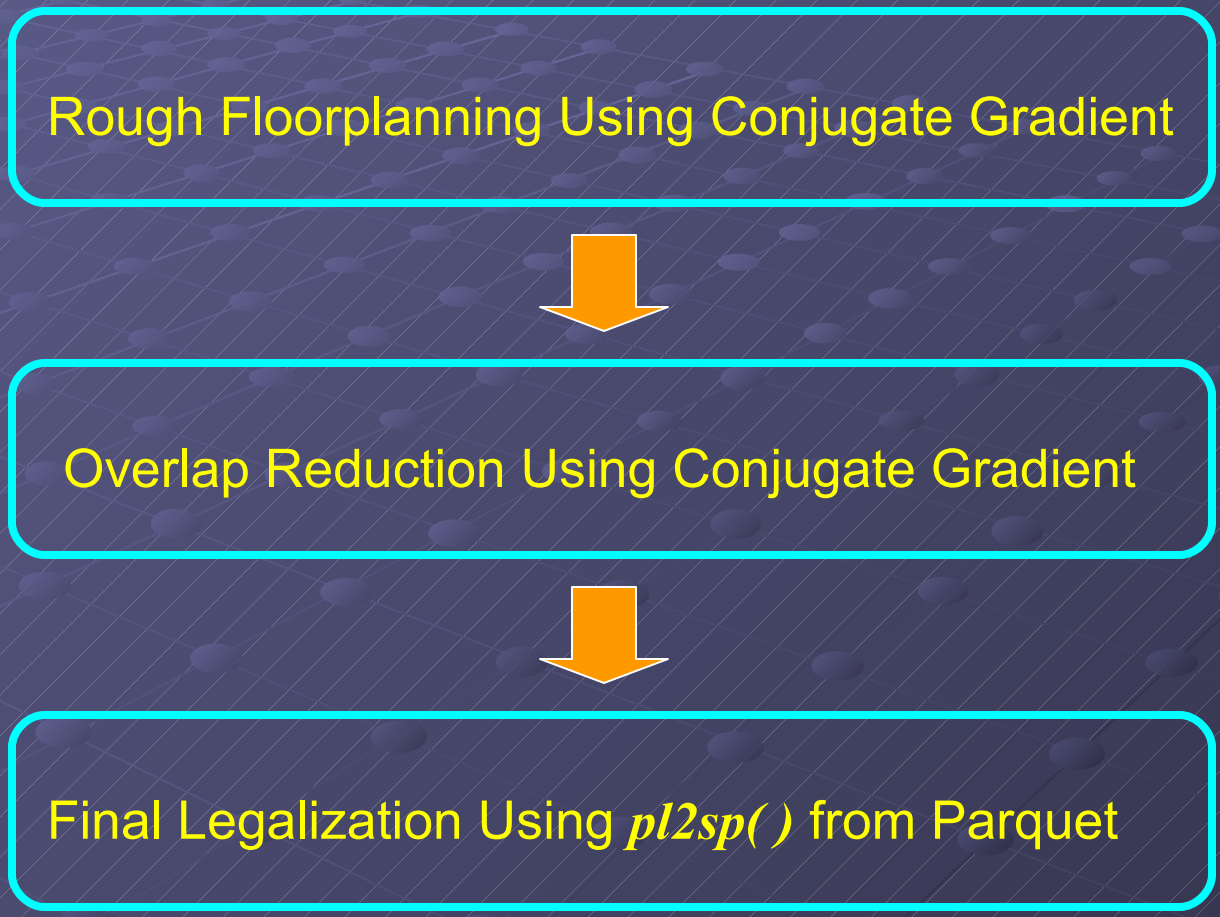
A Useful Heuristic



$$P_O = \sum_{i=1}^{n-1} \sum_{j=i+1}^{n} S_{ij}^M + \sum_{i=1}^{n} (A_i - S_i^D)$$

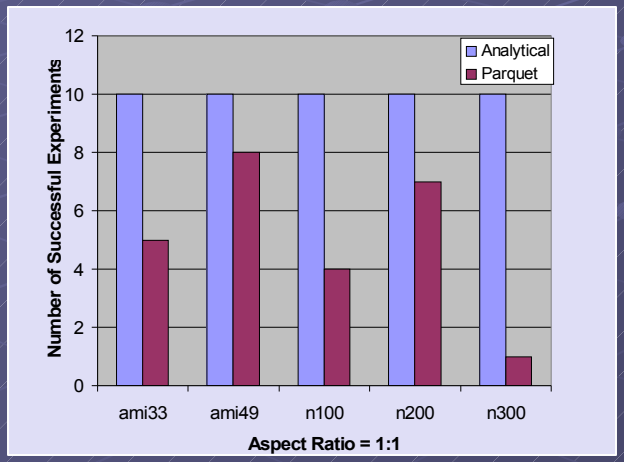
Observation: The overlap reduction step does not change the locations of the modules significantly

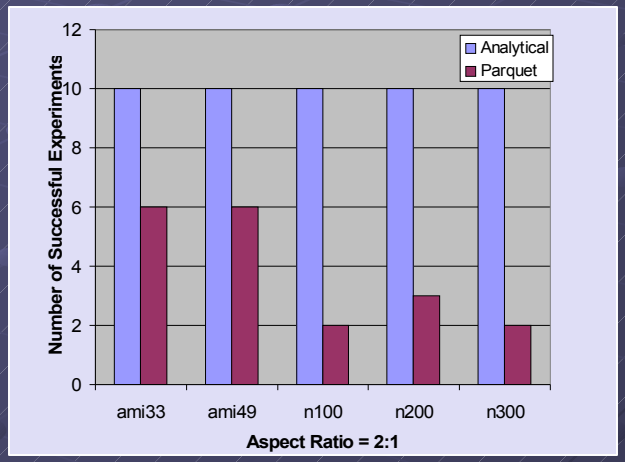
Overall Procedure

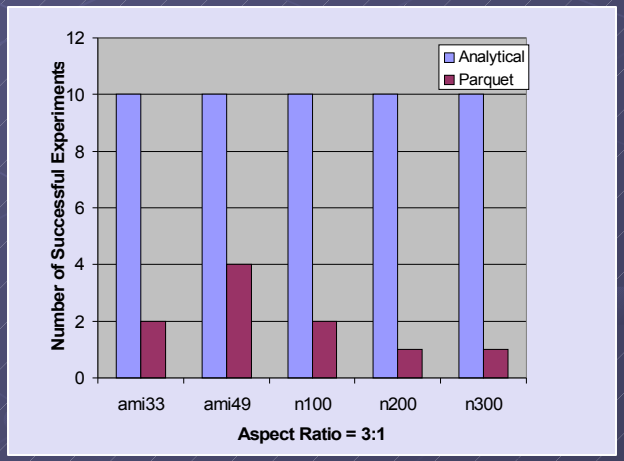


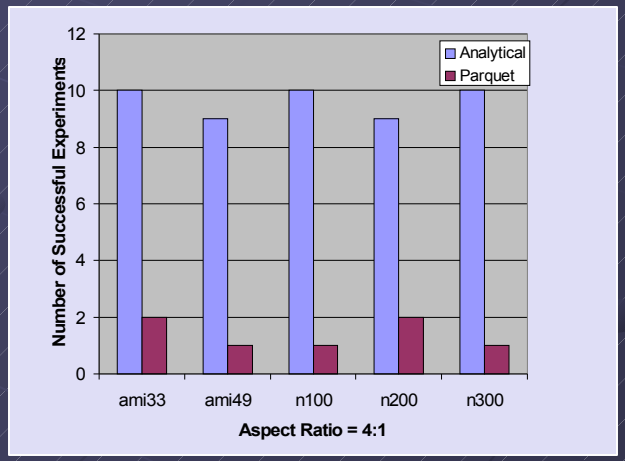
Experimental Results

- Success rate over 10 experiments (15% white space)



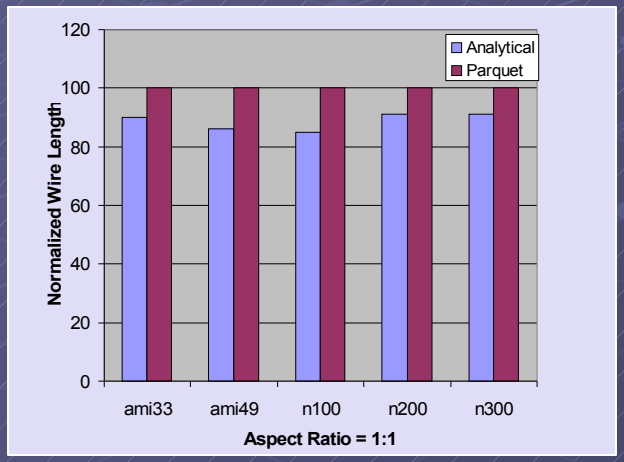


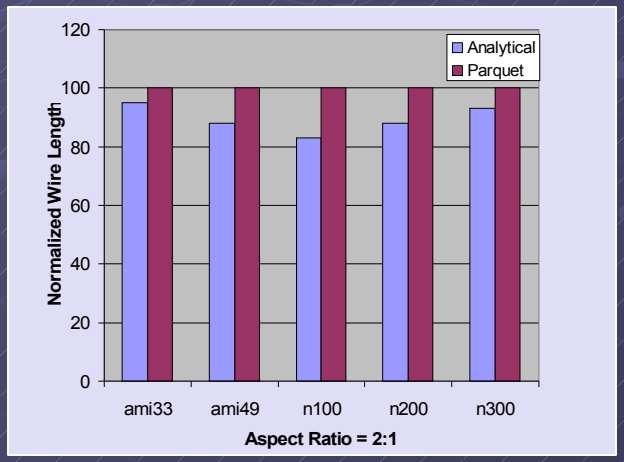


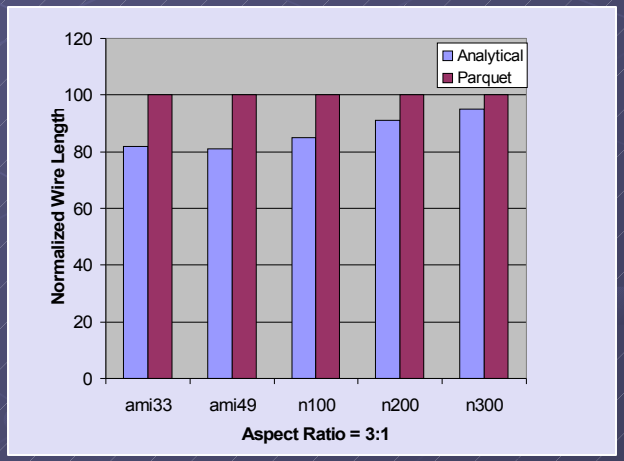


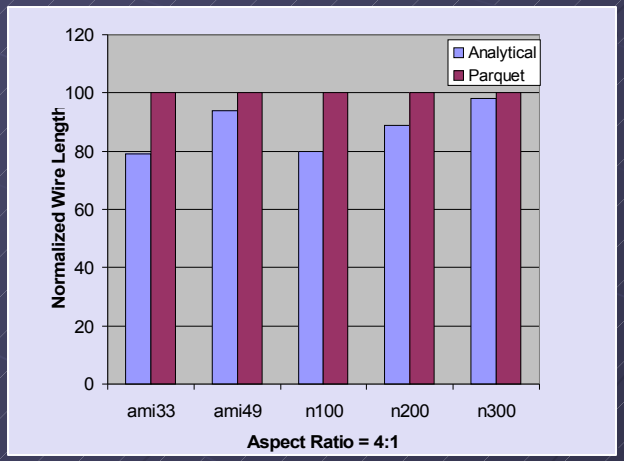
Experimental Results

- Wire Length



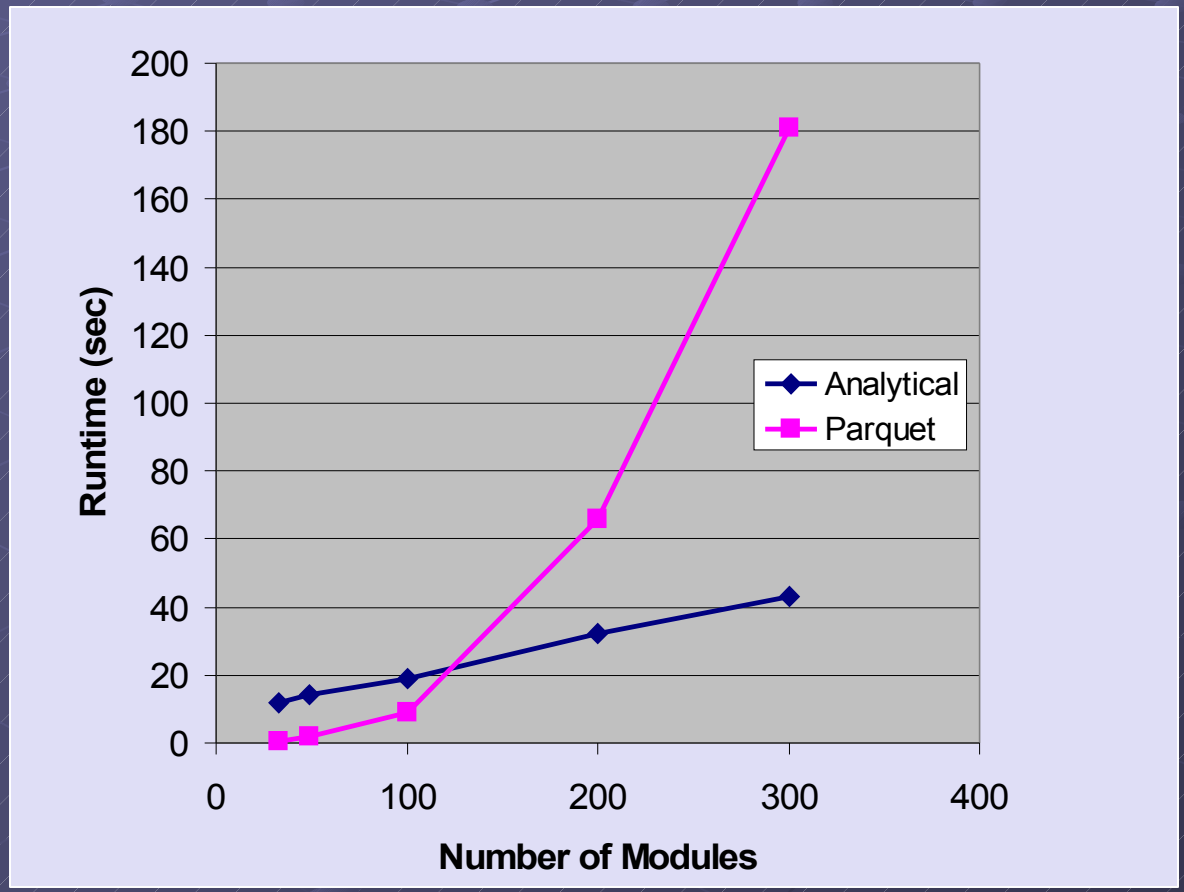






Experimental Results

- Runtime



Conclusions

- An analytical floorplanning algorithm for soft modules presented
- High success rate, good wire length, and high efficiency demonstrated