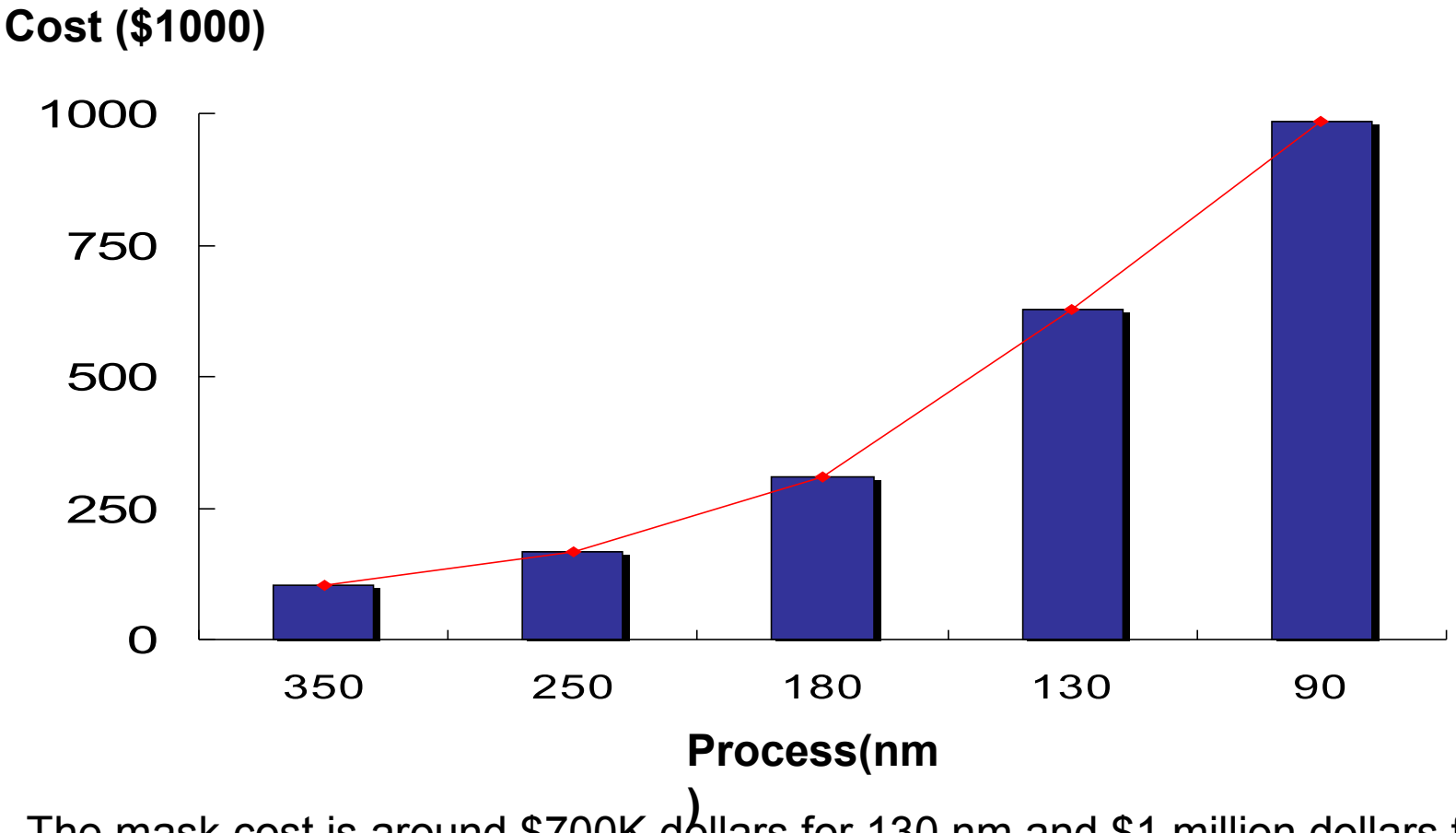
A Multi-Technology-Process Reticle Floorplanner and Wafer Dicing Planner for Multi-Project Wafers

Chien-Chang Chen and Wai-Kei Mak

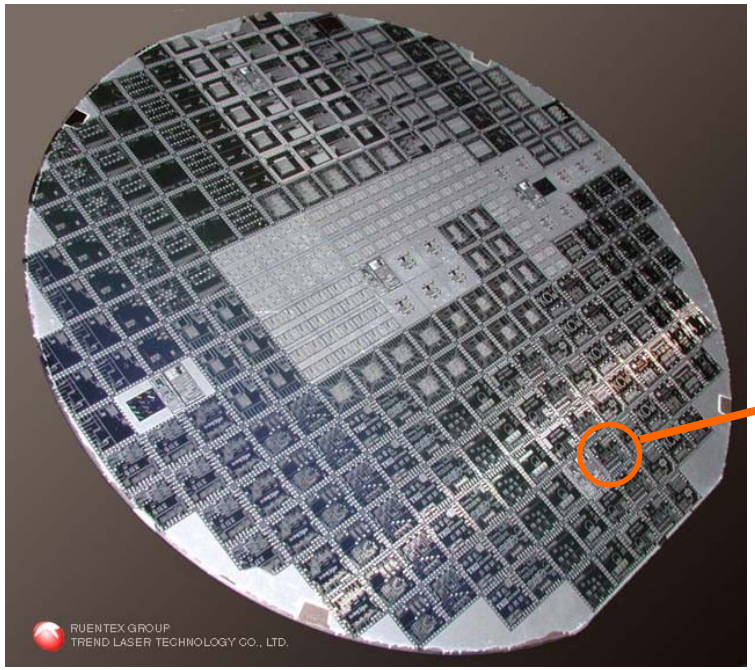
Department of Computer Science
National Tsing Hua University

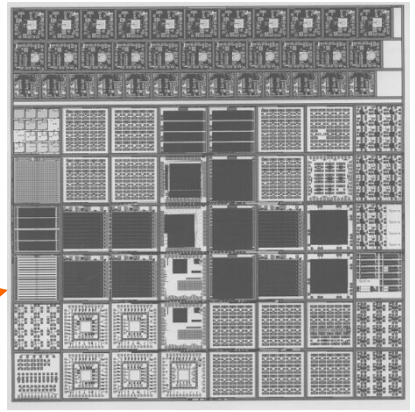
Trend of Mask cost



The mask cost is around $700K dollars for 130 nm and $1 million dollars for 90nm.

Intro. to Multi-Project Wafer





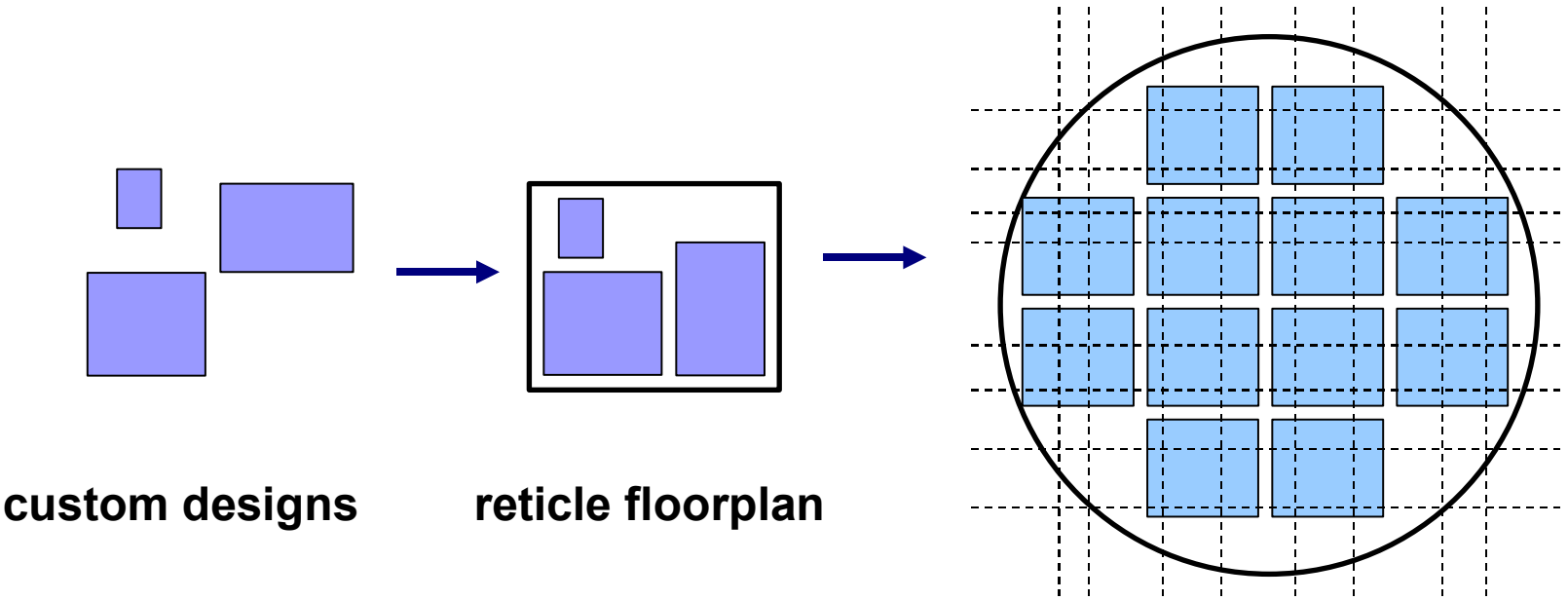
Reticle

MPW provides a cost-sharing method for fast prototyping and low volume designs.

* Source from http://www.ruentex.com.tw/trend-web/files/img_htm/sun2.htm and http://foundry.zarlink.com/gifs/mpw.jpg

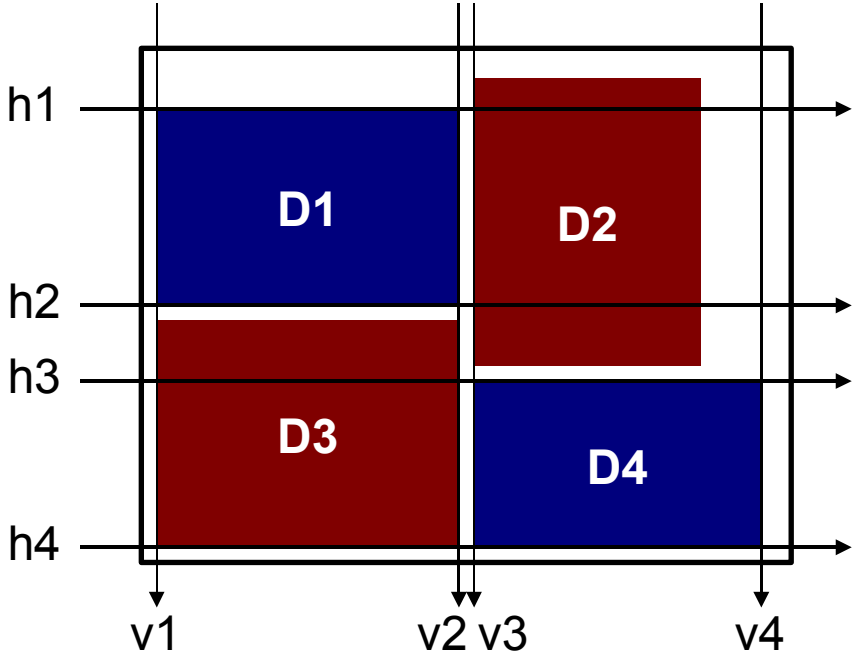
Intro. to Multi-Project Wafer

- The procedure for manufacturing Multi-Project Wafer



Intro. to Multi-Project Wafer

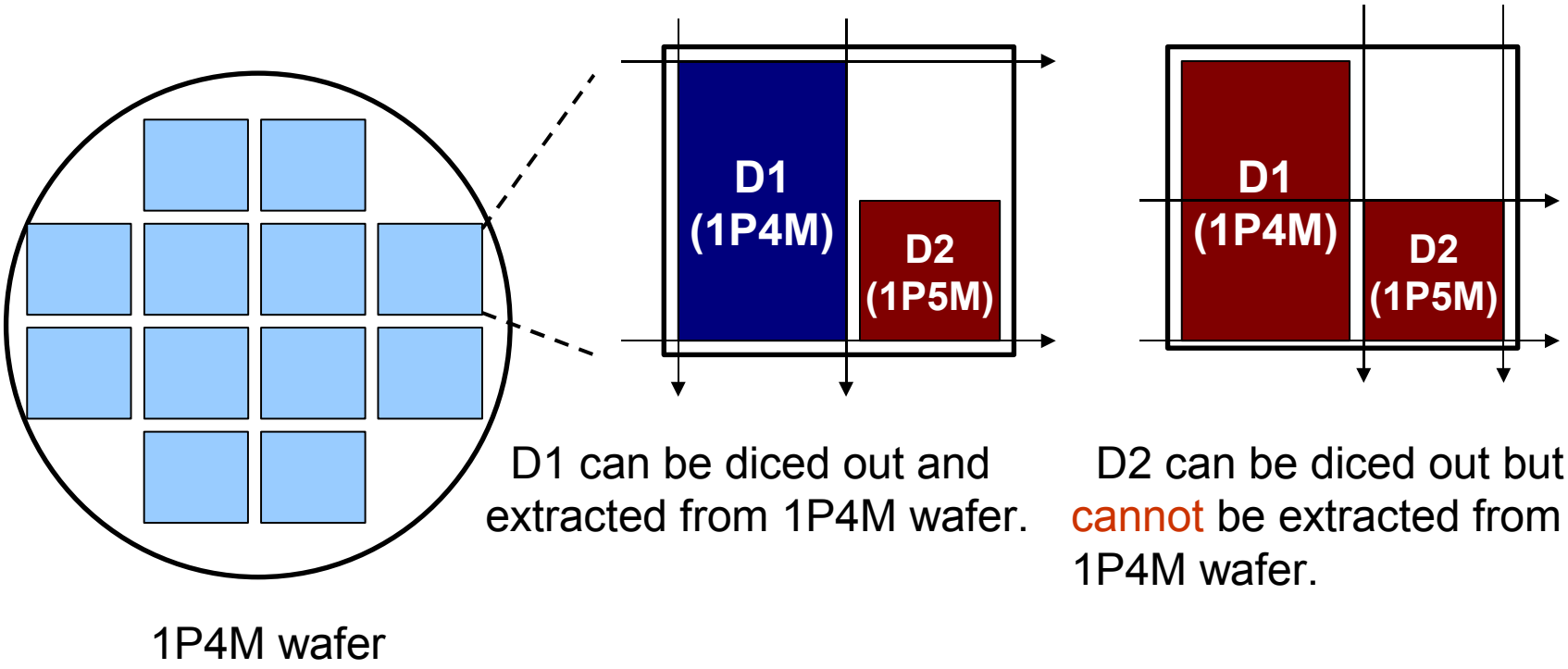
- A die can be diced out successfully only when
  (1) the cut lines are along the margins of the die;
  (2) no cut lines are across the die.



{ h1, h2, h3, h4 } is a row dicing plan.
{ v1, v2, v3, v4 } is a column dicing plan.
Only D1 and D4 are diced out.

Multi-Technology-Processes

- Each design with the desired technology process , such as 1P4M (1 poly and 4 metal layers)



1P4M wafer

D1 can be diced out and extracted from 1P4M wafer.

D2 can be diced out but cannot be extracted from 1P4M wafer.

Problem Formulation

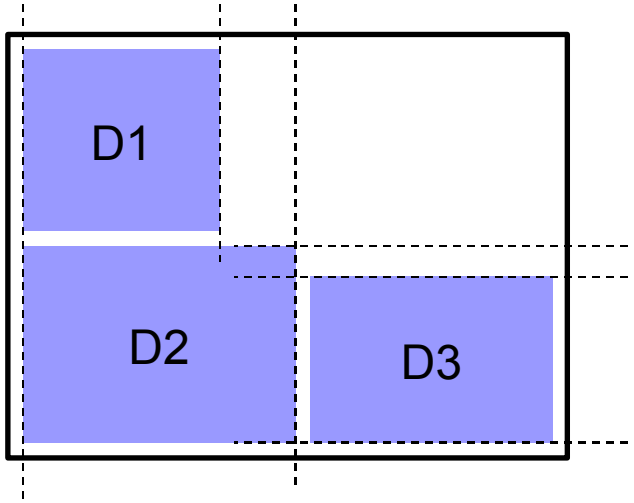
- Given : (1) a set of *N* projects with their desired technology processes and demands
  (2) the maximum dimensions of a reticle
  (3) the wafer size

- Objective : Find (1) a reticle floorplan, (2) a set of side-to-side wafer dicing plans in order to satisfy the demands of each project while minimizing the required wafers.

Conflict Situations

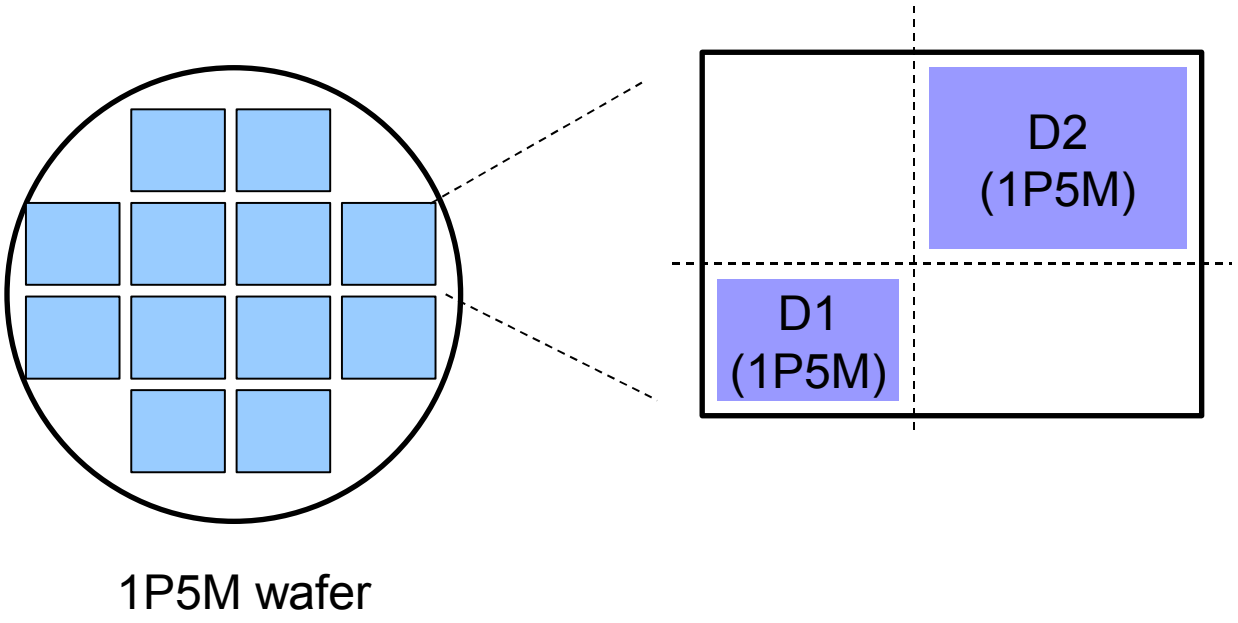
- We say that two dies are in ***vertical (horizontal) conflict*** if no set of cut lines can dice the two dies simultaneously, otherwise the two dies are ***conflict-free***.

D1 and D2 are in vertical conflict.
D2 and D3 are in horizontal conflict.
D1 and D3 are conflict-free.



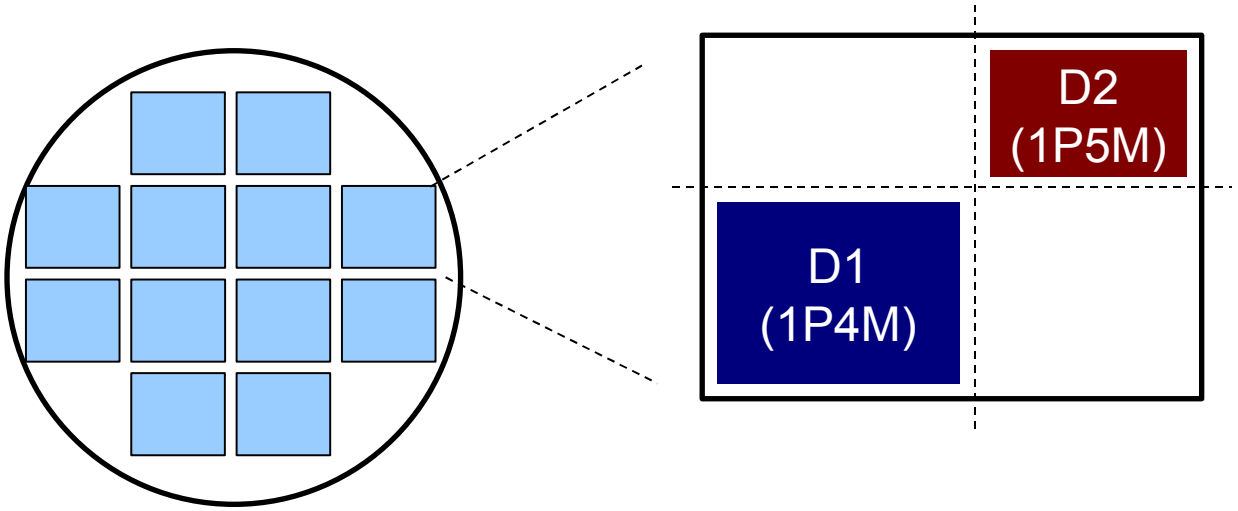
Reticle Floorplanning Analysis

- Two dies of the same technology process are in conflict-free positions on a reticle can be diced out and produced simultaneously.



Reticle Floorplanning Analysis

- Observation 1: *Even if two dies with different desired processes are conflict-free in the reticle floorplan, they still cannot be produced at the same time.*



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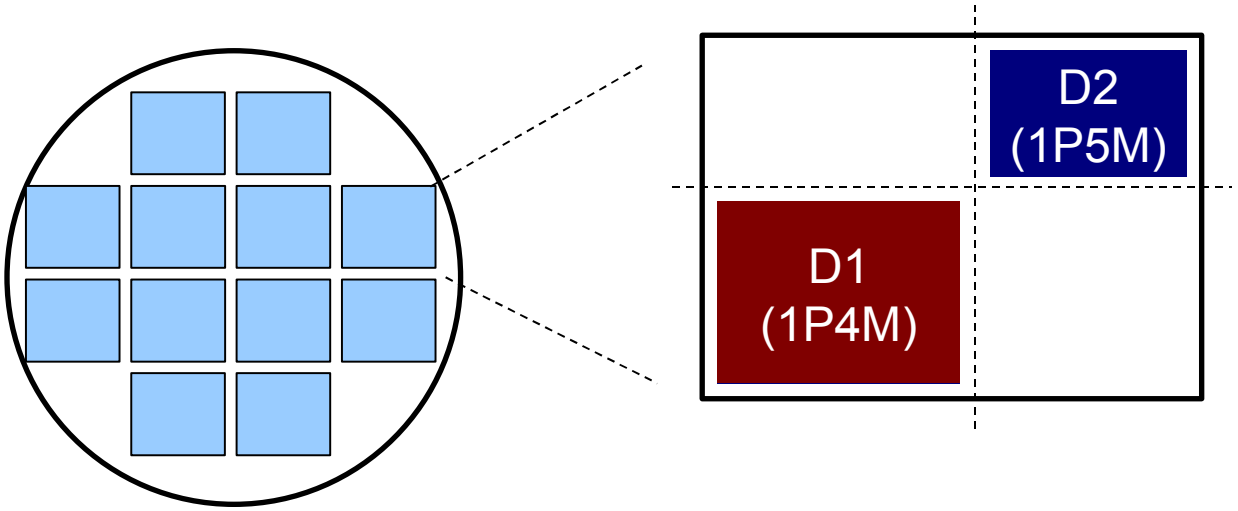


1P5M wafer

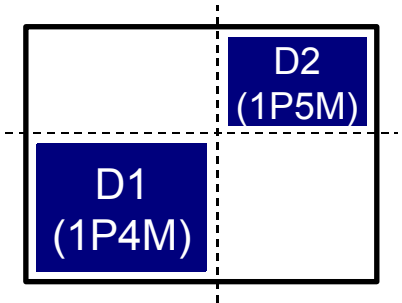
Reticle Floorplanning Analysis

- Observation 1: *Even if two dies with different desired processes are conflict-free in the reticle floorplan, they still cannot be produced at the same time.*

→ Place the dies of the same technology process in conflict-free positions on the reticle.

→ Minimize the horizontal / vertical conflict situations for dies of the same technology process.

→

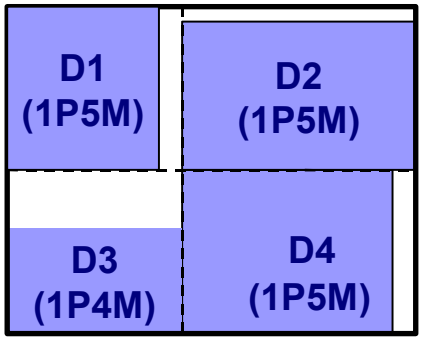


Reticle Floorplanning Analysis

- Observation 2: *We can put multiple instances of the same die on a reticle during floorplanning depending on the demand of the die.*

Variables of ILP-based Floorplanner

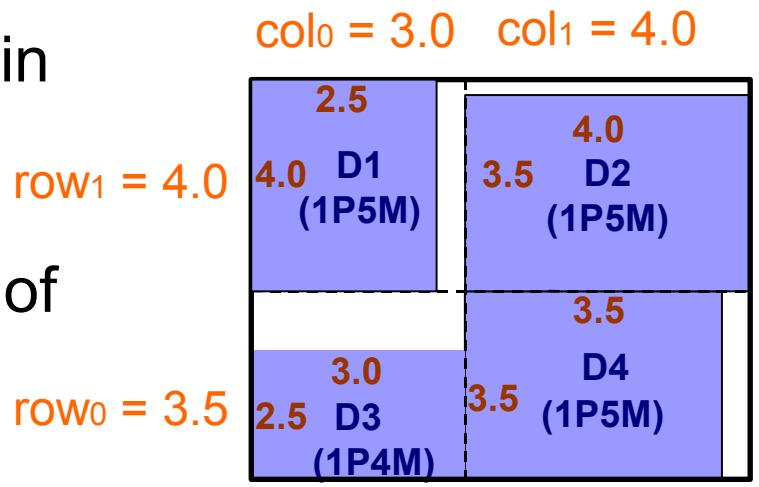
- Assume a grid structure with *p* rows and *q* columns is imposed on the reticle.



- x_{ijk} denotes whether die *k* is allocated to row *i* and column *j* or not.
- r_k denotes whether die *k* is rotated or not.

Variables of ILP-based Floorplanner

- row_i denotes the height of row *i* in the grid.
- col_j denotes the width of column *j* in the grid.
- rc_i denotes the maximum number of the dies of the same technology process in row *i*. $rc_0=1$ and $rc_1=2$
- cc_j denotes the maximum number of the dies of the same technology process in column *j*. $cc_0=1$ and $cc_1=2$



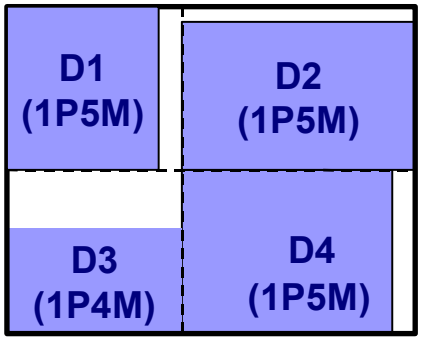
Constants of ILP-based Floorplanner

- ***W_k***, ***H_k***, ***D_k*** denote width, height, and demand of die *k* respectively, where $1 \le k \le N$.

- ***Total_Dmd*** denote the total demand of the dies,

$$Total\_Dmd = \sum_{k=1}^{N} D_k$$

- ***T_m*** denotes the set of dies which must be produced by the technology process 1P*m*M. ***T_4*** = {D3} and ***T_5*** = {D1,D2,D4}



- ***Rw***, ***Rh*** denote the given maximum width and height of the reticle.

Constraints of ILP-based floorplanner

- There is at least one instance of each die type allocated to a grid cell.

$$\sum_{i=1}^{p} \sum_{j=1}^{q} x_{ijk} \geq 1 \qquad \forall\, k$$

- At most one die allocated to each grid cell.

$$\sum_{k=1}^{N} x_{ijk} \leq 1 \qquad \forall\, i, j$$

Constraints of ILP-based floorplanner

- The height (width) of each row (column) is calculated by the following conditions,

$$H_k(x_{ijk} - r_k) + W_k(x_{ijk} + r_k - 1) \le row_i \quad \forall i$$
$$W_k(x_{ijk} - r_k) + H_k(x_{ijk} + r_k - 1) \le col_j \quad \forall j$$
$$row_i \ge 0 \quad \forall i$$
$$col_j \ge 0 \quad \forall j$$

	x_{ijk}	r_k	LHS
case1	1	1	W_k
case2	1	0	H_k
case3	0	1	<0
case4	0	0	<0

- The sum of all row heights and the sum of all column widths are not greater than the given maximum dimensions

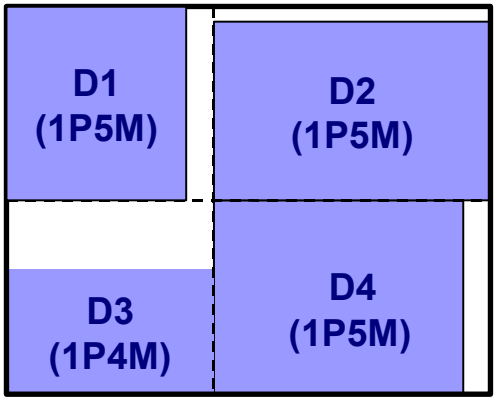
$$\sum_{i=1}^{p} row_i \le Rh$$
$$\sum_{j=1}^{q} col_j \le Rw$$

Constraints of ILP-based floorplanner

- Using the following conditions to calculate the maximum number of dies of the same technology process in row and column

$$\sum_{k \in Tm} \sum_{j=1}^{q} x_{ijk} \leq rc_i \qquad \forall\, i, m$$

$$\sum_{k \in Tm} \sum_{i=1}^{p} x_{ijk} \leq cc_j \qquad \forall\, j, m$$



Objective function of ILP-based floorplanner

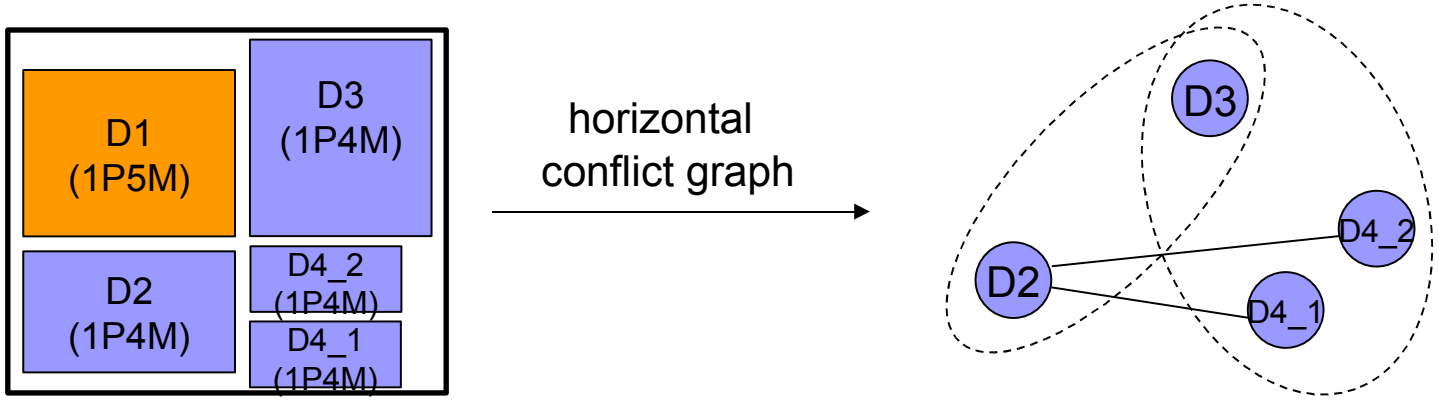
$$min: \quad \sum_{i=1}^{p} rc_i + \sum_{j=1}^{q} cc_j - \sum_{k=1}^{N} \frac{D_k}{Total\_Dmd} \sum_{i=1}^{p} \sum_{j=1}^{q} x_{ijk}$$

(1) By minimizing the maximum number of dies of the same process in each row (column), we can maximize the number of conflict-free dies for the same process.

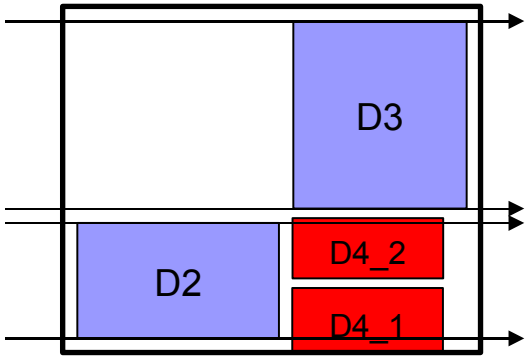
(2) We can put more than one instance of a die type on the reticle according to its demand.

Candidate row/column dicing plans

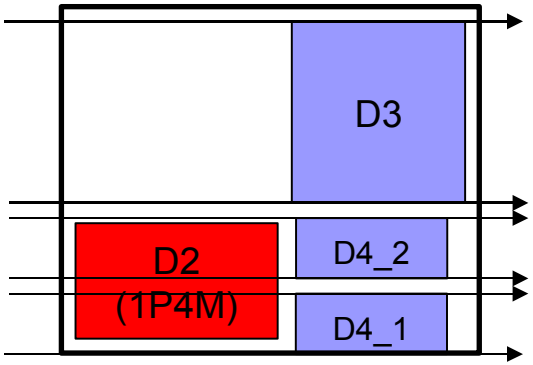
Find all candidate row (column) dicing plans of technology process 1P*4*M



rdp(1)



rdp(2)



SA-based wafer dicing planner

- Using a simulated annealing-based approach with the following perturbations,
  - Exchange the row (column) dicing plans of two rows (columns) where the number of printed reticle images of the rows (columns) are not equal.
  - Change the row (column) dicing plan of a row (column)
- We target to minimize the number of required wafers.

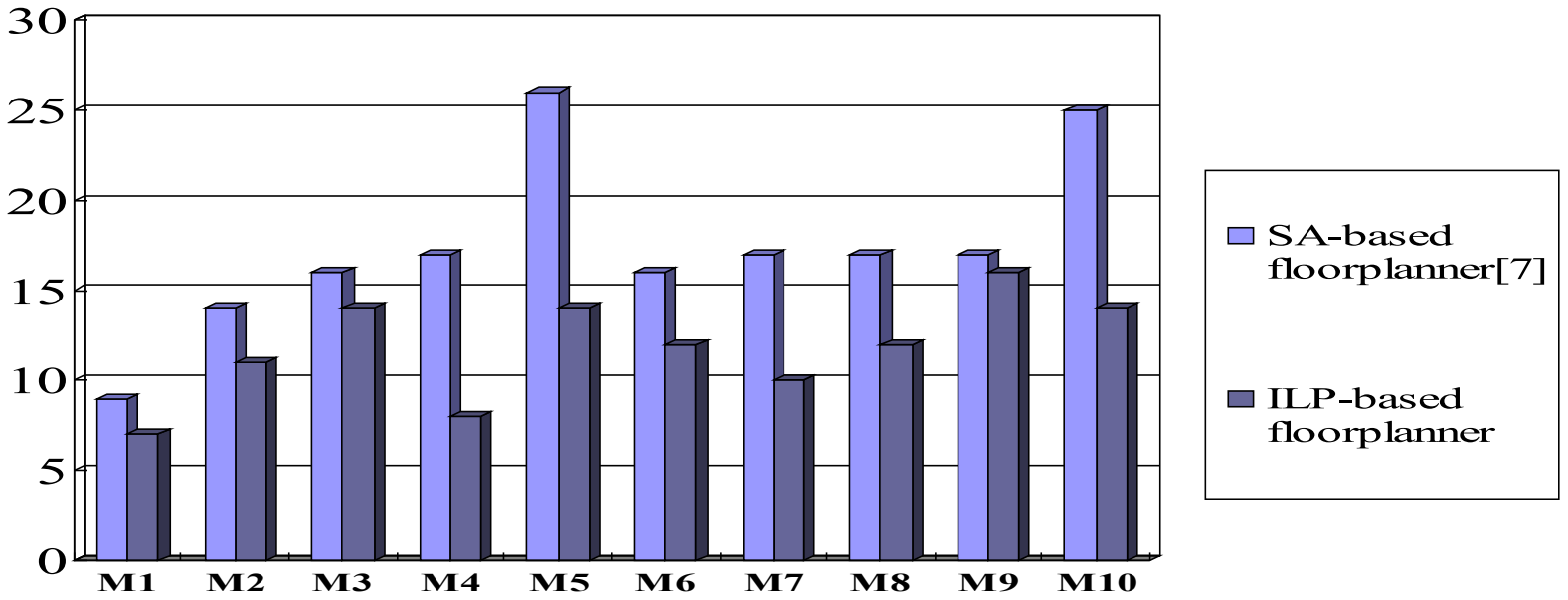
Experimental results

- We used ten benchmarks as follows to evaluate our floorplanner and wafer dicing planner.

Benchmark	No. of die types	No. of technology processes	Max. reticle dimensions.
M1	10	4	15x15
M2	10	5	20x20
M3	14	4	20x20
M4	15	4	15x15
M5	15	4	20x20
M6	16	4	20x20
M7	18	4	20x20
M8	18	3	15x15
M9	20	5	20x20
M10	20	4	15x15

Experimental results

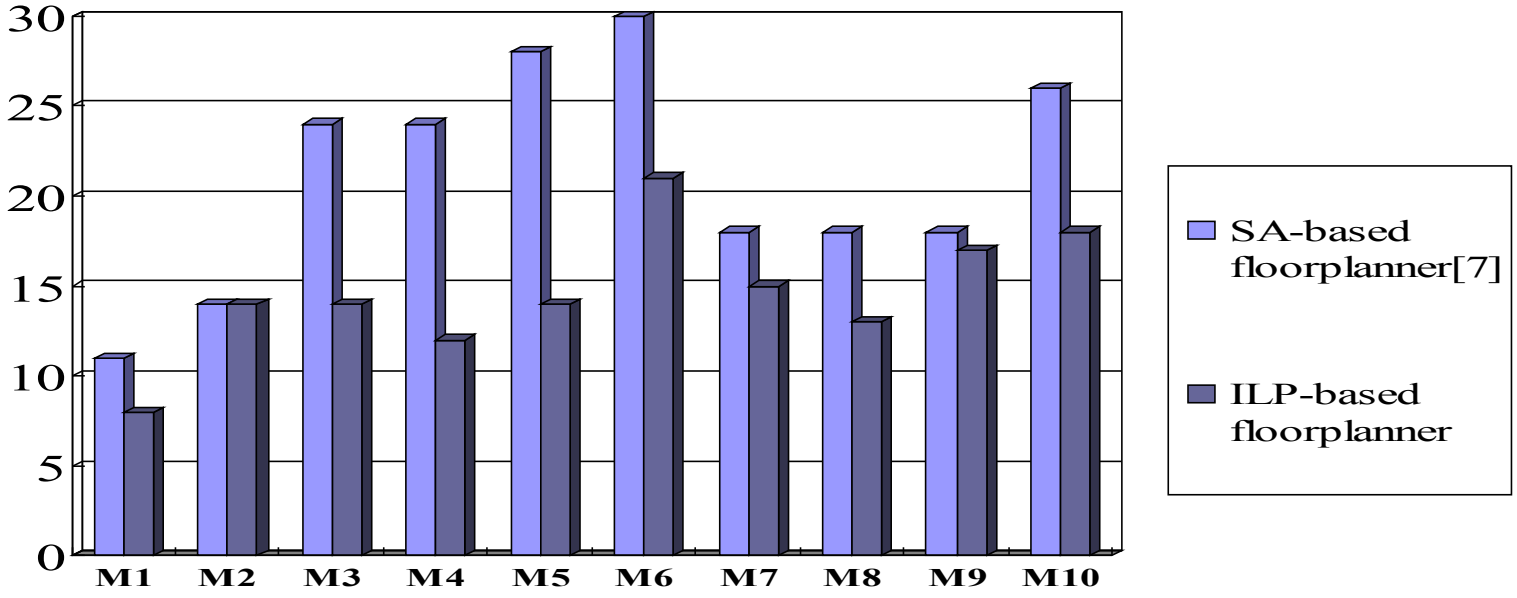
- The experiments assuming that all die types using the same technology process



The maximum wafer reduction is 52% and average reduction is 30%.

Experimental results

- The experiments considering the desired technology process of each die.



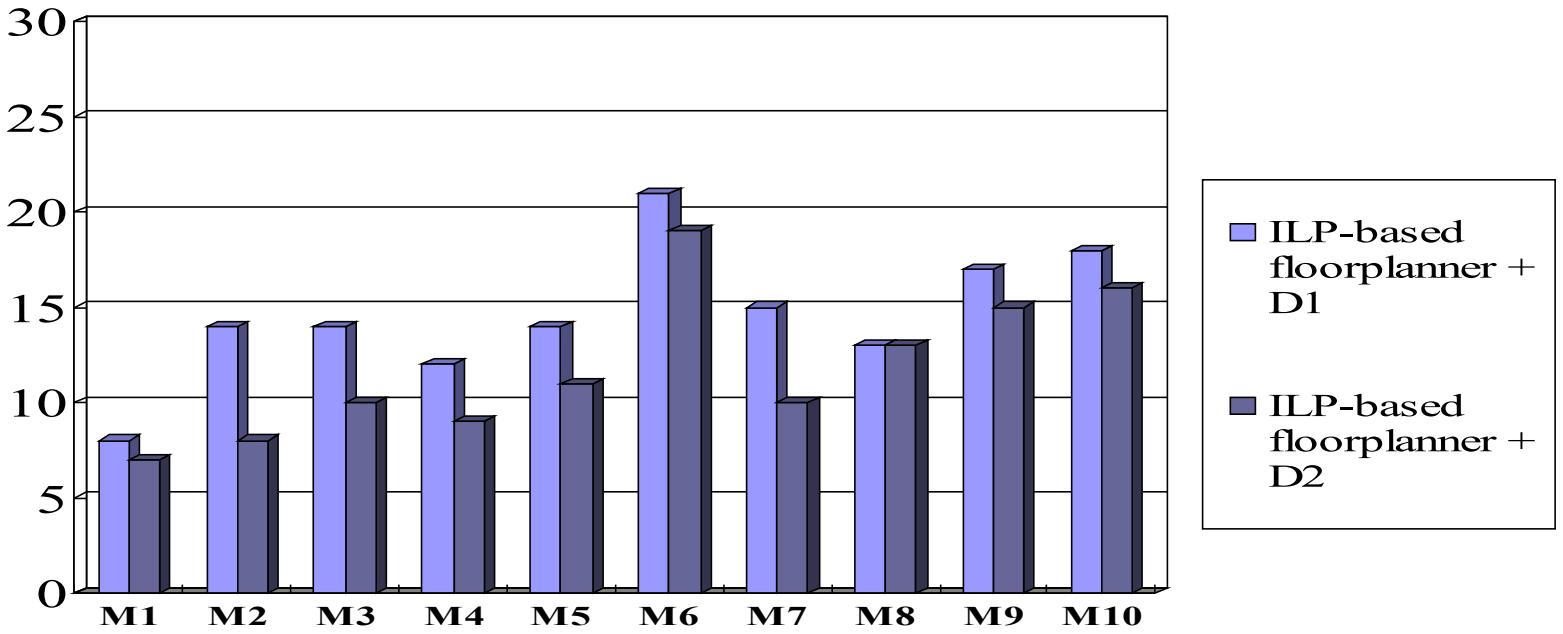
The maximum wafer reduction is 50% and average reduction is 28%.

Experimental results

- We tried two mechanisms of wafer dicing for comparison.

  D1 : Use the same wafer dicing plan for the same technology process wafers.

  D2 : Use different wafer dicing plan for each wafer.



Conclusions

- We considered the fact that each design has its own desired technology process.
- Our floorplanner incorporates die replication according to the demand of each die type.
- Our wafer dicing planner considered the circular shape of the wafer.
- The experimental results are better than a previous SA-based floorplanner.

Thank you !