Design Space Exploration for Minimizing Multi-Project Wafer Production Cost

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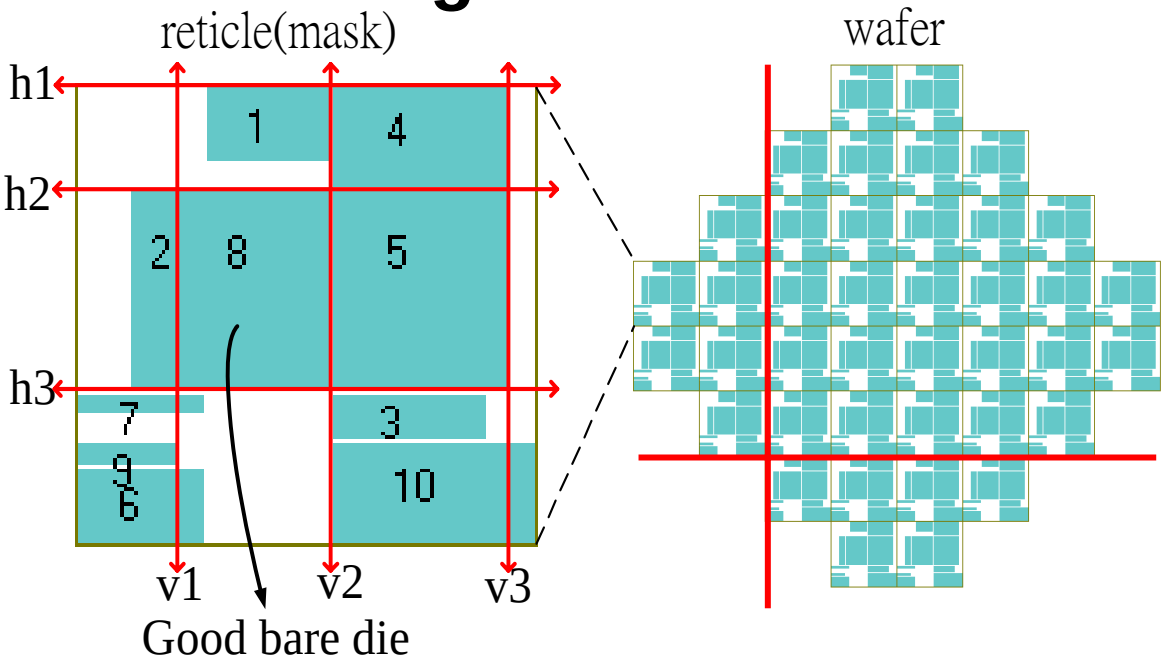
Outline

- Introduction
- Cost Model
- Compatibility & Area Driven Floorplanner
- Space Exploration Methodology
- Experimental Results
- Conclusions

Multiple Project Wafers (MPW)

- An MPW consists of many reticle fields, each of which has more than one chip from different projects
- To amortize mask cost and wafers' cost among chips from different projects
- Side-to-side dicing constraint



Reticle Floorplanning Problem

- **Input**

  ***N* chips, their widths and heights, their required production volumes, and the upper bounds on reticle width and height**

- **Constraints**

  Non-overlapping constraints and side-to-side dicing constraints

- **Objective**

  Dicing yield is maximized

- **Output**

  The coordinates of these chips in a reticle

Wafer Dicing Problem

- **Input**

  A reticle floorplan of *N* chips and the required production volumes V_p for chips *p*'s

- **Constraints**

  Side-to-side dicing constraint

  $V_p \leq B_p$ **(number of good bare dice)**

- **Objective**

  Min Q **(the number of wafers used)**

- **Output**

  The wafer dicing plan for each of the *Q* wafers

Ways for Satisfying Production Volumes

- **Wafer yield**

$$z_k = \min_{\forall p} B_p / V_p$$

where B_p is the number of good bare dice,

V_p is the required production volume,

k is the given number of wafers

- **Estimate the number of wafers used *Q***

$$Q = k\lceil 1/z_k \rceil$$

Why Design Space Exploration?

- **Production cost is not solely decided by the number of wafers**
  - **Dicing yield ➡ the number of wafers used**
  - **Wafer lithography cost**
  - **Reticle area ➡ mask cost**

Cost Analysis for Wafer Fabrication

- **Mask cost**
  - **The reticle area is larger, the mask cost is higher**
  - **Main contributors**
    - **Data preparation, mask write, mask inspection, mask repair, etc.**
- **Wafer production cost**
  - **Wafer field size (reticle size) dependent**
    - **Exposure**
  - **Wafer field size independent**
    - **Hot process, etching, sputtering, polishing, materials, etc.**

Total MPW Fabrication Cost

$$T_{mpw}(A) = C_m(A) + Q(A)C_e(A) + Q(A)C_w$$

Where

***A*: reticle area**

$C_m(A)$: mask cost

$C_e(A)$: exposure cost per wafer

C_w: field-size independent wafer cost

$Q(A)$:the number of wafers needed to satisfy volume requirements

Exposure Cost per Wafer

$$C_e(A) = n_A(l_v c_v + l_c c_c + l_n c_n)$$

where

***A*: the wafer field size**

n_A: the number of reticle on a wafer

l_v, l_c and l_n: the number of very critical, critical, and non-critical layers, respectively

c_v, c_c and c_n: costs per exposure for the corresponding layers

Our Cost Share Model

$$C_{mpw}(p) = C_m(A)A_p \Big/ \sum_{i=1..N} A_i +$$

$$C_e(A)Q(A)V_p \Big/ \sum_{i=1..N} V_i + Q(A)C_w A_p V_p \Big/ \sum_{i=1..N} A_i V_i$$

Where

***N*: the number of chips going with MPW**

$C_m(A)$: the mask set cost with reticle area *A*

A_i: the area of chip *i*

$C_e(A)$: the exposure cost per wafer

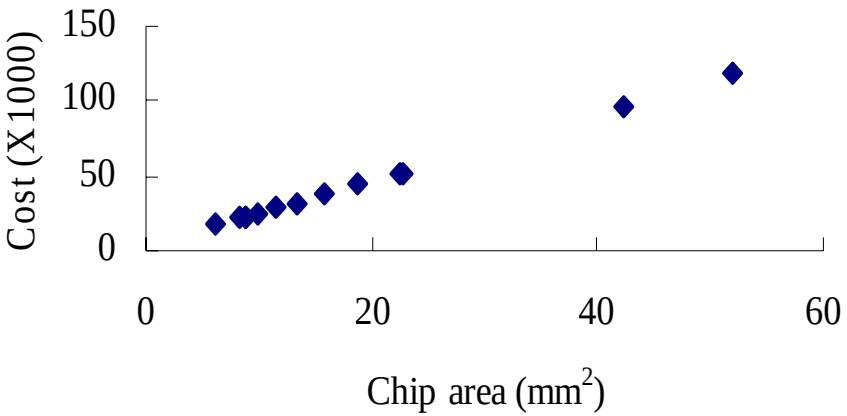
$Q(A)$: the total number of wafers used

C_w: the field-size independent cost per wafer

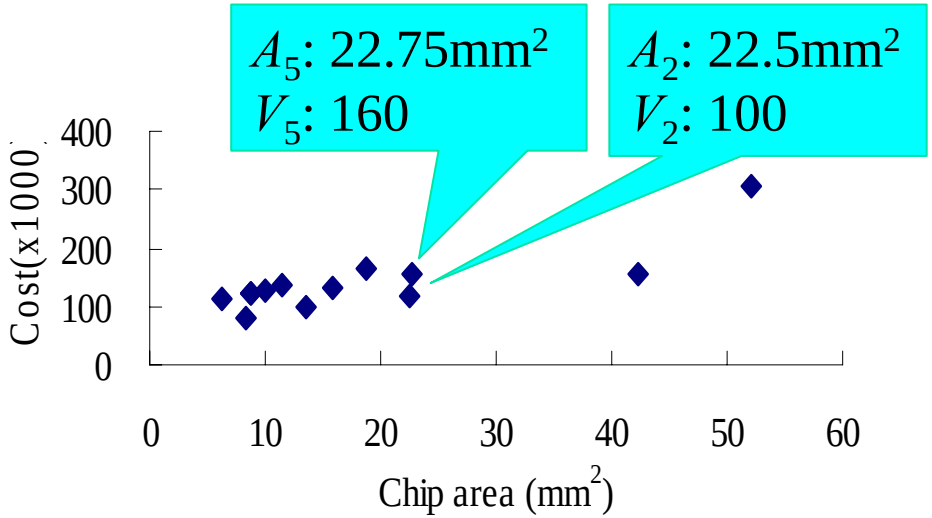
V_i: the required production volume of chip *i*

Production Cost Share

- **Properties**
  - **A smaller chip should pay less than a larger chip if they have the same production volume**
  - **A chip with larger production volume should pay more than a chip with smaller production volume if they have the same area**



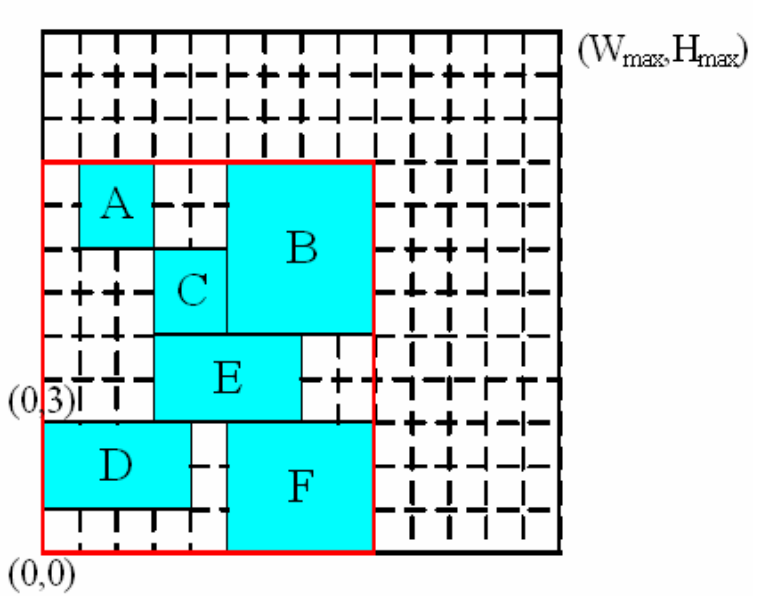
Cost shared by chips with same production volume



Cost shared by chips with different production volume

Compatibility & Area Driven Floorplanner

- **Discretized reticle plane**



- **Neighborhood structures for SA**
  - **Move a chip to a new location**
  - **Rotate a chip**
  - **Move a chip and then rotate it**
  - **Move a chip and align it with another chip**

Compatibility & Area Driven Floorplanner cont.

- **Objective function**

$$Max \quad (1-\delta_1-\delta_2)\sum_{p=1}^{N-1}\left(\sum_{q=p+1}^{N} E_{pq}(V_p+V_q)\right)-\delta_1\beta WH-\delta_2\beta R$$

where

***E*$_{pq}$: 1 if chips *p* and *q* are compatible**

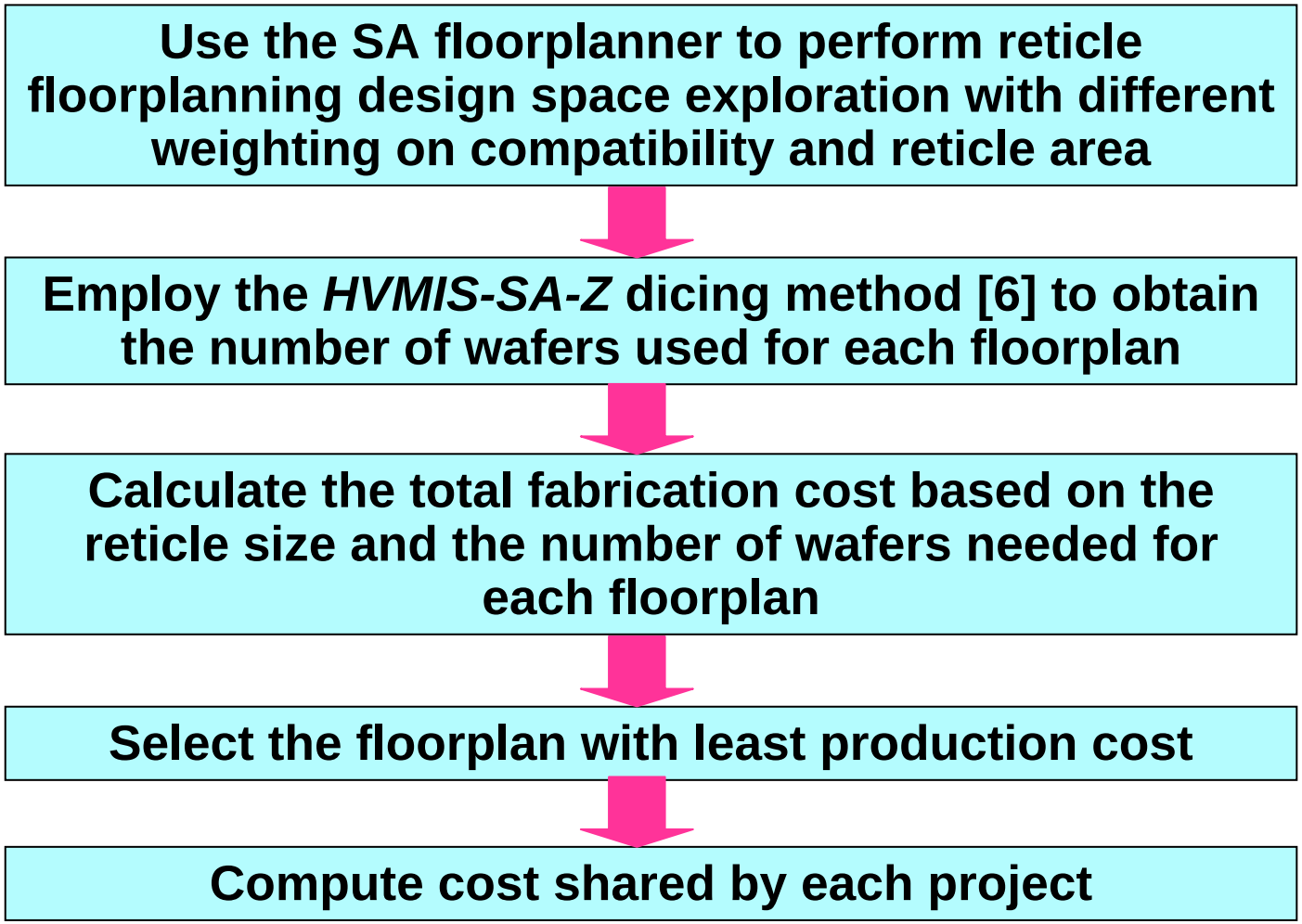
$\beta=(N-1)\sum_{p=1}^{N}V_p/(W_{\max}H_{\max})$ **: normalizing factor**

***W* (*H*): reticle width(height)**

***R* : the total overlap area of chips**

$\delta_1(\delta_2)$ **: coefficient for reticle and compatibility (penalty)**

Space Exploration Methodology



Experimental Setup

- **300mm wafers**
- **8 very critical layers (l_v), 8 critical layers (l_c), and 12 non-critical layers (l_n) from [7]**
- **Costs per exposure from [7]: c_v=\$2.5, c_c=\$1.5, c_n=\$0.5**
- **Field size independent wafer cost (C_w) from [12]: \$2500**

Mask Cost & Test Cases

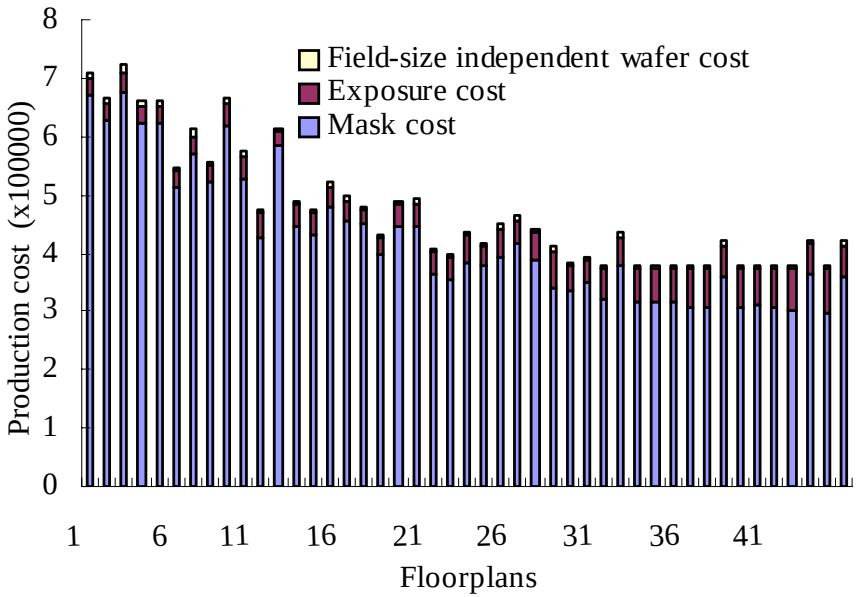
Source: [7]

Wafer field size	25*25 625mm^2	16*24 384 mm^2	16*16 256 mm^2	8*16 128 mm^2	8*8 64mm^2
Mask cost	1,240,000	728,000	532,000	352,000	296,000

(*w*, *h* | 1X required volume) W_{max}=20 mm, H_{max}=20 mm	
I5	(2.5,6.25 | 100|), (1.8,5.5 | 200), (2,1.25 | 300), (2.2,1.75 | 200), (1.7,2.25 | 200), (1.5,1.55 | 200), (2.3,3.75 | 200), (1,3.25 | 200), (1.3,4.25 | 80), (2.7, 1.1 | 60)
I6	(6.5, 6.5 | 60), (4.5, 5.0 | 100), (5.5, 1.5 | 120), (4.5, 3.0 | 120), (6.5, 3.5 | 160), (4.5, 3.5 | 160), (6.5, 8.0 | 200), (3.3, 3.5 | 200), (2.5, 3.5 | 200), (3.5, 2.5 | 200), (7.5, 2.5 | 200), (4.0, 2.5 | 200), (2.5, 2.5 | 200)

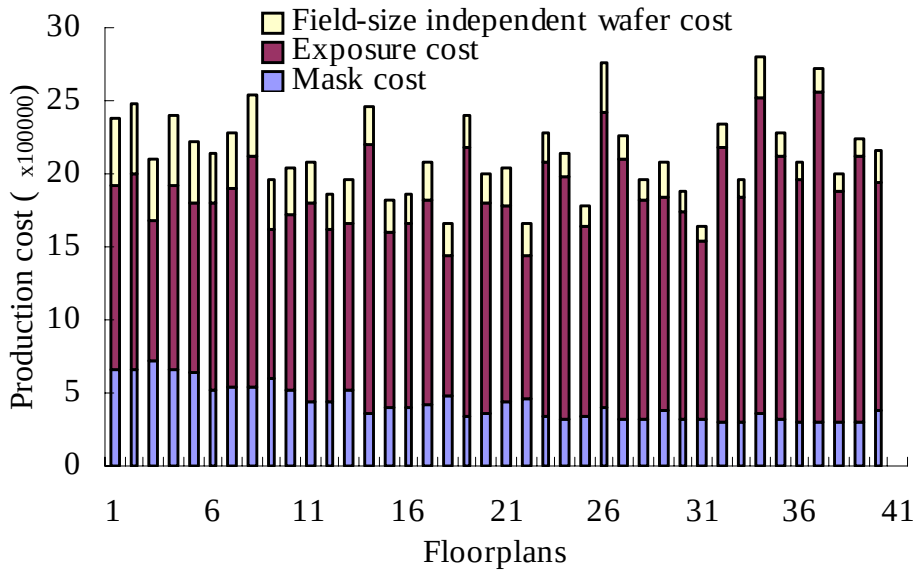
MPW Production Cost

48% saving w/r poorest
34% saving w/r average



I5 with 1X volume

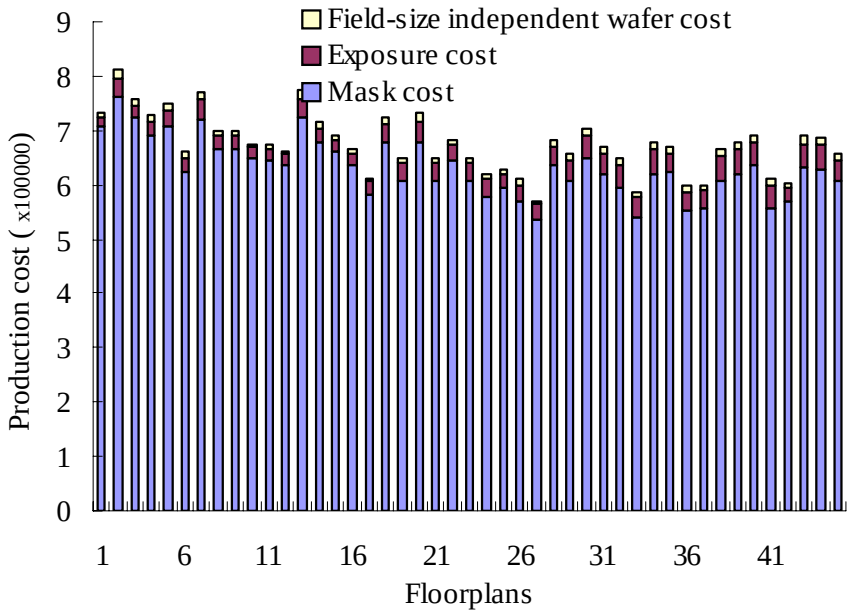
41% saving w/r poorest
24% saving w/r average



I5 with 50X volume

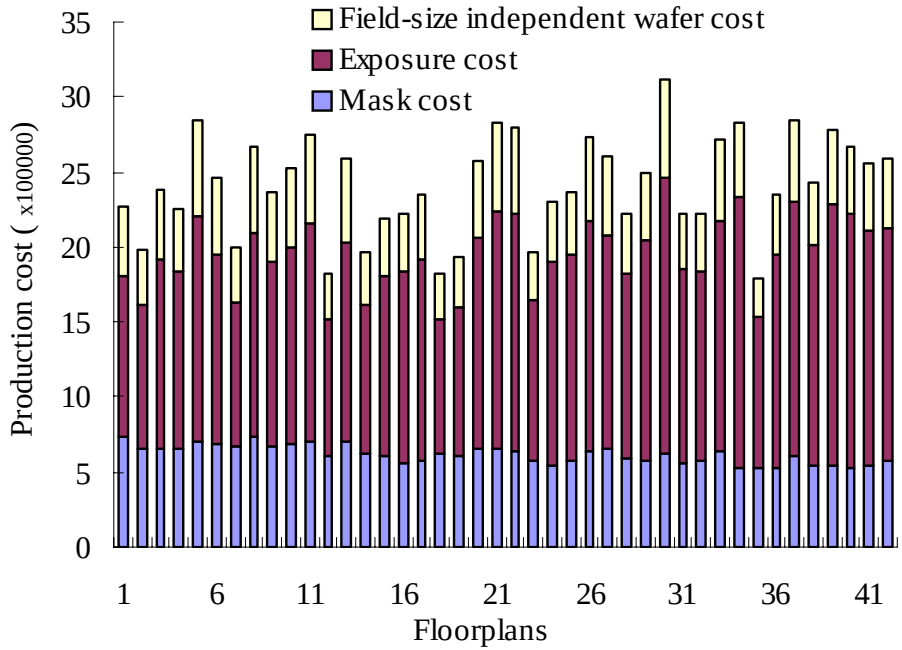
MPW Production Cost

30% saving w/r poorest
17% saving w/r average



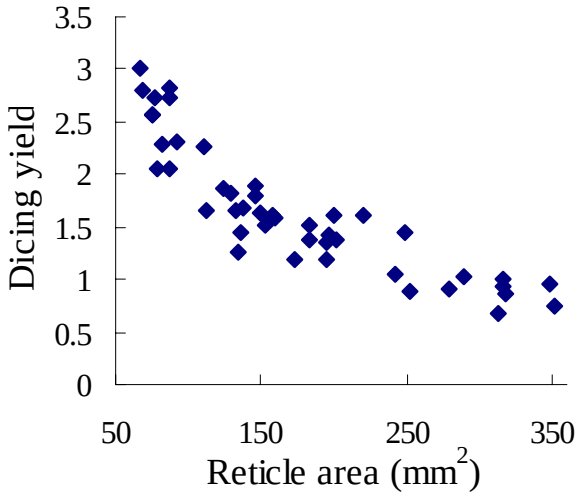
I6 with 1X volume

42% saving w/r poorest
22% saving w/r average

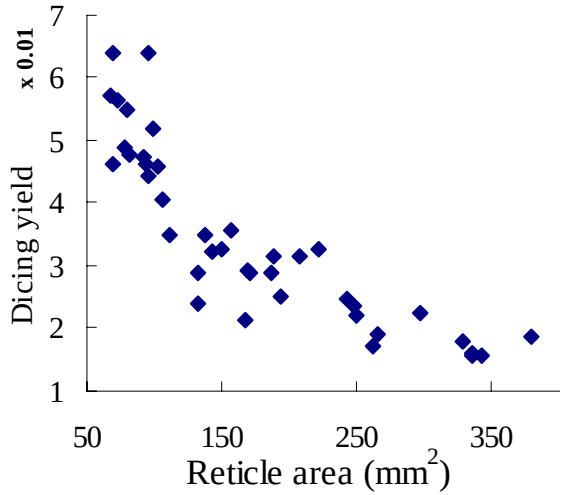


I6 with 50X volume

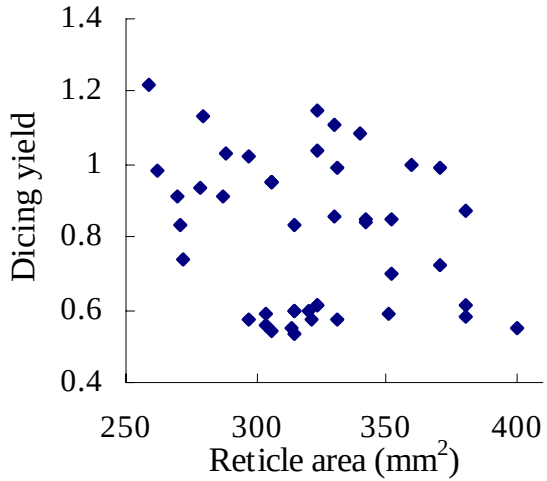
Reticle area vs. Dicing Yield



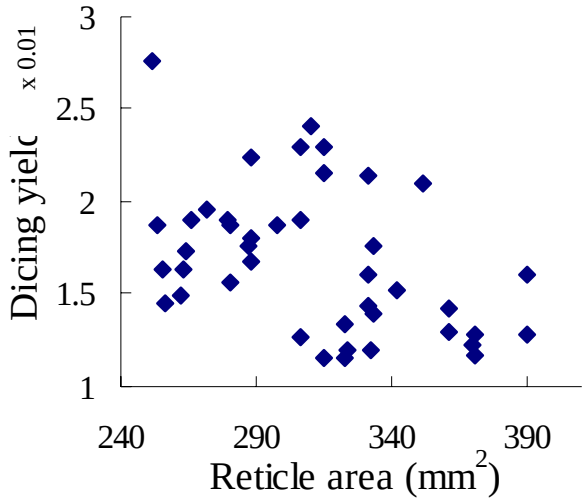
I5 with 1X volume



I5 with 50X volume

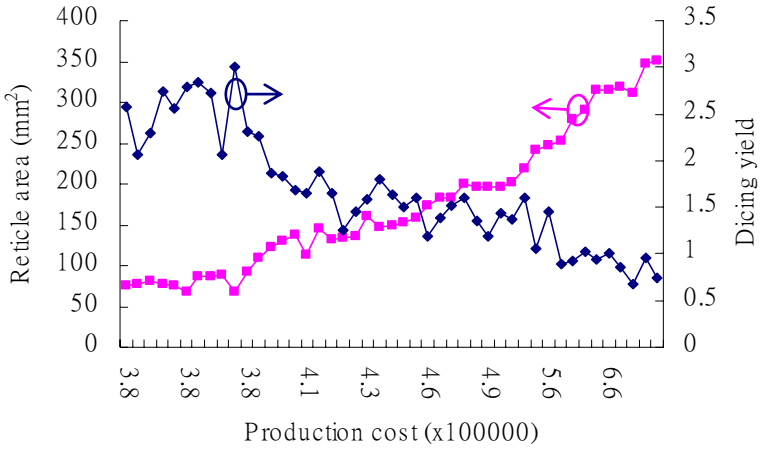


I6 with 1X volume

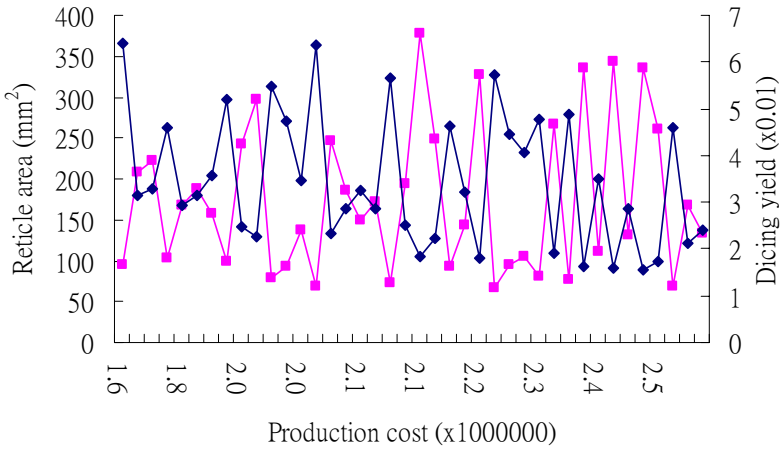


I6 with 50X volume

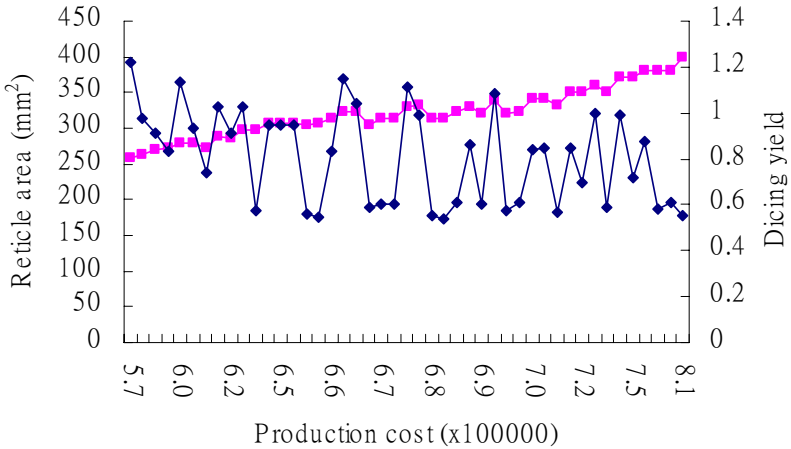
Reticle Area, Dicing Yield, and Production Cost



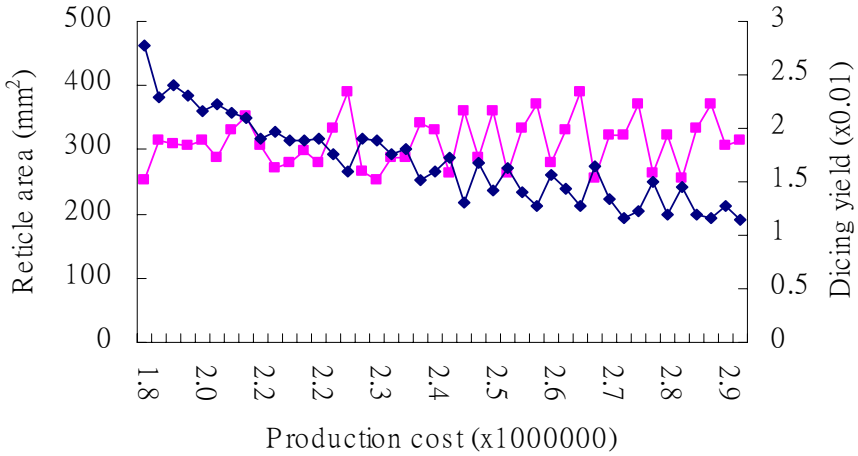
I5 with 1X volume



I5 with 50X volume



I6 with 1X volume



I6 with 50X volume

Conclusions

- A methodology to explore MPW reticle floorplan design space
- A compatibility and area-driven floorplanner based on SA
- A new formula for computing the MPW fabrication cost assumed by each chip
- A good floorplan saving up to 48% cost for small volume production and 42% cost for medium volume production
- Although reticle area generally corresponds well to production cost, especially for small volume production, a design space exploration is strongly recommended for achieving minimal-cost production

Thank you for your attention!