Power distribution techniques for dual-VDD circuits

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Outline

- Motivation for multiple supply design
- Implications of using multiple on-chip supplies
- Power delivery
  - Board and package level issues
  - On-die power grid design
- Results and conclusions

Motivation – low power design

- Reducing power dissipation at high performance essential for: enhanced battery life in mobile applications, reduced cooling costs for workstations, improved reliability, …

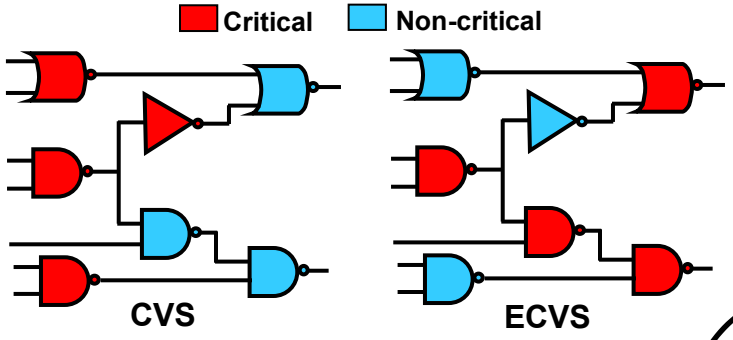
- Dynamic power dissipation in CMOS circuits α $(VDD)^2$
  Static power dissipation in CMOS circuits α $(VDD)^3$

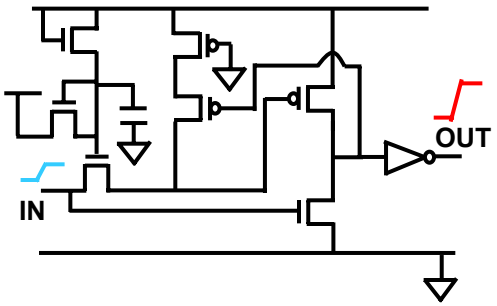
- Quadratic/cubic savings in power if VDD scaled down
  - However, delay goes up, thus necessitating careful VDD assignment

$\Rightarrow$ Multi-VDD design – an important technique leveraging this

Several implications when actually implementing this idea

Implications of using multiple supplies





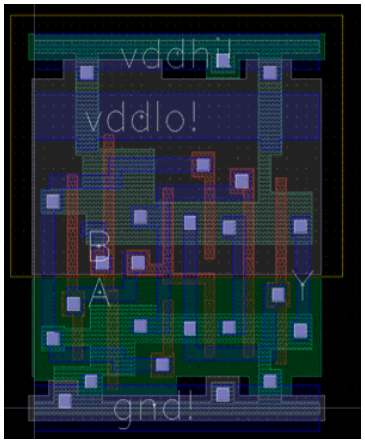
Circuits
Level shifting

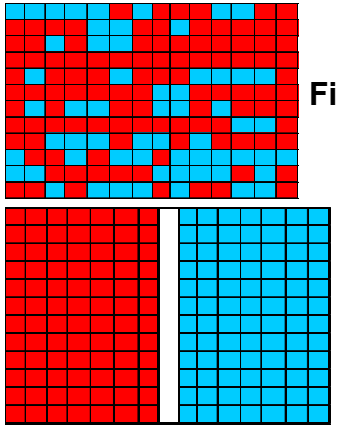
Algorithms
VDD assignment

Coupled issues

Physical design
VDD Granularity

Power delivery
Distribution
Generation





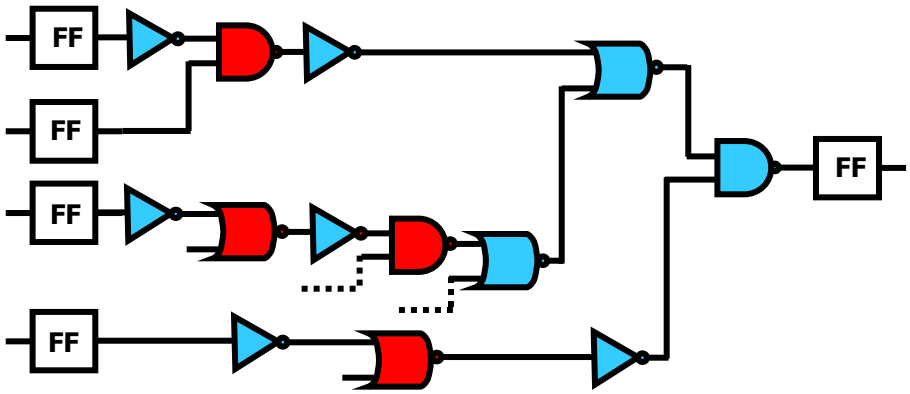
Fine-grained

Islanding

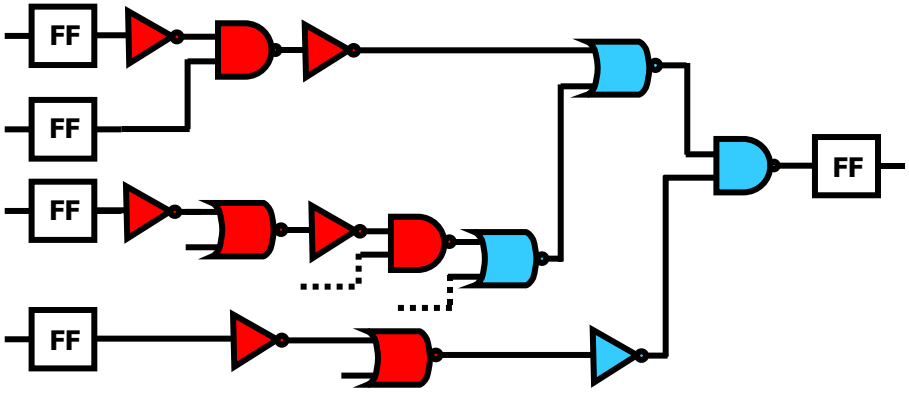
Multiple supply design

- Concept: Apply a lower supply (VDDL) to gates on non-critical paths thus reducing power while meeting timing

Fine-grained Dual-VDD



Dual-VDD islands



- A fine-grained VDD assignment scheme provides best power reduction
  - Extended Clustered Voltage Scaling (ECVS)
    K. Usami *et al.*, "Automated low power technique exploiting multiple supply voltages applied to a media processor," *IEEE JSSC*, 1998.
- However, physical design and power delivery are complicated

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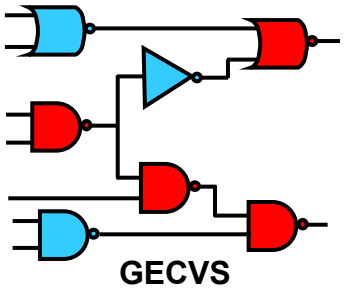
Power delivery for dual-VDD circuits

- Fine-grained dual-VDD places VDDL/VDDH gates arbitrarily on the die
- Dual-VDD circuits need to supply two on-die voltages
  - Wire congestion
  - Power grid integrity
- Board and package level issues
  - Fixed resources need to be split between VDDL and VDDH
- However, load on each supply lower than on original single supply, allowing robust power delivery within available resources (fixed decap, C4, wiring)

VDD assignment and power savings

- A large number of gates go to the lower supply in a dual-VDD optimized netlist

	VDDL = 0.8V		VDDL = 0.6V	
	% Savings	%VDDL	% Savings	%VDDL
c880	28	65	31	55
c2670	32	65	37	56
c5315	35	58	37	49
c7552	44	91	49	71

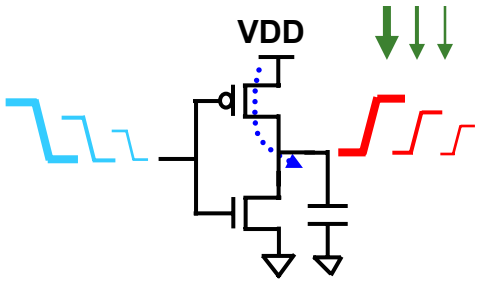


  - Avg. 70% (58%) for VDDL = 0.8V (0.6V) with respect to original single VDD design (1.2V)

Current drawn from VDDL/VDDH

- Current drawn at gate level

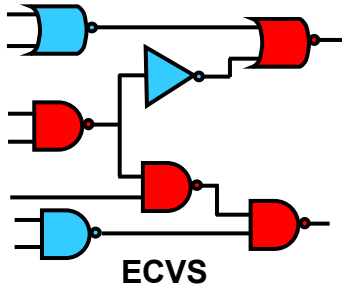
	Single-VDD		Dual-VDD: VDDL=0.8V		Dual-VDD: VDDL=0.6V	
	Low-VTH	High-VTH	Low-VTH	High-VTH	Low-VTH	High-VTH
INVX10	1.00	0.90	0.57	0.49	0.36	0.27
NAND2X2	1.00	0.85	0.54	0.45	0.34	0.23
NAND3X6	1.00	0.88	0.55	0.47	0.35	0.24
NOR2X1	1.00	0.86	0.52	0.39	0.30	0.19
NOR3X4	1.00	0.85	0.50	0.37	0.29	0.18



  - Avg. 54% (33%) for VDDL = 0.8V (0.6V)

- Current drawn at circuit level

	Single VDD	Dual VDD: VDDL=0.8V		Dual VDD: VDDL=0.6V	
	VDD	VDDH	VDDL	VDDH	VDDL
c880	9.7	5.6	2.2	5.9	1.3
c2670	23.6	11.9	6.5	10.1	3.0
c5315	36.7	20.9	7.2	20.9	3.6
c7552	47.9	13.9	19.4	20.4	8.5



  - Avg. 49% (51%) and 28% (14%) for VDDH and VDDL for 0.8V (0.6V)

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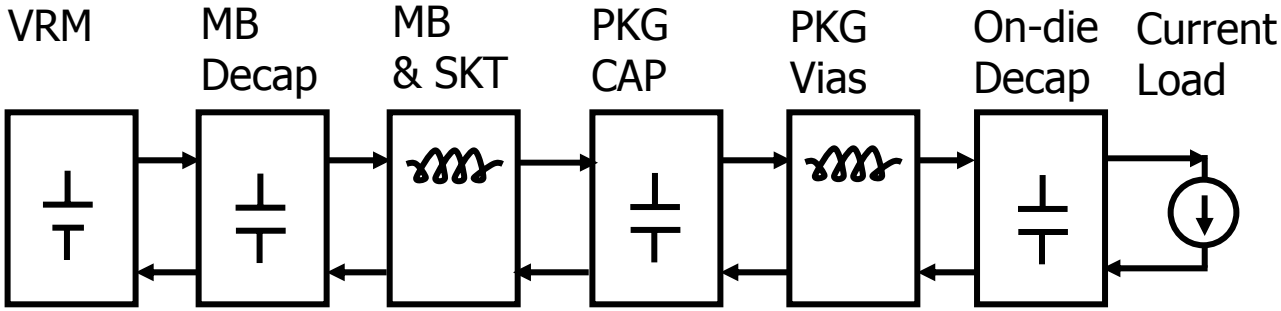
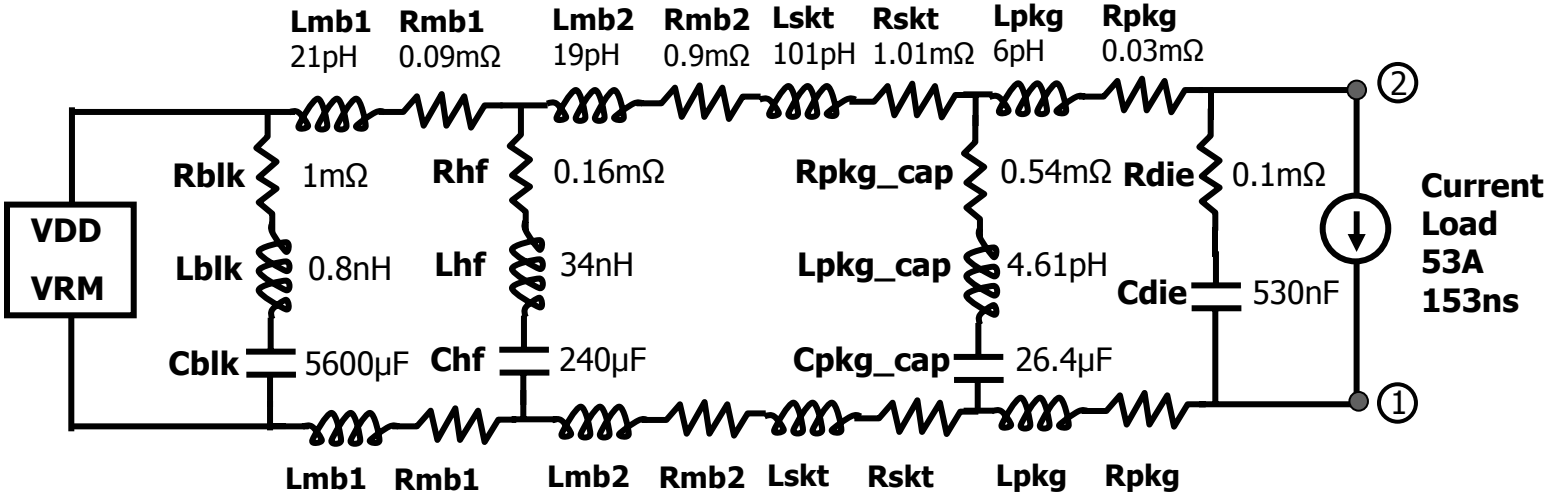
Board and package level study

- High-level model



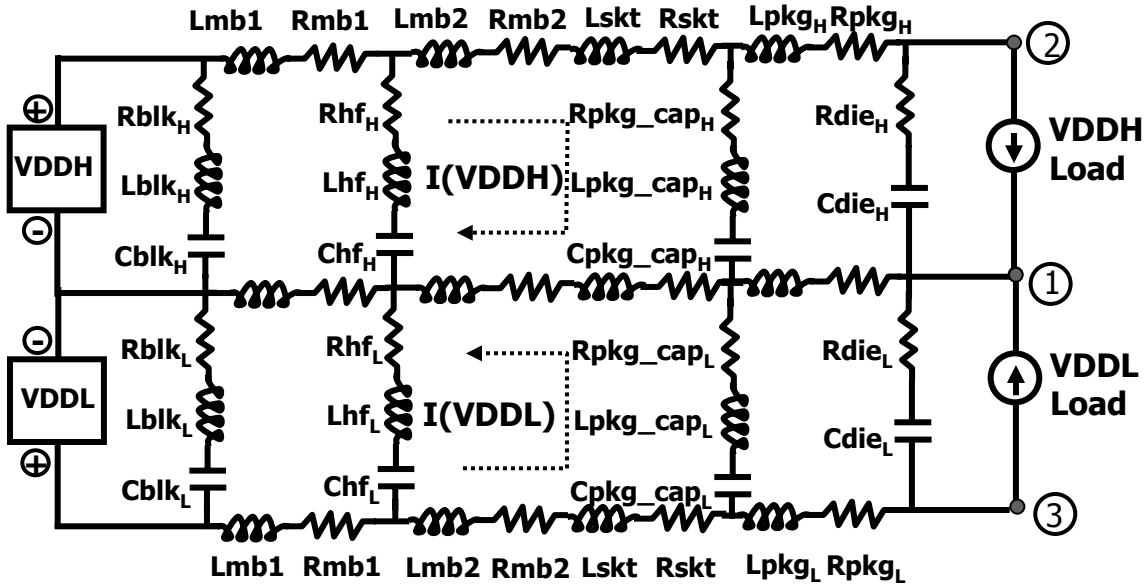
- Electrical model



Intel, “Intel Pentium 4 processor in the 432 pin/Intel 850 Chipset Platform,” 2002.

Package level results

- Two VRMs on board to supply VDDL and VDDH
- Ground path can be shared by VDDL and VDDH
- Decoupling capacitance divided in the ratio of current loads



			VDD or VDDH & VDDL		GND	
			PK	QS	PK	QS
Single-VDD	VDD	mV	92.7	65.0	92.7	65.0
		%	7.7	5.4	7.7	5.4
Dual-VDD	VDDH	mV	63.0	34.0	68.9	40.7
		%	5.3	2.8	5.7	3.4
VDDL = 0.6V	VDDL	mV	18.0	9.0	68.9	40.7
		%	3.0	1.5	11.5	6.8
Dual-VDD	VDDH	mV	63.0	32.0	77.8	46.0
		%	5.3	2.7	6.5	3.8
VDDL = 0.8V	VDDL	mV	37.0	18.0	77.8	46.0
		%	4.6	2.3	9.7	5.7

- Similar power supply noise with same resources (decap, C4) as single-VDD case

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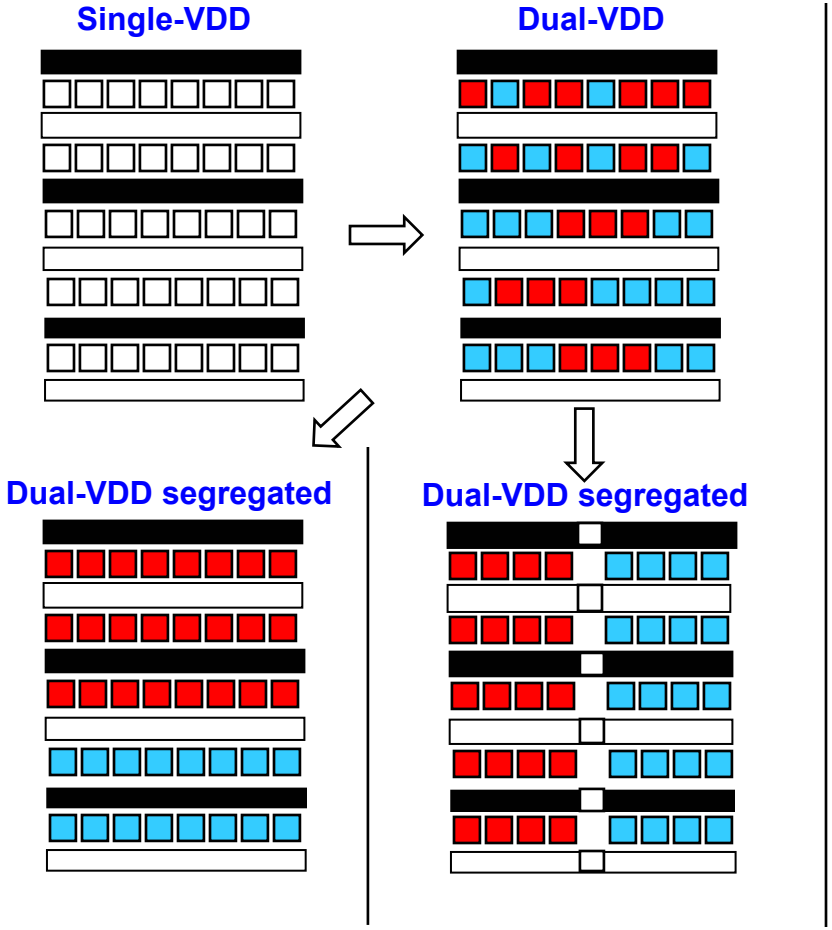
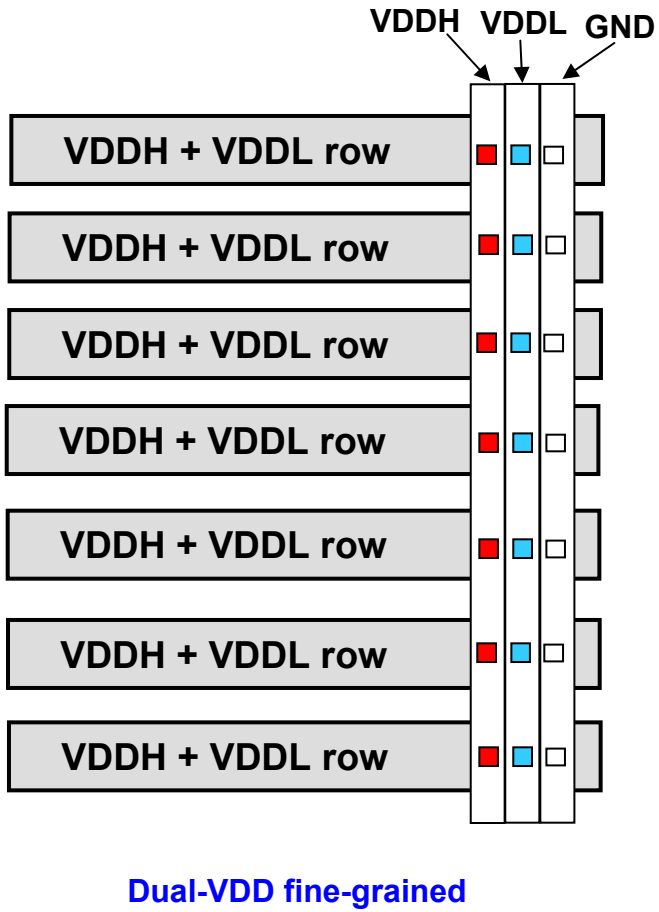
Dual-VDD physical design alternatives





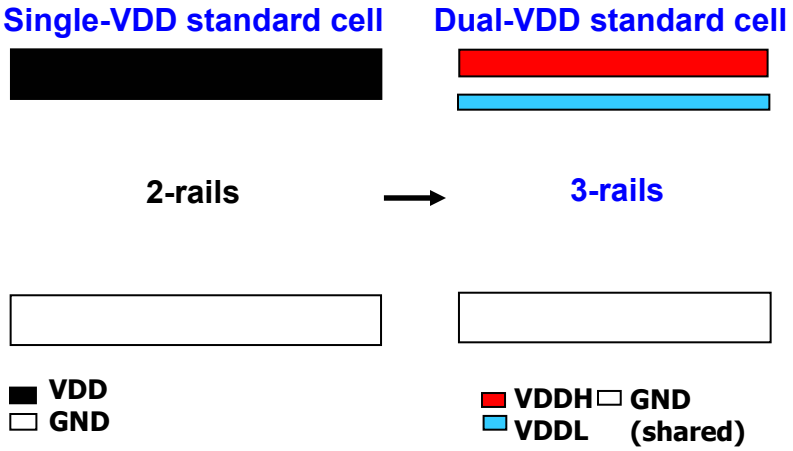
Dual-VDD fine-grained

Segregated placement constrains placer leading to higher core-area and wirelength

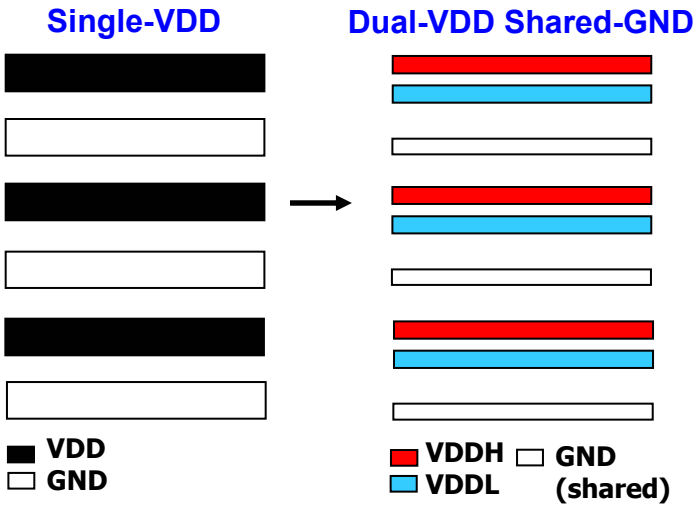
C. Yeh, *et al.*, "Layout techniques supporting the use of dual supply voltages for cell-based designs," *Proc. DAC*, 1999.
M. Igarashi, *et al.*, "A low-power design method using multiple supply voltages," *Proc. ISLPED*, 1997.

Unconstrained dual-VDD placement

- Multi-rail standard cells



- Grid texture



Dual-VDD power grid design

- Important while designing the dual-VDD grid:
  - Scale wires with respect to the single-VDD considering how the current demand has scaled
  - VDDL gates more sensitive to grid noise $\Rightarrow$ important as ground is shared
    - 120mV noise is 10% for a 1.2V gate, but 15% for a 0.8V gate
    - 7% higher delay for a 1.2V gate, but 16% for a 0.8V gate
  - Placement of VDDL and VDDH gates $\Rightarrow$ assign more wiring resources to VDDL grid in areas where there is more demand for VDDL current
  - Consider effects that arise from the board and package level such as shared C4s
    - Fewer C4s leads to higher effective package R, L

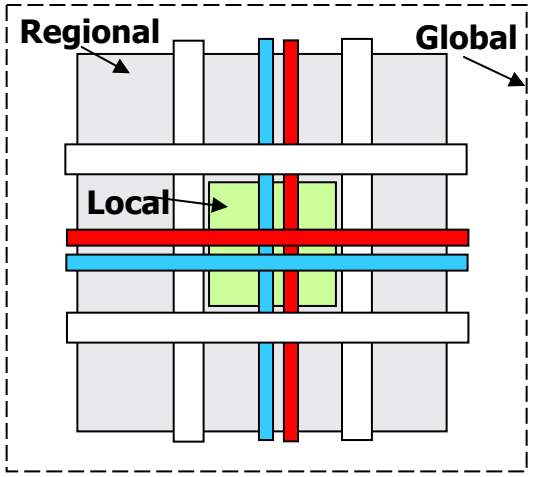
Proposed technique (D-Place)

- Let α = I(VDDH)/I(VDD) and β = I(VDDL)/I(VDD)
- Scale wires as follows $W_{VDDH} = \alpha W$

$$W_{VDDL} = \beta \frac{VDDH}{VDDL} W$$

$$W_{GND} = (\alpha + \beta) \frac{VDDH}{VDDL} W$$

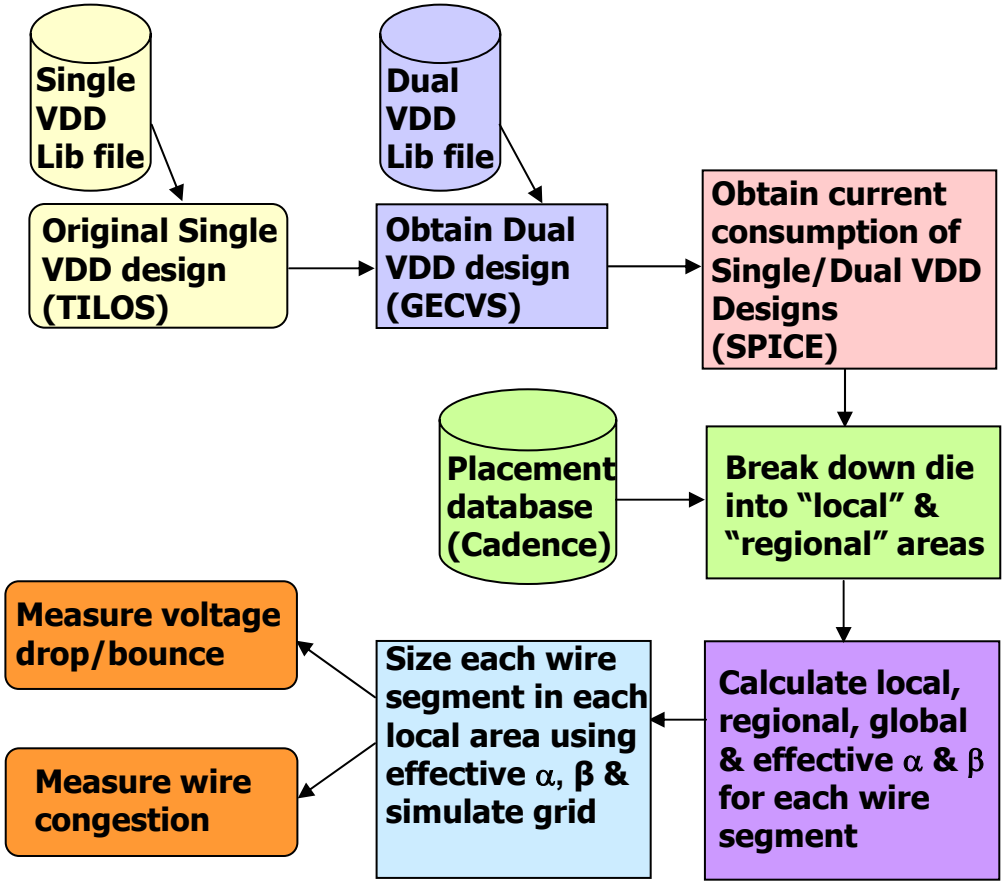
- Partition the chip floorplan



- Obtain effective α and β as:

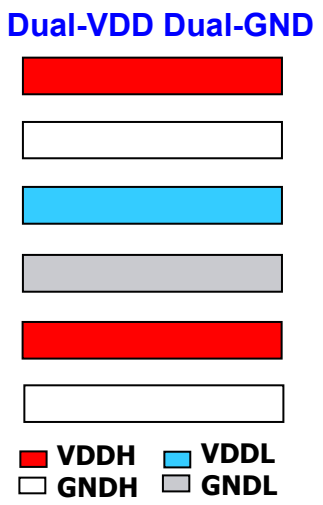
$$\alpha_{effective} = \frac{\alpha_{local} + \alpha_{regional} \frac{Area_{local}}{Area_{regional}} + \alpha_{global} \frac{Area_{local}}{Area_{global}}}{1 + \frac{Area_{local}}{Area_{regional}} + \frac{Area_{local}}{Area_{global}}}$$

Design flow

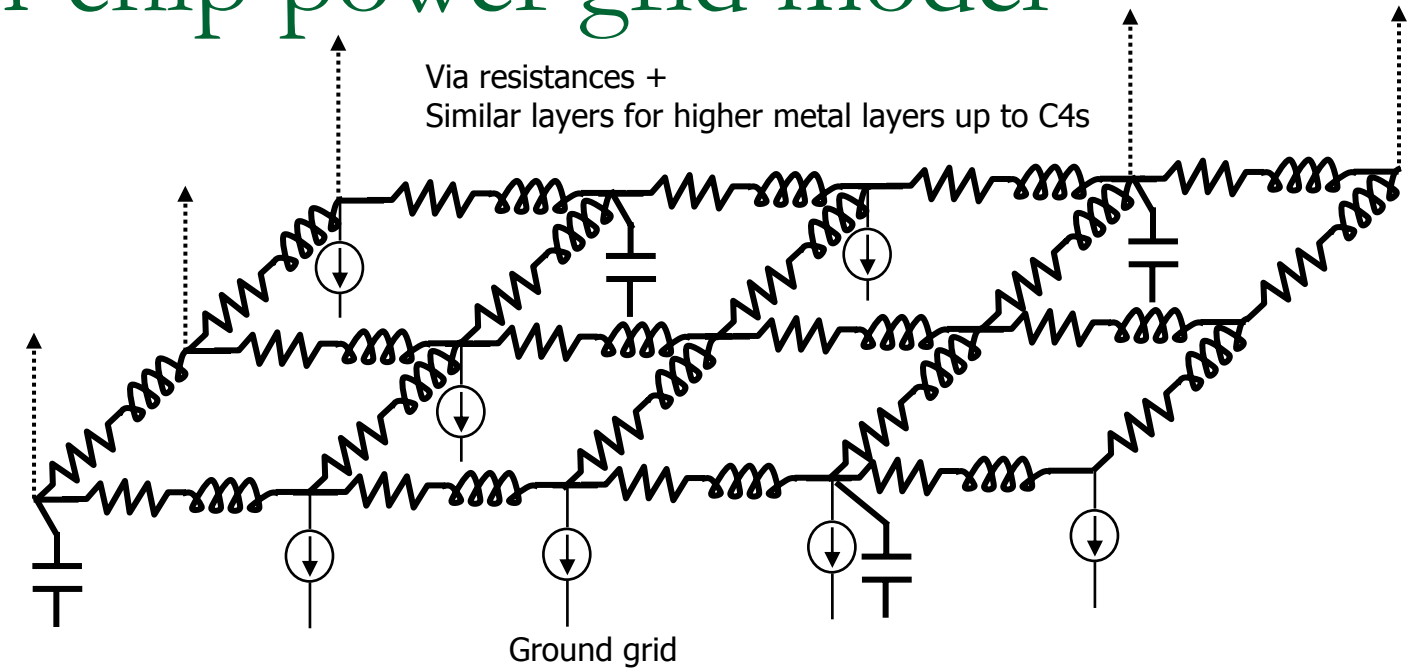

Single VDD Lib file
Dual VDD Lib file
Original Single VDD design (TILOS)
Obtain Dual VDD design (GECVS)
Obtain current consumption of Single/Dual VDD Designs (SPICE)
Placement database (Cadence)
Break down die into "local" & "regional" areas
Measure voltage drop/bounce
Measure wire congestion
Size each wire segment in each local area using effective α, β & simulate grid
Calculate local, regional, global & effective α & β for each wire segment

Prior work

- Dual-VDD and Dual-GND:
  - Requires two separate grounds off-chip
  - Complicates timing analysis and design of the board
  - M. Popovich *et al.*, *GLVLSI*, 2005.
  - (DVDG)
- Dual-VDD and Shared-GND:
  - C. Yeh *et al.*, *DAC*, 1999
  - (D-Vanilla)



On-chip power grid model



- 3-D PEEC model
- Wires fractured and represented by RLC models
- Modeled area about 0.5mm^2 (600,000 R/L/C elements)

C. Hoer and C. Love, “Exact inductance equations for rectangular conductors with applications to more complicated geometries,” *J. Res. Nat. Bureau Stds.*, 1965.
S. C. Wong, *et al.*, “Modeling of interconnect capacitance, delay and crosstalk in VLSI,” *IEEE Trans. Sem. Manuf.*, 2000.

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Peak voltage drop comparisons

VDDL = 0.6V

		Single VDD	DVDG	D-Vanilla	D-Place
c880	MAX	16.9%	30.9%	16.4%	18.6%
	AVG	9.5%	14.7%	9.6%	9.5%
c2670	MAX	25.6%	35.5%	32.2%	25.5%
	AVG	15.9%	19.8%	15.2%	14.5%
c5315	MAX	29.6%	38.2%	37.4%	32.0%
	AVG	21.6%	23.4%	20.2%	19.8%
c7552	MAX	26.8%	34.2%	34.5%	29.4%
	AVG	22.2%	21.0%	21.1%	18.7%

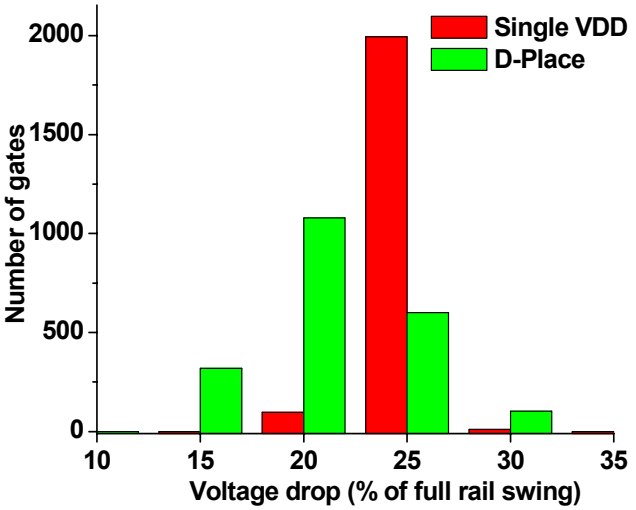
VDDL = 0.8V

		Single VDD	DVDG	D-Vanilla	D-Place
c880	MAX	16.9%	30.3%	16.3%	19.5%
	AVG	9.5%	15.9%	9.7%	9.8%
c2670	MAX	25.6%	36.1%	27.6%	27.0%
	AVG	15.9%	22.1%	15.8%	15.3%
c5315	MAX	29.6%	38.1%	33.0%	31.8%
	AVG	21.6%	25.4%	20.1%	20.3%
c7552	MAX	26.8%	31.4%	31.6%	28.7%
	AVG	22.2%	24.9%	22.3%	20.1%

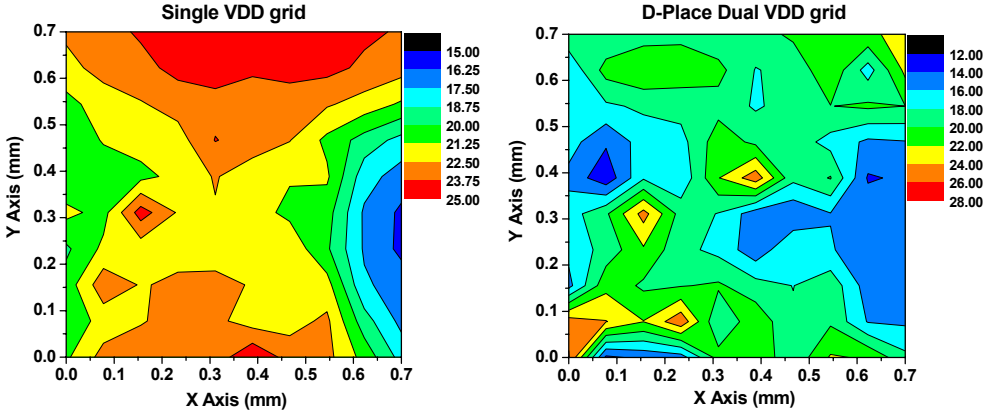
- D-Place similar to single-VDD grids in AVG cases
- Inferior by < 2.6% (≈15mV) in some MAX cases
- 0.6V VDDL as robust as 0.8V
- 0.6V also provides higher power savings
- Proposed approach better by 2-7% (AVG) and 7-12% (MAX) compared to prior approaches

Voltage variation across die

- Gate-level statistics
  - Few gates worse but many better off
  - Favorable for circuit timing



- Voltage drop contours



Dual-VDD grid as robust as single-VDD grid

Additional comparison metrics

- Wire congestion

	Single	DVDG		D-Vanilla		D-Place	
	VDD	0.6V	0.8V	0.6V	0.8V	0.6V	0.8V
c880	0.17	0.17	0.17	0.19	0.20	0.17	0.16
c2670	0.17	0.17	0.17	0.19	0.20	0.16	0.16
c5315	0.17	0.17	0.17	0.19	0.20	0.18	0.16
c7552	0.17	0.17	0.17	0.19	0.20	0.15	0.15

  - Comparable to single-VDD as wires are scaled in proportion to lowered current demand

- Maximum voltage variation across die

	Single	DVDG		D-Vanilla		D-Place	
	VDD	0.6V	0.8V	0.6V	0.8V	0.6V	0.8V
c880	10.4%	24.5%	21.1%	11.2%	11.0%	13.8%	13.5%
c2670	14.9%	26.6%	25.2%	26.3%	22.4%	18.7%	19.7%
c5315	13.7%	28.2%	23.8%	28.4%	22.6%	21.9%	20.2%
c7552	10.8%	19.9%	16.3%	24.5%	23.9%	19.1%	18.3%

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Summary

- Demonstrated the feasibility of power delivery for dual-VDD circuits
- Leveraged the observation that dual-VDD circuits have significantly lower supply current demands
- Addressed board and package level issues
- Proposed an improved method for designing on-die grids

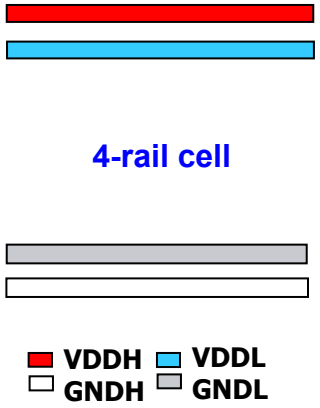
Questions

Thanks!

Simulation setup

- CMOS process: 1.2V, 0.13μm, dual-Vth, 6 metal layers
- Voltage assignment scheme:
  - Fine-grained (ECVS) based algorithm
  - Asynchronous level converters used
- VDDL = {0.6V, 0.8V}
- VDDH = 1.2V (nominal)
- Standard cell row based layout using Cadence SE

DVDG standard cell



Decap estimation

$$C_{decap} = \frac{\int_0^{\tau} I(t)dt}{V_{noise-\lim}}$$

Scaled decap

	Scaled Decap Dual VDD	
Decoupling Capacitance	Decap (VDDH)	1.02nF (1.06nF)
	Decap (VDDL)	0.91nF (1.30nF)
	Total Decap	1.93nF (2.36nF)
Grid integrity metrics		
	MAX	27.6% (27.0%)
	AVG	16.9% (15.3%)

Dual-VDD level conversion and VDD assignment references

S. H. Kulkarni and D. Sylvester, “High performance level conversion for multi-VDD design,” *IEEE TVLSI*, 2004.
S. H. Kulkarni, *et al.*, “A new algorithm for improved VDD assignment in low power dual VDD systems,” *ISLPED*, 2004.