A New Test and Characterization Scheme for 10+ GHz Low Jitter Wide Band PLL

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Outline of Presentation

- Objectives
- PLL Basic Attributes
- Process Technology Overview
- Proposed Test and Characterization Scheme
  - VCO Frequency Range Measurement
  - Duty Cycle Measurement at Level Shifter Circuit
- Conclusion

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Objectives

- Design a new test scheme for a high performance PLL
  - Without additional jitter penalty
  - Short measurement time for manufacturing
  - Integrated PLL reset function
- Design a new characterization scheme for level shifter circuits
  - Duty cycle measurement at +4.0 GHz clock
  - General environment for measurement
  - High accuracy
  - Pick optimum level shifter circuit

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PLL Basic Attributes

- Max VCO Frequency in Locked Condition :
  - 21.424GHz
- VCO Frequency (Lock) at Low Voltage :
  - 6.6 GHz @ 0.804V
  - 10.0 GHz @ 0.957V
- Minimum Cycle-Cycle Jitter :
  - 9.48 ps P- P
  - 1.09 ps RMS
- Temperature Sensitivity (df / dT) :
  - ~ -0.1 % / deg C
- Average Power :
  - < 20 mW
- cf. 2004 VLSI Circuits Paper C15.1

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Process Technology Overview

- **90nm PD-SOI CMOS process**
  - **Twin-well CMOS on P^- SOI substrate**
  - **Standard digital process**
  - **L_{eff} < 50 nm (nominal)**
  - **Dual gate oxide thicknesses**
    - **Thin oxide: T_{inv} ~ 1.95 nm**
    - **Thick oxide: T_{inv} ~ 3.1 nm**
- **Refer to 2004 VLSI Technology paper T10.2,**
  2002 IEDM paper 16.1.1

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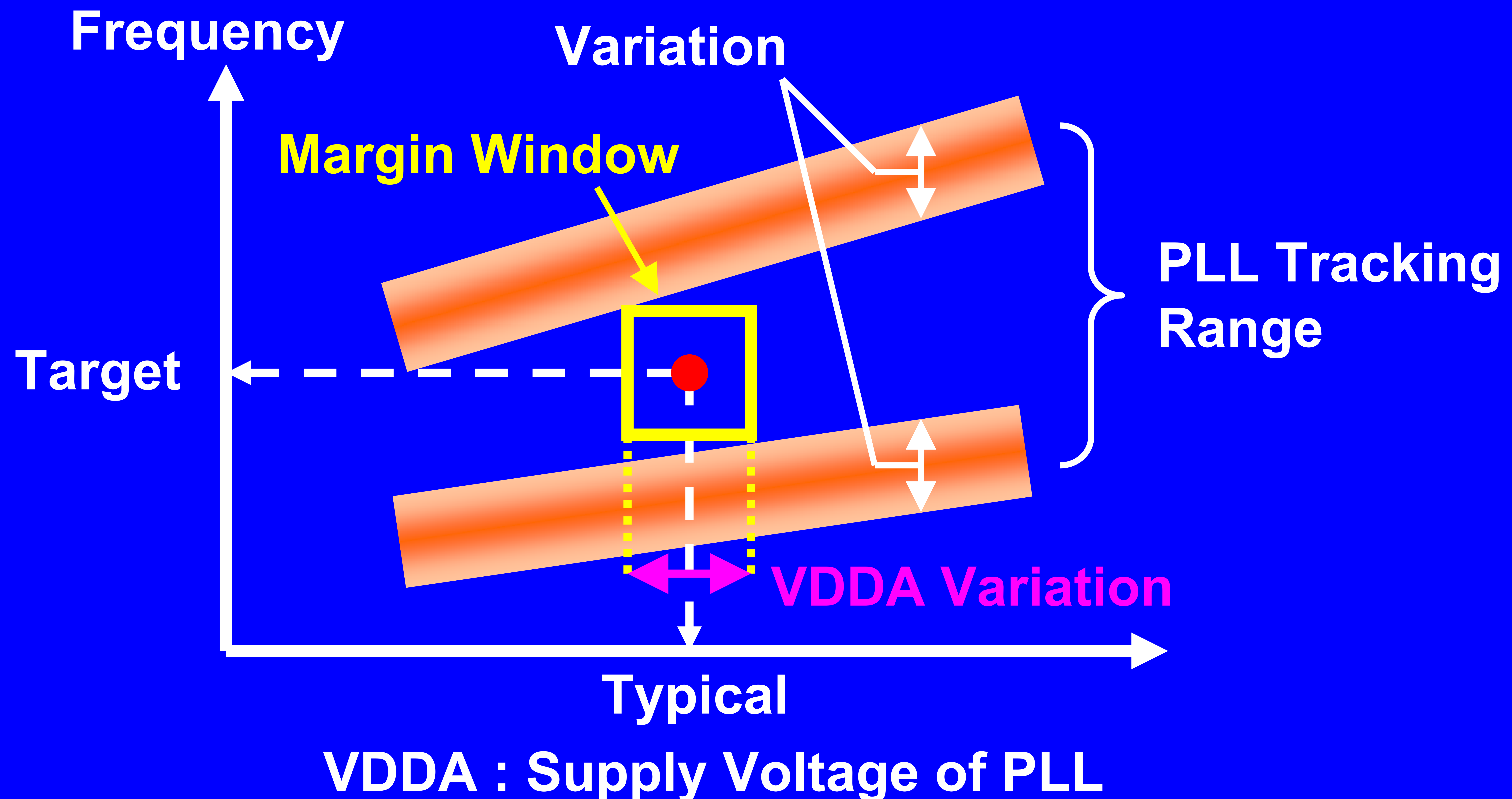
PLL Tracking (Lock) Range

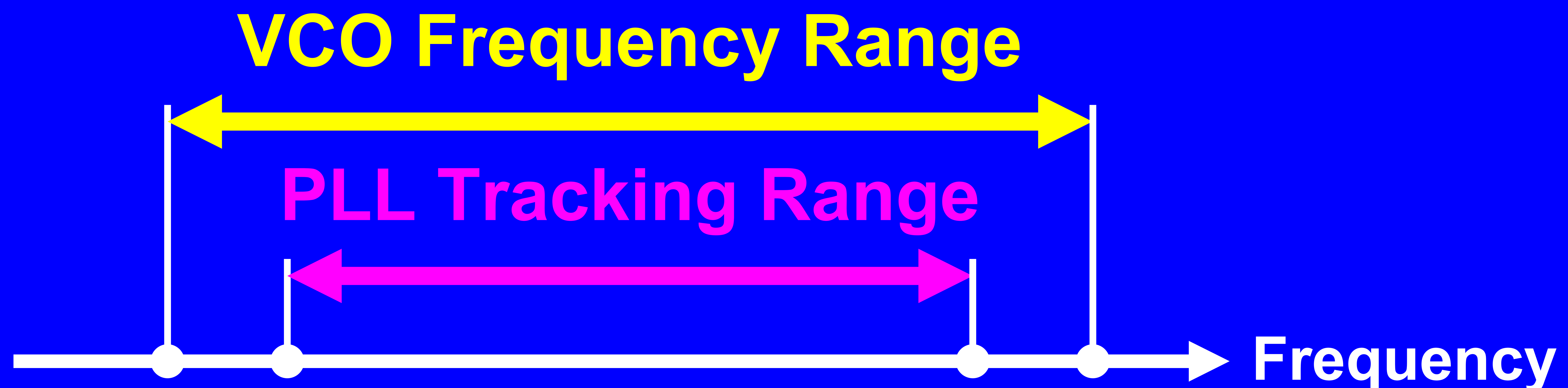
- Important attribute of PLL for acquisition of lock
- Closely related with PLL yield



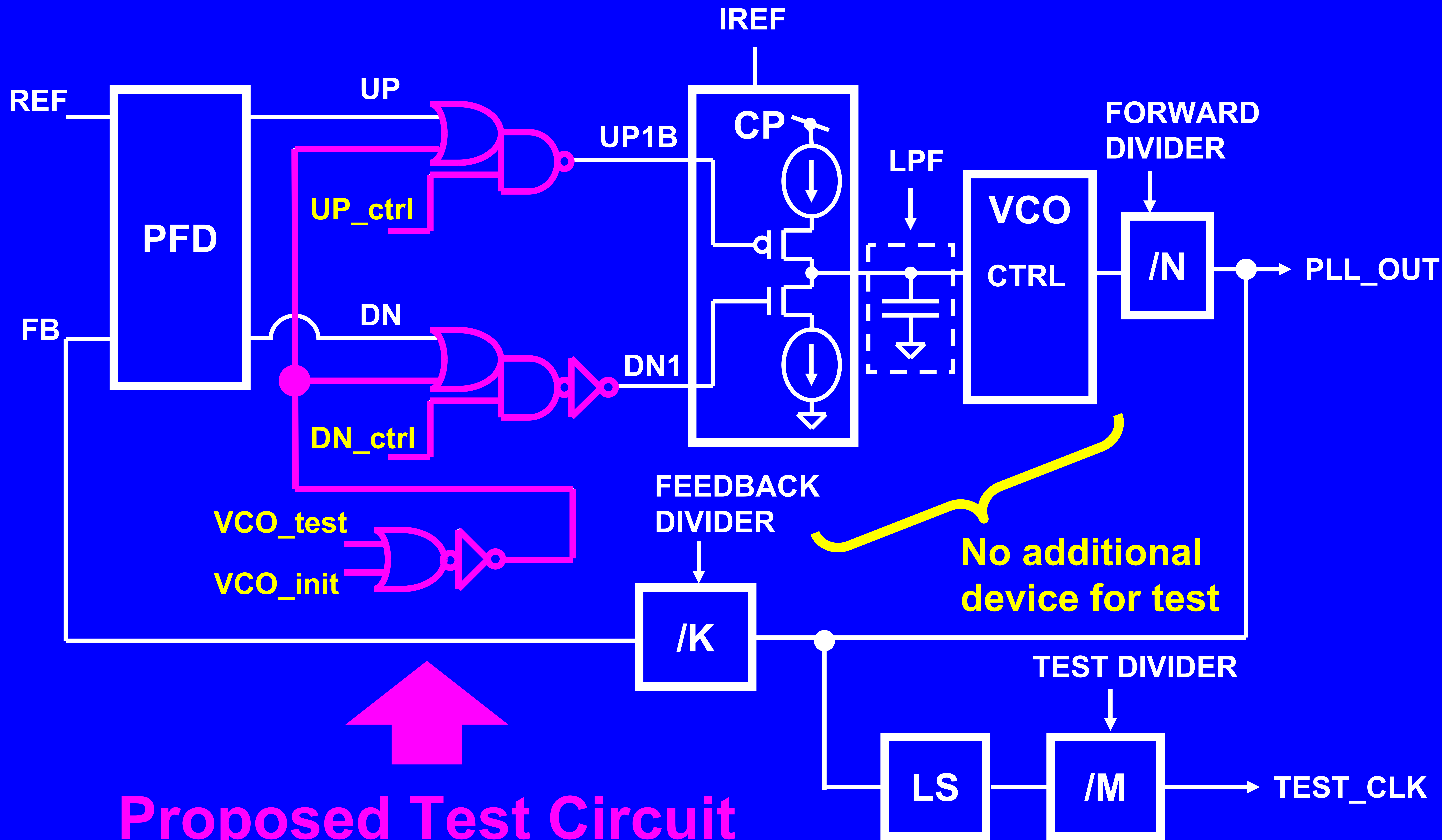
VDDA : Supply Voltage of PLL

Test for Screening PLL

- Not easy to measure PLL tracking range
  - Need to wait until PLL is locked
  - Need to change a frequency of reference clock every measurement
  - Difficult to define locked condition
- VCO frequency range can be easily measured by proposed test scheme.



PLL with VCO Test Mode



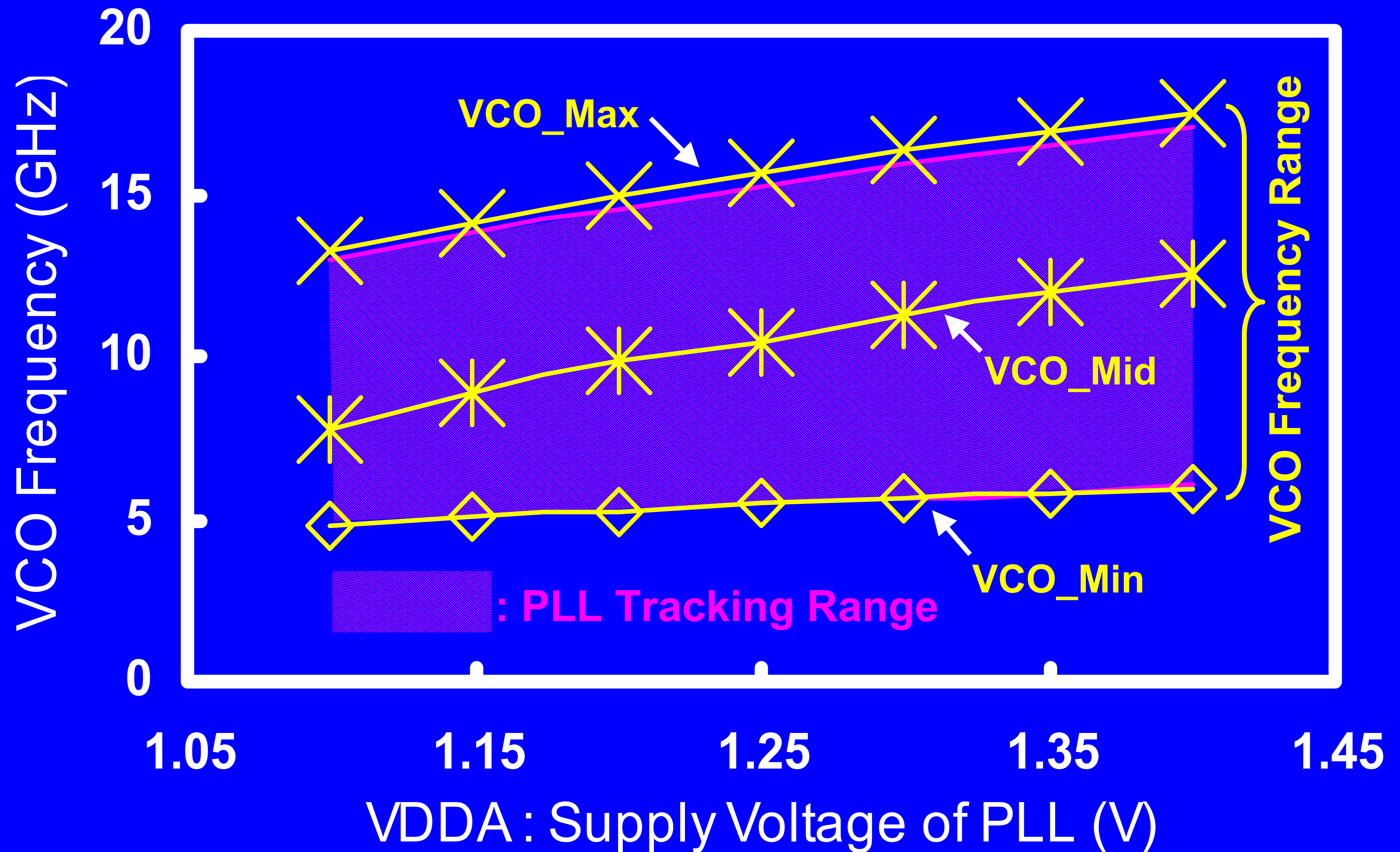
LS : Level Shifter

Truth Table of PLL Operating Mode

	Normal Function	PLL Reset Function	VCO Test Mode		
VCO_init	L	H	*		
VCO_test	L	*	H		
UP_ctrl	H	L	L	H	H
DN_ctrl	H	H	H	H	L
PLL_OUT	Target Frequency	Minimum Frequency	Minimum Frequency	Middle Frequency	Maximum Frequency

* : don't care

PLL Tracking Range and VCO Frequency Range



Advantages of Proposed Test Scheme

- VCO frequency range, that is close to PLL tracking range, is easily measured.
  - Suitable for screening PLL on manufacturing
- Middle frequency of VCO is observed.
  - Indicator of VCO gain and device quality

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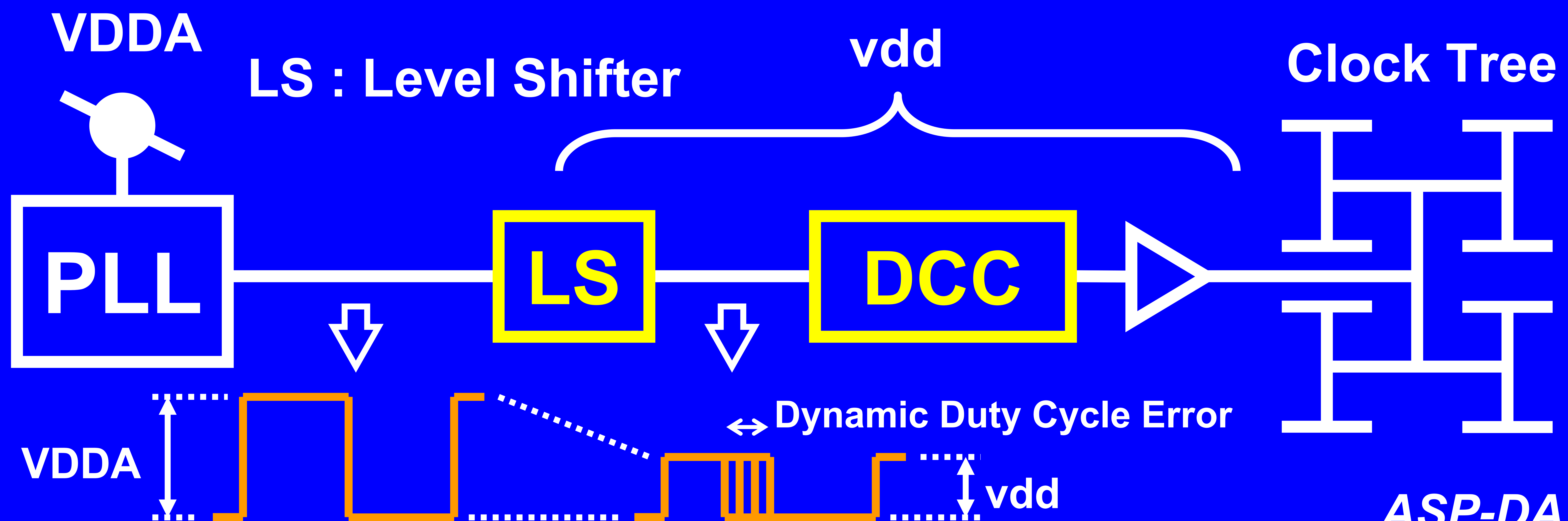
Duty Cycle of System Clock

- Duty cycle of system clock is important for the maximum operating frequency.
- Duty Cycle Correction (DCC) circuit is implemented.
  - Static Correction
- However, Level Shifter (LS) circuit causes dynamic duty cycle error because vdd changes dynamically.



Success of Duty Cycle Measurement on Unpackaged Die at 4.2GHz

This phase difference is equal to the pulse width of CLK.

CLK : 4.2GHz (119ps)

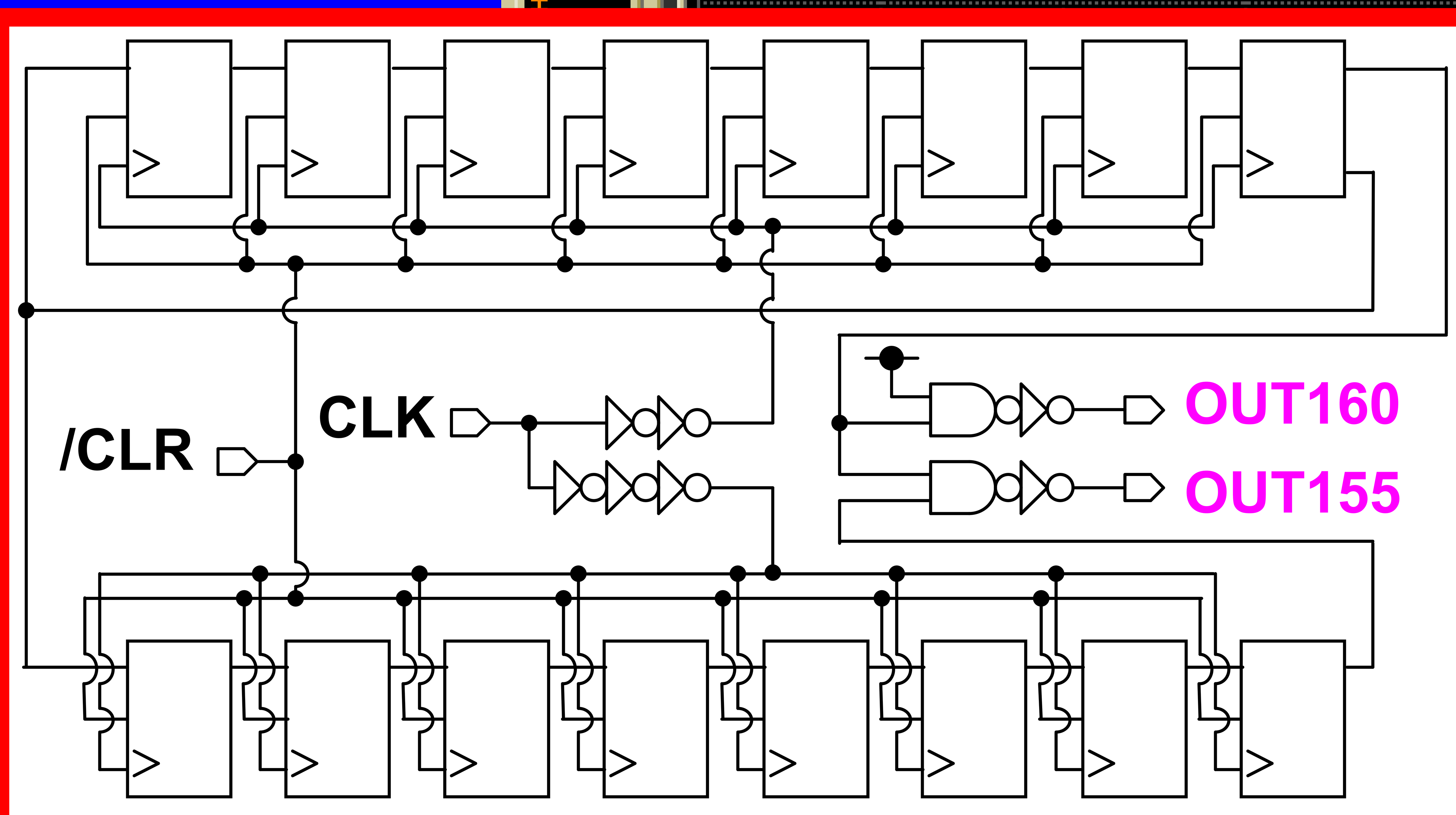
OUT160 : 262.5MHz (3.8ns)

CLK divided by 16

OUT160

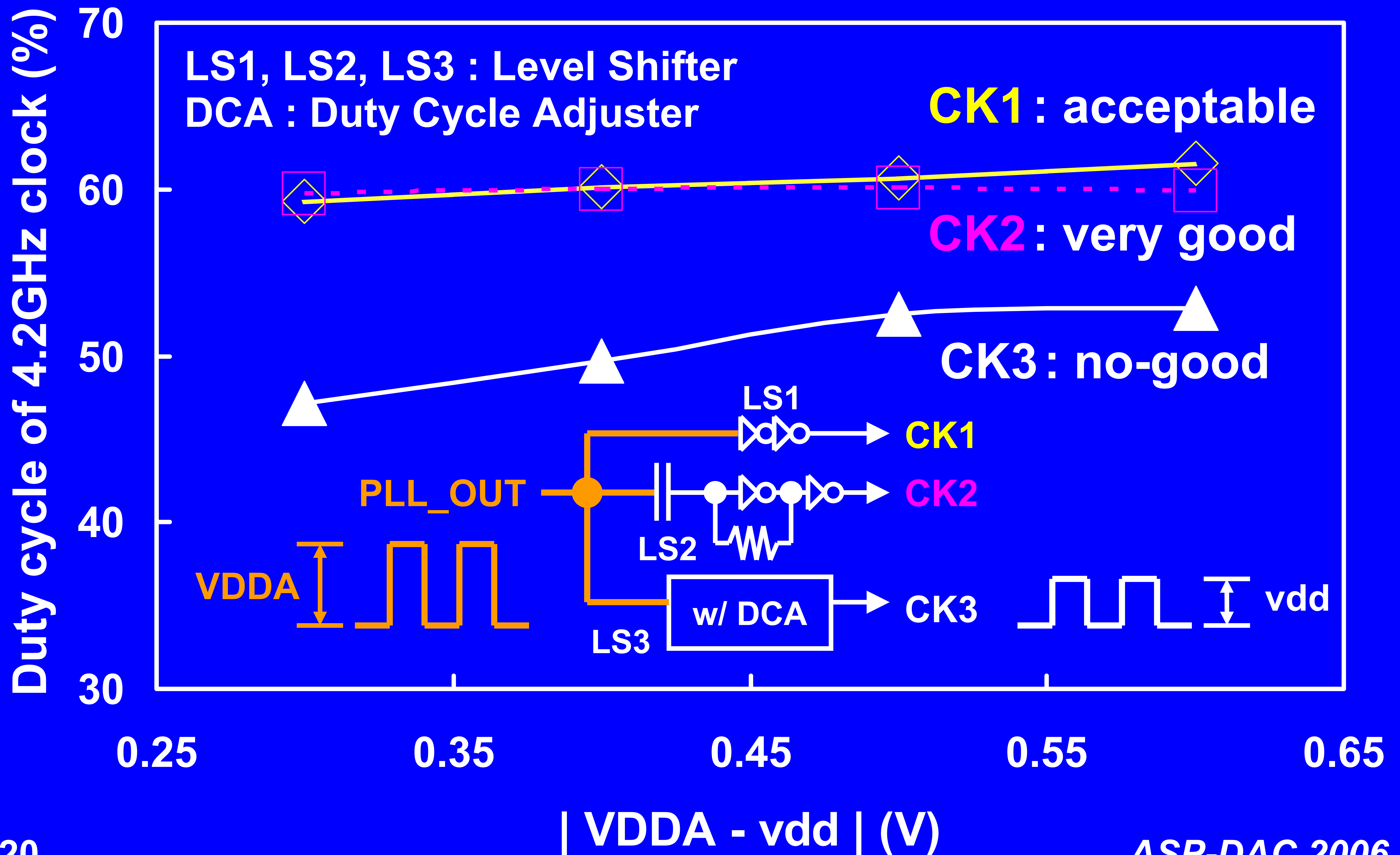
OUT155

500ps



Proposed circuit for duty cycle measurement

Characterization Results on Unpackaged Die at 4.2GHz



Advantages of Proposed Characterization Scheme

- Measure duty cycle of high frequency clock on unpackaged die
- Measured pulse width :
  - < 120ps
- Check duty cycle error that depends on voltage difference between VDDA and vdd at level shifters
  - Pick optimum level shifter circuit

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Conclusion

- New Test Scheme for PLL
  - Without additional jitter penalty
  - Predict PLL tracking range
  - Be used on manufacturing
- New Characterization Scheme for Clock
  - Be used in a general environment for measurement
  - Measure duty cycle at 4.2GHz
  - With high accuracy

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