Parameterized Block-Based Non-Gaussian Statistical Gate Timing Analysis

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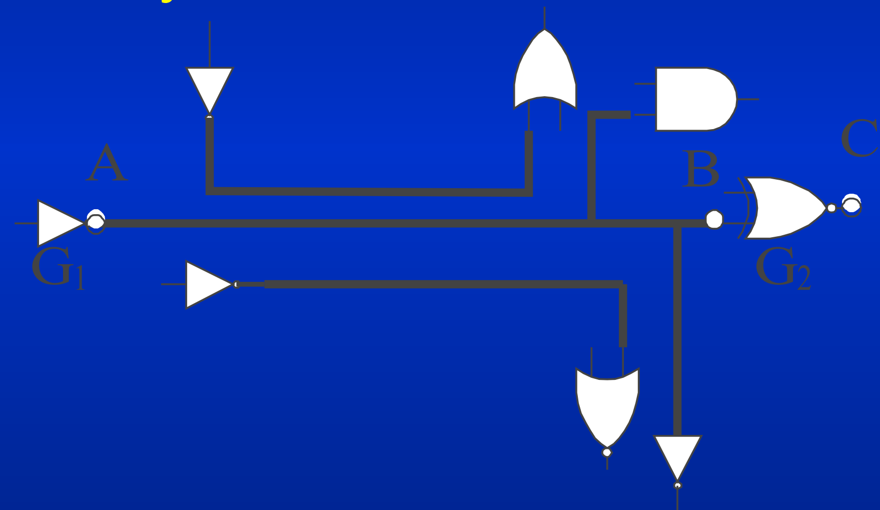
Asia and South Pacific Design Automation Conference
Jan 27th, 2005

Outline

- Introduction
- Motivation
- Variational Gate Timing Analysis
- Experimental Results
- Conclusion and Future Work

Circuit Delay

- Circuit delay in VLSI circuits consists of two components:
  - Interconnect propagation delay
    - Elmore
    - D2M
    - AWE
  - Gate propagation delay
    - Total Capacitance
    - Effective Capacitance

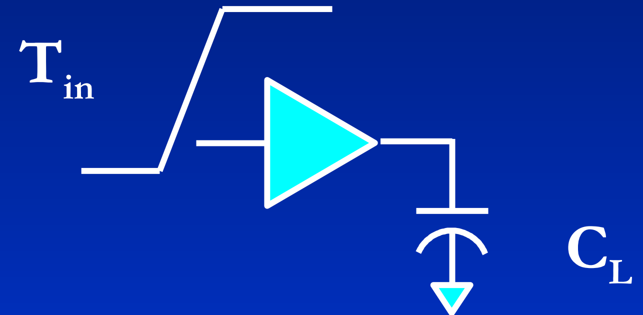


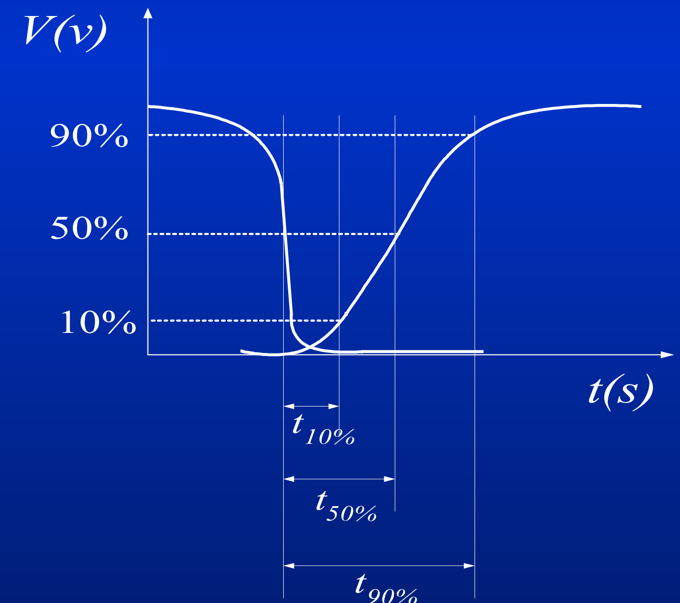
Total Capacitance Approach

- For commercial ASIC cell libraries, it is common to characterize various output transition times as a function of the input transition time and output capacitance i.e.,

$$t_{\alpha}^{gate} = f_{\alpha}^{gate}(T_{in}, C_L)$$

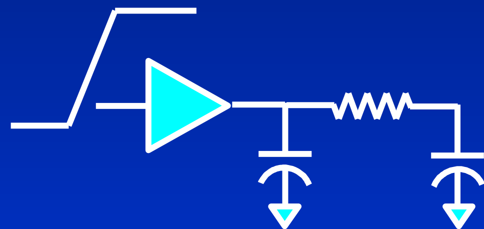
  - α% denotes the percentage of the output transition,
  - t_{α} is the output delay with respect to the 50% point of the input signal,
  - f_{α} is the corresponding delay function.





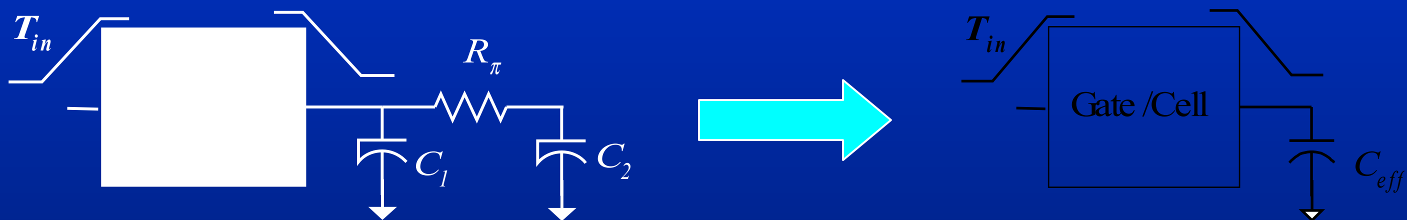
Effective Capacitance Approach

- Second order RC-π model



RC-π load for effective capacitance algorithms

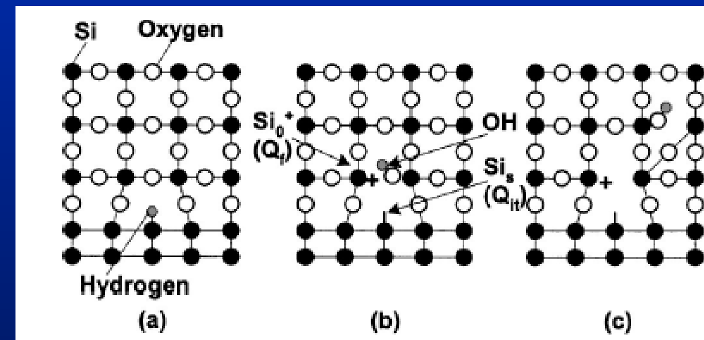
- Iterative effective capacitance algorithm



$$C_{eff} = C_1 + kC_2 \quad \text{where} \quad 0 \leq k \leq 1$$

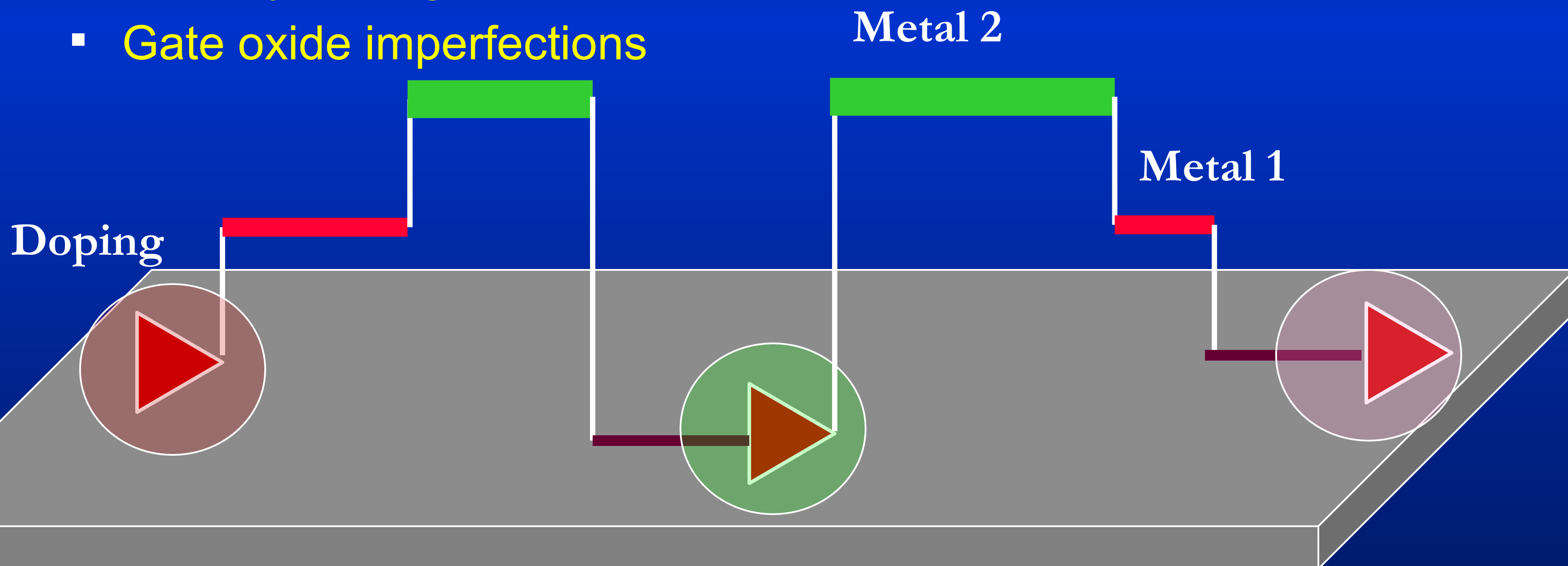
UDSM Designs and Parameter Variations

- Circuit variability is increasing in UDSM
- Types of circuit variability
  - Intrinsic variation caused by the IC manufacturing process
    - Systematic variation (known quantitative relationship)
      - Leff
    - Random variation (uncertain)
      - Gate oxide thickness
      - Channel doping
      - ILD permittivity
  - Extrinsic variation caused by the operational environment
    - Long term variation
      - Negative Biased Temperature Instability
      - Hot Carrier Effect
    - Short term variation
      - Vdd variation
      - Temperature variation
      - L/C coupling effects



σTA: Sources of Variations

- Global Sources of Variation (X_i)
  - Metal Layer Width Variation
  - Vdd Variation
- Independent Random Sources of Variation (S)
  - Impurity doping deviations
  - Gate oxide imperfections



Non-Gaussian Sources of Variations

- Sources of variation may exhibit non-Gaussian distributions
- Using the first three moments of the parameters variations to approximate the process variation
- Skewness: The degree of asymmetry of a distribution (κ)

$$\kappa = \frac{\mu_3}{\sigma^3}$$

μ_3 is the 3rd central moment

σ^2 is the second central moment

Canonical First-Order (CFO) Model for Timing Parameters

- In block-based σTA, any timing quantity (slew, delay, slack, arrival times) is modeled as follows:

$$A = a_0 + a_1 \Delta X_1 + a_2 \Delta X_2 + \ldots + a_n \Delta X_n + a_{n+1} \Delta S_a$$

  - "a_0" is the mean or nominal value,
  - "n" represents n global sources of variation,
  - "ΔX_i" is the ith global source of variation with ***Dist***$(\mu=0, \sigma^2=1, \kappa)$
  - "ΔS_a" is the independent random source of variation ***Dist***$(\mu=0, \sigma^2=1, \kappa)$
  - "a_i" is the sensitivity of A to corresponding source of variation.

CFO Model for Interconnect Electrical Parameters

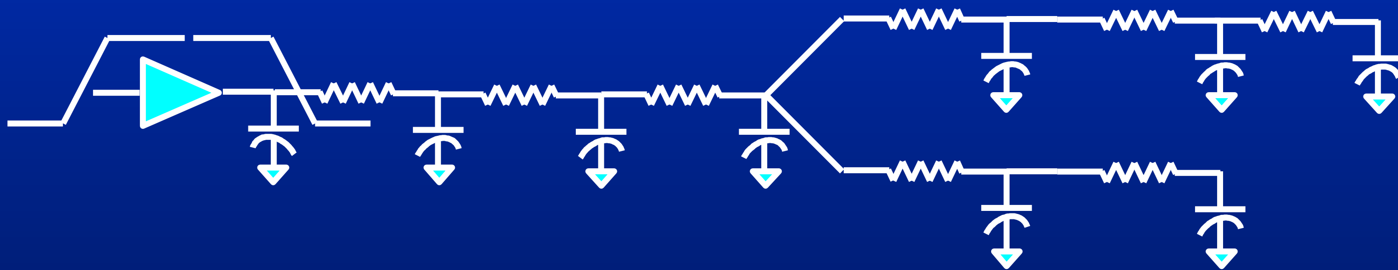
- We may present electrical parameters of the wire (i.e., R and C) in the CFO form. For example;

$$R = r_{nom} + r_1 \Delta X_1 + r_2 \Delta X_2 + \ldots + r_n \Delta X_n + r_{n+1} \Delta S_r$$

  - "r_{nom}" is the nominal resistance value,
  - "n" represents n global sources of variation,
  - "ΔX_i" is the ith global source of variation with $\boldsymbol{Dist}(\mu=0, \sigma 2=1, \kappa)$
  - "ΔS_r" represents the independent random source of variation for resistance with $\boldsymbol{Dist}(\mu=0, \sigma 2=1, \kappa)$
  - "r_i" is the sensitivity of R to the corresponding source of variation.

Problem Statement

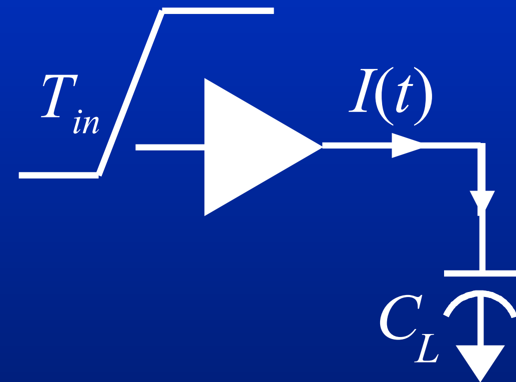
- Given that
  - each *R* and *C* is in CFO form,
  - gate input transition time is in CFO form,
  - gate itself experiences parameter variations.
- The objective is to find the
  - Gate delay in the CFO form,
  - Gate output slew in the CFO form.



Variational Total Capacitive Load Model

- Given is a variational CMOS driver where
  - input rise time, T_{in}, is in CFO form,
  - output capacitive load, C_L, in the CFO form.

- The objective is to find
  - gate propagation delay in CFO form,
  - output slew in the CFO form.



Solution

- The gate propagation delay is a function of:

$$T_\alpha = f_\alpha\left(T_{in}, C_L, z\right) \text{ where } z = \left\{\frac{W}{L}, V_T, V_{dd}, Temp, \ldots\right.$$

- α denotes the percentage of the output transition,
- T_α is the output delay with respect to 50% point of the input signal,
- f_α is the corresponding delay function,
- z denotes the parameter set associated with the gate.

Solution (Cont'd)

- Substitute the terms with their corresponding CFO models.
- Differentiate with respect to the global and independent random sources of variation:

$$T_\alpha = f_\alpha\left(\Delta X_i\big|_{i=1\ldots m}, \Delta S_j\big|_{j=1\ldots p}\right)$$

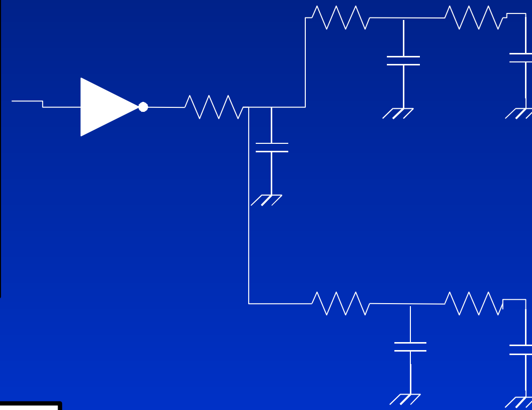
$$T_\alpha \cong f_\alpha\Big|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} + \sum_{i=1}^{m}\left(\frac{\partial f_\alpha}{\partial \Delta X_i}\Bigg|_{\substack{\Delta X_l=0\\ \Delta S_k=0}}\right)\Delta X_i + \sum_{j=1}^{p}\left(\frac{\partial f_\alpha}{\partial \Delta S_i}\Bigg|_{\substack{\Delta X_l=0\\ \Delta S_k=0}}\right)\Delta S_j$$

- Considering ΔS_j's as independent unit normal sources of variations, we get

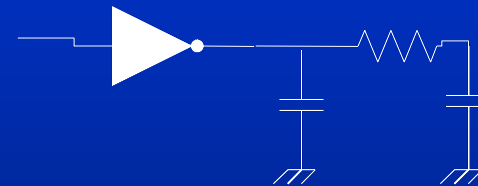
$$T_\alpha \cong f_\alpha\Big|_{\substack{\Delta X_l=0\\ \Delta S_k=0}} + \sum_{i=1}^{m}\left(\frac{\partial f_\alpha}{\partial \Delta X_i}\Bigg|_{\substack{\Delta X_l=0\\ \Delta S_k=0}}\right)\Delta X_i + \sqrt{\sum_{j=1}^{p}\left(\frac{\partial f_\alpha}{\partial \Delta S_i}\Bigg|_{\substack{\Delta X_l=0\\ \Delta S_k=0}}\right)^2}\;\Delta S_{t_\alpha}$$

Variation-Aware Gate Timing Analysis Algorithm

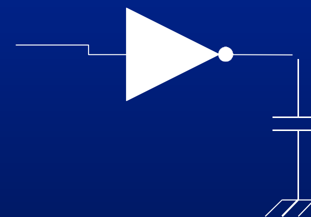
Calculate a **variational RC-π** model for the gate load



Replace the **variational RC-π load** with the equivalent **variational C_{eff}** value



Calculate the **variational gate delay/slew**

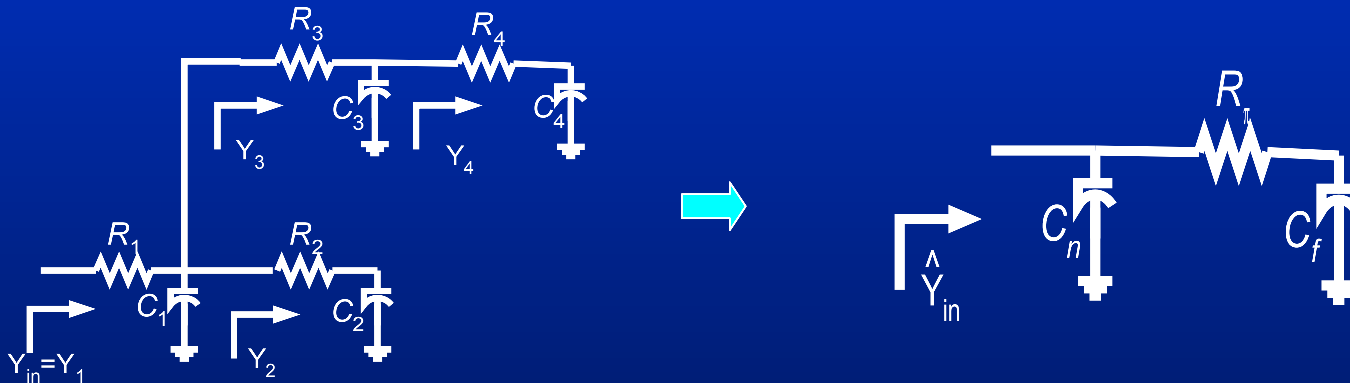


RC-π Load in CFO Form

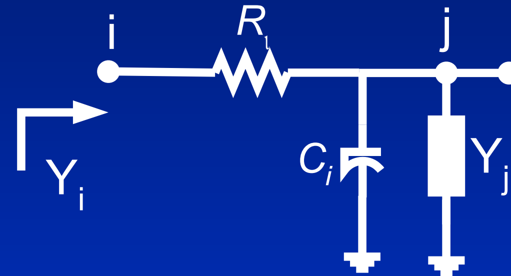
- In STA, by matching the first, second, and third moments of the admittance, we have:

$$C_n = Y_{1,in} - \frac{Y_{2,in}^{2}}{Y_{3,in}} \qquad R_\pi = -\frac{Y_{3,in}^{2}}{Y_{2,in}^{3}} \qquad C_f = \frac{Y_{2,in}^{2}}{Y_{3,in}}$$

- where $Y_{k,in}$ is the kth moment of the admittance of the real load



RC-π Load in CFO Form (Cont'd)



$$Y_i(s) = sY_{1,i} + s^2Y_{2,i} + \ldots + s^kY_{k,i} + \ldots..$$

$$Y_j(s) = sY_{1,j} + s^2Y_{2,j} + \ldots + s^kY_{k,j} + \ldots..$$

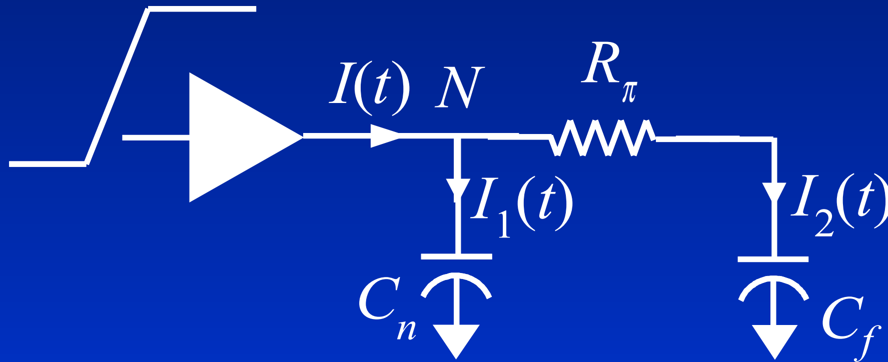
- Then,

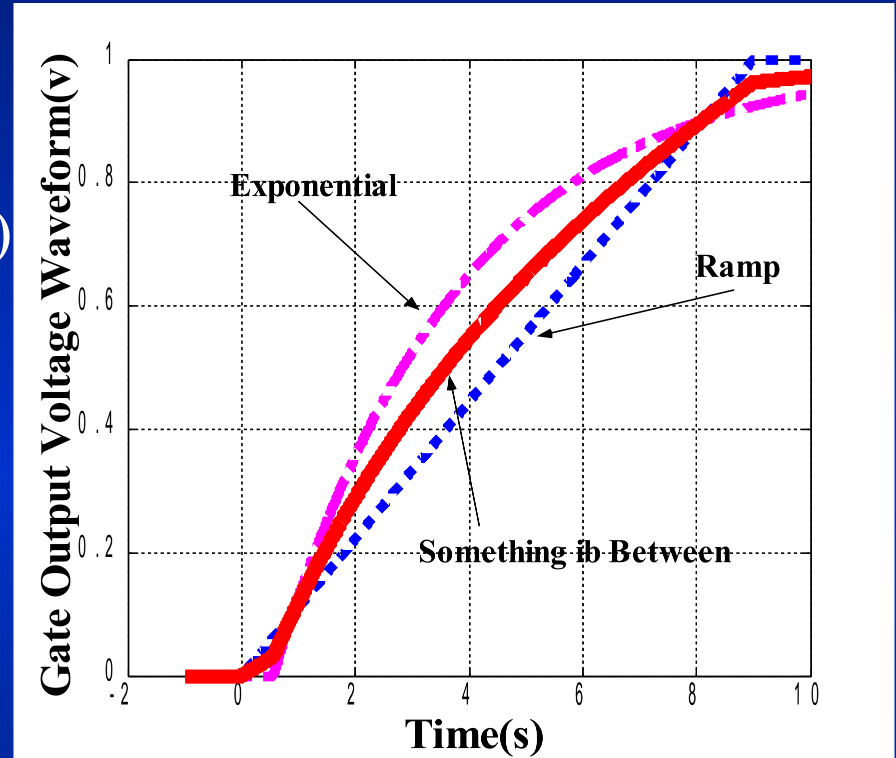
$$Y_{1,i} = Y_{1,j} + C_i$$

$$Y_{k,i} = Y_{k,j} - R_i \sum_{l=1}^{k-1} Y_{l,i}Y_{k-l,j} - R_iC_iY_{k-1,i} \quad for \;\; k \geq 2$$

- Using appropriate CFO forms during the recursive calculation of the admittance moments, we can obtain the π model parameter values in CFO form.

One-iteration C_{eff} Analysis





$$C_{eff}^{Exp}(\theta) = C_n + k_{Exp}(\theta)\, C_f$$

$$C_{eff}^{Ramp}(\theta) = C_n + k_{Ramp}(\theta)\, C_f$$

$$C_{eff}(\theta) = C_n + \left(\zeta\, k_{Exp}(\theta) + (1-\zeta)\, k_{Ramp}(\theta)\right) C_f$$

Calculating C_{eff} in the CFO form using One-iteration approach

$$c_{eff} = c_{eff,0} + \sum_{i=1}^{m} c_{eff,i}\Delta X_i + c_{eff,m+1}\Delta S_{c_{eff}}$$

- Use one-iteration approach to calculate C_{eff} in CFO form
- Find the sensitivities such that

$$E\left[\left(c_{eff} - F\left(t_r, t_{in}, c_{eff}, c_n, r_\pi, c_f\right)\right)^2\right]$$ is minimized

where function F was introduced in one-iteration C_{eff} approach

Experimental Results Setup

- Our experiments use 90nm CMOS process parameters
- Two different configurations
  - two inverters connected in series
    - first inverter size Wp/Wn =30/15μm
    - second inverter Wp/Wn={20/10, 50/25, 70/35, 100/50} μm
  - inverter followed by a 2-input NAND gate
    - first inverter Wp/Wn =30/15μm
    - 2-input NAND gate Wp/Wn={40/40, 50/50, 100/100} μm
- Ramp input to the first inverter
  - nominal value $(t_{in})^{nom}$={10ps,80ps,150ps,220ps,300ps}.

Pure Capacitive Load Results

- Purely capacitive load
  - nominal value $(C)^{nom} = \{400, 500, 800, 1400\} fF$
  - The scaled distribution of the sources of variation is considered to have a skewness of 0.4, 0.6, and 0.8.
- Average error of about 3%
- 89 times faster than Monte Carlo

Pure Capacitive Load Results

Table 1: Average error for the inverter driving pure capacitive load (Skewness=0.4)

	σ=10%		σ=15%	
Average error	**Delay**	**Slew**	**Delay**	**Slew**
Mean	1.5%	1.7%	2.2%	2.3%
Variance	1.2%	1.3%	1.8%	1.9%
Skewness	1.0%	1.1%	1.4%	1.3%

Table 2: Average error for the inverter driving pure capacitive load (Skewness=0.8)

	σ=10%		σ=15%	
Average error	**Delay**	**Slew**	**Delay**	**Slew**
Mean	1.9 %	2.3%	2.5%	2.9%
Variance	1.6%	1.7%	1.9%	2.1%
Skewness	1.4%	1.5%	1.5%	1.9%

Table 3: Average error for the 2-input NAND gate driving pure capacitive load (Skewness=0.6)

	σ=10%		σ=15%	
Average error	**Delay**	**Slew**	**Delay**	**Slew**
Mean	3.0 %	3.1%	3.2%	3.1%
Variance	2.5%	2.7%	2.8%	2.9%
Skewness	2.2%	2.3%	2.5%	2.6%

General RC Load Results

- Nominal value of the total *R* of the load
  - $(R)^{nom}$= {150, 260, 300, 710, 1000}W
- Nominal value of the total *C* of the load
  - $(C)^{nom}$={400, 500, 800, 1400}*fF*.
- The scaled distribution of the sources of variation is considered to have a skewness of 0.5, 0.75, and 1
- An average error of about 6%
- 95 times faster than the Monte Carlo

General RC Load Results

Table 4: Average error for the inverter driving general *RC* load (Skewness=0.5)

	σ=10%			σ=15%		
Average error	**Ceff**	**Delay**	**Slew**	**Ceff**	**Delay**	**Slew**
Mean	3.2%	3.5%	4.9%	3.5%	5.4%	5.8%
Variance	2.4%	3.3%	4.5%	2.6%	5.9%	5.2%
Skewness	2.5%	3.3%	4.9%	2.0%	5.5%	5.5%

Table 5: Average error for the inverter driving general *RC* load (Skewness=0.75)

	σ=10%			σ=15%		
Average error	**Ceff**	**Delay**	**Slew**	**Ceff**	**Delay**	**Slew**
Mean	3.5%	5.1 %	5.3%	3.8%	5.9%	6.1%
Variance	2.9%	4.3%	5.5%	3.6%	6.2%	6.2%
Skewness	2.8%	4.1%	4.9%	3.1%	5.9%	5.9%

Table 6: Average error for the 2-input NAND gate driving general *RC* load (Skewness=1)

	σ=10%			σ=15%		
Average error	**Ceff**	**Delay**	**Slew**	**Ceff**	**Delay**	**Slew**
Mean	4.1%	5.2 %	5.1%	4.2%	6.1%	6.7%
Variance	3.9%	5.4%	5.2%	4.3%	6.1%	6.1%
Skewness	4.0%	6.1%	5.6%	4.2%	6.5%	6.3%

Conclusion and Future Work

- Variability increases as we go toward UDSM technologies
- A solution for parameterized block-based Non-Gaussian gate timing analysis is proposed

- A more exact gate model for statistical analysis purpose?
- How to perform statistical gate timing analysis in the presence of noise?

Thank you!

One-iteration C_{eff} Analysis (Cont'd)

$$C_{eff}^{Exp}(\theta) = C_n + k_{Exp}(\theta)\, C_f \quad \textit{where}$$

$$k_{Exp}(\theta) = \left[1 + \frac{y}{\theta}\left(e^{\ln(1-\theta)/y} - 1\right)\right] \quad \textit{and} \quad y = \ln\left[\frac{1-\alpha}{1-\beta}\right] \times \frac{R_\pi C_f}{T_{R(\alpha-\beta)}}$$

$$C_{eff}^{Ramp}(\theta) = C_n + k_{Ramp}(\theta)\, C_f \quad \textit{where}$$

$$k_{Ramp}(\theta) = \left[1 - \frac{x}{\theta}\left(1 - e^{-\theta/x}\right)\right] \quad \textit{and} \quad x = (\beta - \alpha)\frac{R_\pi C_f}{T_{R(\alpha-\beta)}}$$

Therfore;

$$c_{eff}(\theta) = F\left(t_r\left(t_{in}, c_{eff}(\theta)\right), c_n.r_\pi, c_f\right)$$