ASP-DAC 2006

Contents

Highlights

Keynote Addresses

Wednesday, January 25, 9:00-10:00, Small Auditorium, 5F

"Automotive Electronics: Steady Growth for Years to Come!"
Alberto Sangiovanni-Vincentelli - The Edgar L. and Harold H. Buttner Chair of Electrical Engineering and Computer Science, Univ. of California, Berkeley, and Chief Technology Advisor, Member of the Board and Co-founder, Cadence Design Systems, United States

Thursday, January 26, 9:00-10:00, Small Auditorium, 5F

"Challenging Device Innovation"
Satoru Ito - President & CEO, RENESAS Technology Corp., Japan

Friday, January 27, 9:00-10:00, Small Auditorium, 5F

"Effective Platform-based Development for Large-scale Systems Design"
Yukichi Niwa - Senior Advisory Director, Group Executive of Platform Technology Development Headquarters, CANON INC., Japan

Special Sessions

1D: Wednesday, January 25, 10:15-12:20, Room 416+417
"Presentation + Poster Discussion: University Design Contest"

2D: Wednesday, January 25, 13:30-15:35, Room 416+417
"Invited Talks: Electrothermal Design of Nanoscale Integrated Circuits"

2D-1: Electrothermal Analysis and Optimization Techniques for Nanoscale Integrated Circuits
Yong Zhan, Brent Goplen, Sachin S. Sapatnekar (Univ. of Minnesota, United States)

2D-2: Electrothermal Engineering in the Nanometer Era: From Devices and Interconnects to Circuits and Systems
Kaustav Banerjee, Sheng-Chih Lin, Navin Srivastava (Univ. of California, Santa Barbara, United States)

2D-3: Area Optimization for Leakage Reduction and Thermal Stability in Nanometer Scale Technologies
Ja Chun Ku, Yehea Ismail (Northwestern Univ., United States)

2D-4: Compact Thermal Models for Estimation of Temperature-dependent Power/Performance in FinFET Technology

Aditya Bansal, Mesut Meterelliyoz (Purdue Univ., United States), Siddharth Singh (Osmania Univerisity, India), Jung Hwan Choi, Jayathi Murthy, Kaushik Roy (Purdue Univ., United States)

3D: Wednesday, January 25, 16:00-18:05, Room 416+417
"Invited Talks: Flash Memory in Embedded Systems"

3D-1: Current Trends in Flash Memory Technology
Sang Lyul Min, Eyee Hyun Nam (Seoul National Univ., Republic of Korea)

3D-2: Configurability of Performance and Overheads in Flash Management
Tei-Wei Kuo, Jen-Wei Hsieh (National Taiwan Univ., Taiwan), Li-Pin Chang (National Chiao-Tung Univ., Taiwan), Yuan-Hao Chang (National Taiwan Univ., Taiwan)

4D: Thursday, January 26, 10:15-12:20, Room 416+417
"Invited Talks: Open Access Overview"

4D-1: An Introduction to OpenAccess -An Open Source Data Model and API for IC Design-
Michaela Guiney, Eric Leavitt (Cadence, United States)

4D-2: Open Access Overview "Industrial Experience"
Yoshio Inoue (Renesas, Japan)

4D-3: EDA Vendor Adoption
Hillel Ofek (Sagantec, United States)

4D-4: Utility of the OpenAccess Database in Academic Research
David Papa, Igor Markov (Univ. of Michigan, United States), Phillip Chong (Cadence Design Systems, United States)

7D: Friday, January 27, 10:15-12:20, Room 416+417
"Invited Talks + Panel Disucssion: H.264/AVC Design Challenges and Solutions"

7D-1: Introduction to H.264 Advanced Video Coding
Jian-Wen Chen, Chao-Yang Kao, Youn-Long Lin (National Tsing Hua Univ., Taiwan)

7D-2: Algorithm and DSP Implementation of H.264/AVC
Hung-Chih Lin, Yu-Jen Wang, Kai-Ting Cheng, Shang-Yu Yeh, Wei-Nien Chen, Chia-Yang Tsai, Tian-Sheuan Chang, Hsueh-Ming Hang (National Chiao-Tung Univ., Taiwan)

7D-3: Hardware Architecture Design of an H.264/AVC Video Codec
Tung-Chien Chen, Chung-Jr Lian, Liang-Gee Chen (National Taiwan Univ., Taiwan)

7D-4: ASIP Approach for Implementation of H.264/AVC
Sung Dae Kim, Jeong Hoo Lee, Chung Jin Hyun, Myung Hoon Sunwoo (Ajou Univ., Republic of Korea)

7D-5: Panel Discussion

Moderator: Wayne Wolf (Princeton Univ.)
Panelists: Youn-Long Lin (National Tsing Hua Univ.)
Hsueh-Ming Hang (National Chiao-Tung Univ.)
Liang-Gee Chen (National Taiwan Univ.)
Myung-Hoon Sunwoo (Ajo Univ.)

Designers' Forum

5D: Thursday, January 26, 13:30-15:30, Small Auditorium, 5F
"Invited Talks: Low Power Design"

5D-1: Low-Power Design Methodology for Module-wise Dynamic Voltage and Frequency Scaling with Dynamic De-skewing Systems
Takeshi Kitahara, Hiroyuki Hara, Shinichiro Shiratake (Toshiba, Japan), Yoshiki Tsukiboshi (Toshiba Microelectronics Co., Japan), Tomoyuki Yoda, Tetsuaki Utsumi, Fumihiro Minami (Toshiba, Japan)

5D-2: Single-Chip Multi-Processor Integrating Quadruple 8-Way VLIW Processors with Interface Timing Analysis Considering Power Supply Noise
Satoshi Imai, Atsuki Inoue, Motoaki Matsumura, Kenichi Kawasaki, Atsuhiro Suga (Fujitsu Lab., Japan)

5D-3: A System-level Power-estimation Methodology based on IP-level Modeling, Power-level Adjustment, and Power Accumulation
Masafumi Onouchi, Tetsuya Yamada (Hitachi Ltd., Japan), Kimihiro Morikawa, Isamu Mochizuki, Hidetoshi Sekine (Renesas, Japan)

5D-4: PowerViP: SoC Power Estimation Framework at Transaction Level
Ikhwan Lee, Hyunsuk Kim, Peng Yang, Sungjoo Yoo (Samsung Electronics, Republic of Korea), Eui-Young Chung (Yonsei Univ., Republic of Korea), Kyu-Myung Choi, Jeong-Taek Kong, Soo-Kwan Eo (Samsung Electronics, Republic of Korea)

6D: Thursday, January 26, 16:30-18:00, Small Auditorium, 5F
"Panel Discussion: Functional Verification -now and future-"

Organizer: Haruyuki Tago (TOSHIBA)
Moderator: Yoshio Masubuchi (TOSHIBA)
Panelists: Sanjay Gupta (IBM)
Michael Stellfox (Cadence)
Tetsuji Sumioka (Sony)
Sunao Torii (NEC)

8D: Friday, January 27, 13:30-15:30, Small Auditorium, 5F
"Invited Talks: 'Cell' Processor"

8D-1: A New Test and Characterization Scheme for 10+ GHz Low Jitter Wide Band PLL

Kazuhiko Miki (Toshiba, Japan), David Boerstler, Eskinder Hailu, Jieming Qi, Sarah Pettengill (IBM Microelectronics, United States), Yuichi Goto (Toshiba, Japan)

8D-2: An SPU Reference Model for Simulation, Random Test Generation and Verification
Yukio Watanabe (Toshiba, Japan), Balazs Sallay, Brad Michael, Daniel Brokenshire, Gavin Meil, Hazim Shafi (IBM, United States), Daisuke Hiraoka (Sony Computer Entertainment Inc., Japan)

8D-3: A Cycle Accurate Power Estimation Tool
Rajat Chaudhry, Daniel Stasiak, Stephen Posluszny, Sang Dhong (IBM, United States)

8D-4: Key Features of the Design Methodology Enabling a Multi-Core SoC Implementation of a First-Generation CELL Processor
Dac Pham, Hans-Werner Anderson, Erwin Behnen, Mark Bolliger, Sanjay Gupta, Peter Hofstee, Paul Harvey, Charles Johns, Jim Kahle (IBM, United States), Atsushi Kameyama (Toshiba America Electronic Components, United States), John Keaty, Bob Le, Sang Lee, Tuyen Nguyen, John Petrovick, Mydung Pham, Juergen Pille, Stephen Posluszny, Mack Riley, Joseph Verock, James Warnock, Steve Weitzel, Dieter Wendel (IBM, United States)

9D: Friday, January 27, 16:30-18:00, Small Auditorium, 5F
"Panel Disussion: Top 10 Design Issues by LSI Designers versus EDA Developers"

Organizer: Haruyuki Tago (TOSHIBA)
Moderator: Yoshiaki Hagihara (Sony)
Panelists: Raul Camposano (Synopsys)
Soo-Kwan Eo (SAMSUNG)
Joe Sawichi (Mentor)
Hirofumi Taguchi (Matsushita)
Yasuhiro Tani (CANON)
Ted Vucurevich (Cadence)

Two Full-Day and Four Half-Day Tutorials

FULL-DAY Tutorials:
Tuesday, January 24, 2006, 9:30-17:00

1 **DFM Tools and Methodologies for 65nm and Below**
Organizer: ***Andrew B. Kahng*** -UCSD and Blaze DFM, Inc., United States
Speakers: ***Andrew B. Kahng*** -UCSD and Blaze DFM, Inc., United States, ***Louis K. Scheffer*** -Cadence Design Systems, Inc., United States, ***Michael Orshansky*** -Univ. of Texas, Austin, United States, ***Andrzej Strojwas*** -PDF Solutions, Inc. and CMU, United States

2 **High Performance Interconnect and Packaging**

Organizers: ***Chung-Kuan Cheng*** -Univ. of California, San Diego, United States, ***Howard Chen*** -IBM, United States
Speakers: ***Paul M. Harvey*** -IBM, United States, ***Howard Chen*** -IBM, United States, ***Chung-Kuan Cheng*** -Univ. of California, San Diego, United States, ***Manjit Borah*** -Fastrack, United States, ***Lei He*** -Univ. of California, Los Angeles, United States, ***Sheldon Tan*** -Univ. of California, Riverside, United States

HALF-DAY Tutorials:
Tuesday, January 24, 2006, 9:30-12:30

3 **Low Power / Low Leakage Technologies for Nanometer Era: System and Architecture Level Approaches**
Organizer: ***Kimiyoshi Usami*** -Shibaura Inst. of Tech., Japan
Speakers: ***Naohiko Irie*** -Hitachi Ltd., Japan, ***Hiroshi Nakamura*** -Univ. of Tokyo, Japan

Tuesday, January 24, 2006, 14:00-17:00

4 **Low Power / Low Leakage Technologies for Nanometer Era: Circuit and Device Level Approaches**
Organizer: ***Kimiyoshi Usami*** -Shibaura Inst. of Tech., Japan
Speakers: ***Kimiyoshi Usami*** -Shibaura Inst. of Tech., Japan, ***Tohru Mogami*** -NEC Corporation, Japan

Tuesday, January 24, 2006, 9:30-12:30

5 **Basics and Practice of Current Functional Verification Methods**
Organizer: ***Kiyoharu Hamaguchi*** -Osaka Univ., Japan
Speakers: ***Kiyoharu Hamaguchi*** -Osaka Univ., Japan, ***Erich Marschner*** -Cadence Design Systems, Inc., United States

Tuesday, January 24, 2006, 14:00-17:00

6 **SoC Communication Architectures: Current Practice, Research and Trends**
Organizer: ***Nikil Dutt*** -Univ. of California, Irvine, United States
Speakers: ***Nikil Dutt*** -Univ. of California, Irvine, United States, ***Sudeep Pasricha*** -Univ. of California, Irvine, United States

Welcome to ASP-DAC 2006

On behalf of the Organizing Committee, I would like to welcome you to the Asia and South Pacific Design Automation Conference 2006 (ASP-DAC 2006) being held here at Pacifico Yokohama jointly with the Electronic Design and Solution Fair 2006. ASP-DAC is a sister conference of DAC, DATE and ICCAD, and it is the 11th event of this conference series.

ASP-DAC is the meeting place where researchers and engineers come together to learn and discuss state of the art technologies of system/SoC design, EDA and design methodologies. This year, we put special effort into attracting designers and design industries to produce Designers' Forum.

We have three keynote speakers from academia, the semiconductor industry and the systems industry. Professor Alberto Sangiovanni-Vincentelli, University of California at Berkeley, will explore future system design perspectives in automotive electronics. Satoru Ito, President & CEO of RENESAS Technology Corp. will discuss challenges of device innovation. Yukichi Niwa, Senior Advisory Director of CANON INC. will present the company's key concept of architecting platform based design.

The technical program was selected from 424 papers from 27 countries. The 64 members of the Technical Program Committee chaired by Professor Onodera and helped by over 250 reviewers had to make difficult choices to carefully select 135 papers. It is an outstanding program that covers a variety of key topics from system level design to physical design. Designers' Forum is a new program that shares design experience and solutions of real product designs of the industries whose topics include the CELL and mobile designs, panels of top 10 design issues and system verification. The University Design Contest is also an important event of ASP-DAC, which focuses on a real chip design in academia. On Tuesday, one full-day and six half-day tutorials are scheduled to provide introductions to hot topics like DFM, lowpower, packaging/interconnect, system level design and verification.

An event like ASP-DAC can happen only with the efforts of many people. We wish to express our appreciation to all authors, speakers, reviewers, session organizers, moderators, panelists, session chairs, keynote speakers and committee members. Also my sincere thanks to the dedicated members of the Organizing Committee, the Technical Program Committee, the University LSI Design Contest Committee, the Industry Liaison and the Steering Committee.

Finally, special thanks to all ASP-DAC attendees. I hope you will have a productive and exciting experience at ASP-DAC 2006.

Fumiyasu Hirose
General Chair
ASP-DAC 2006

Message from Technical Program Committee

On behalf of the Technical Program Committee for the Asia and South Pacific Design Automation Conference 2006, we would like to welcome all of you to the conference held from January 24 through 27, 2006 at Pacifico Yokohama Conference Center in Yokohama, Japan.

This year, ASPDAC received 424 paper submissions, which is the second highest number in our history. This is a 46% increase in submissions over the last ASPDAC held in Japan two years ago. The submissions span 27 countries/regions in Asia, North America, South America, Europe, Oceania, and Africa.

The Technical Program Committee was composed of 64 professionals who are experts on EDA, LSI design, and embedded system design, and was organized into 11 subcommittees. The number of committee members is relatively small compared to the previous conferences. However, all the members were committed to make in-depth reviews for all the papers assigned to each sub-committee and physically attend the TPC meeting for paper selection. Based on the result of a rigorous and thorough review followed by a full day face-to-face discussion, we have selected 135 papers and compiled them into a 3-day program of 27 technical sessions in three parallel tracks. The technical program is further enriched by multiple special sessions and panels in one more track, resulting in four parallel tracks of exciting presentations and discussions.

Each day, the technical program starts with a keynote address that is organized through the leadership of Fumiyasu Hirose, General Chair, followed by regular and special sessions. We have 7 special sessions in total. On Wednesday, selected submissions to the University Design Contest will be presented at Session 1D. Session 2D focuses on electrothermal design and Session 3D discusses flash memory in embedded systems. On Thursday, Session 4D addresses an overview of Open Access and Session 5D focuses on low power design challenges for mobile applications. On Friday, Session 7D discusses H.264 design issues and Session 8D addresses design methodology for "Cell" processor development. It should be mentioned that Sessions 5D and 8D are organized as Designers' Forum that is a brand new event for encouraging mutual exchange between/within designers in industry and EDA researchers. Besides two special sessions, Designers' Forum will organize two panel discussions on functional verification (Session 6D, Thursday) and top-10 design issues (Session 9D, Friday). These special sessions will provide you with a wide variety of hot and exciting topics

from system level down to physical level, and from industrial design issues to theoretical fundamentals.

On behalf of the Technical Program Committee, we would like to thank all people involved in the 2006 event. In particular, we would like to thank the members of the Organizing and Technical Program Committees, the members of Industry Liaison, special session organizers, and everyone at JESA for conference management. Also, we would like to express our sincere thanks to all the authors who submitted papers with valuable results, since their contributions form the basis of our technical excellence.

We would be more than happy if you could attend the conference and find something new in the directions of EDA and technologies during ASP-DAC 2006.

Hidetoshi Onodera
ASP-DAC 2006 Technical Program Chair
Yusuke Matsunaga
ASP-DAC 2006 Technical Program Vice Chair

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[2] Embedded and Real-Time Systems

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[3] Behavioral/Logic Synthesis and Optimization

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[4] Validation and Verification for Behavioral/Logic Design

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[5] Physical Design (Routing)

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[6] Physical Design (Placement)

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[7] Timing, Power, Signal/Power Integrity Analysis and Optimization

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[8] Interconnect, Device and Circuit Modeling and Simulation

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[9] Test and Design for Testability

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[10] Analog, RF and Mixed Signal Design and CAD

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[11] Leading Edge Design Methodology for SOCs and SIPs

∗**Hideharu Amano**
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University LSI Design Contest

The University LSI Design Contest was conceived as a unique program of ASP-DAC Conference. The purpose of the Contest is to encourage education and research in LSI design, and its realization on chips at universities, and other educational organizations by providing opportunities to present and discuss innovative and state-of-the-art designs at the conference. Application areas and types of circuits include (1) Analog and Mixed-Signal Circuits, (2) Digital Signal processing, (3) Microprocessors, and (4) Custom Application Specific Circuits. Methods or technology used for implementation include (a) Full Custom and Cell-Based LSIs, (b) Gate Arrays, and (c) Field Programmable Devices, including FPGA/PLDs.

This year, nineteen selected designs from seven countries/areas will be disclosed in Session 1D with a short presentations followed by live discussions in front of posters with light meals. Submitted designs were reviewed by the members of the University Design Contest Committee based on the following criteria: Reliability of design and implementation, Quality of implementation, Performance of the design, Novelty, and Additional special features. In the selection process, emphasis was placed more on reliability, quality, and performance. As a result, the nineteen designs were selected. Also, we have instituted one outstanding design award and two special feature awards.

It is with great pleasure that we acknowledge the contributions to the Design Contest, and it is our earnest belief that it will promote and enhance research and education in LSI design in academic organizations. It is also our hope that many people not only in academia but in industry will attend the contest and enjoy the stimulating discussions.

Date, Time and Locations:

Oral Presentation 10:15-12:20, January 25, 2006, Room 416+417
Poster Presentation 12:20-13:30, January 25, 2006, Room 418 (Food will be served.)

University LSI Design Contest Committee

Co-Chair
Kazutoshi Kobayashi
Kyoto University

Co-Chair
Takahiko Arakawa
RENESAS Technology Corp.

Designers' Forum

This brandnew event, Designers' Formum, is conceived as a unique program for ASP-DAC to encourage mutual exchange both between and within designers in industry, researchers in the area of EDAs, and EDA developers. Here, designs will be presented focusing on design styles, design issues, and ways to tackle design issues. Panel discussions will also be held for the latest design issues.

This year, we will have 2 special sessions in ASP-DAC 2006 as follows. 4 presentations related to low power designs, power models, and power estimation frameworks for the real SoC designs will be given by Toshiba, Fujitsu, Hitachi and Renesas, and Samsung in session 5D, "Low Power Design." In session 8D, "Cell processor", 4 presentations will be given fucusing on simulations, tests, verifications, power estimation, and design methodology of Cell; and PLL design employed in the Cell processor.

In addition to the special sessions, we will have 2 panel discussions. Session 6D, "Functional Verification -now and future-" will be modareted by Dr. Y. Masubuchi of Toshiba, who has been deeply engaged in the architecture design and verifications of the Cell processor. Three panelists are LSI designers, working for functional verifications in LSI design, and one panelist is from an EDA vendor, developing functional verification tools. Session 9D, "Top 10 design issues seen by LSI designers versus EDA developers", on the other hand, will be moderated by Dr. Y. Hagihara of Sony. Three panelists are managers of SoC and system designs, will focus on the top 10 design issues seen by LSI designers; and 3 panelists are techology officers from 3 major EDA vendors, and they will focus on top 10 design issues seen by EDA developers. Discussions will be led toward the perspectives of the future SoC design issues, comparing with the two top 10 issues seen by both LSI designers and EDA developers.

This Designers' Forum is planned by the Industry Laison Members of ASP-DAC2006. It is with great pleasure that we acknowledge the contributions to the Designers' Forum, and it is our earnest belief that this forum will promote mutual exchange of designers and EDA researchers and developers, toward nano-meter SoC design issues.

Industry Liaison Chair
Haruyuki Tago
TOSHIBA CORPORATION

Designers' Forum Chair
Makoto Ikeda
University of Tokyo

Ph.D. Forum at ASP-DAC 2006

This year for the second time ASP-DAC is holding a poster session for Ph.D. students to present their research work. The forum provides a great opportunity for students to get feedback and have discussion with people from academia and industry.

Date and Time: 12:20-13:30, January 26, 2006

Location: Room 418 (Food will be served.)

We would like to thank the following persons that evaluated the submissions,

- Ali Afzali-Kusha, Tehran University, Iran
- Supratik Chakraborty, Indian Institute of Technology Bombay, India
- Naehyuk Chang, Seoul National University, South Korea
- Sheqin Dong, Tsinghua University, China
- Toru Ishihara, Kyushu University, Japan
- Philip Leong, Imperial College, England
- Hiroshi Saito, University of Aizu, Japan
- Toshiyuki Shibuya, Fujitsu, Japan
- Omid Shoaei, University of Tehran, Iran
- Makoto Sugihara, Institute of Systems and Information Technologies, Japan

We would also like to thank SpringSoft Foundation for providing travel grants for students from Taiwan, the Engineering Sciences Society of the Institute of Electronics, Information and Communication Engineers, and ASP-DAC for providing travel grants for other students and sponsoring the event.

Special thanks to Dr. Fumiyasu Hirose, Professor Youn-Long Steve Lin, Professor Hidetoshi Onodera, Dr. Atsushi Takahashi, and Professor Hiroto Yasuura for supporting and contributing to the Ph.D. Forum.

Organizer
Farzan Fallah
Fujitsu Labs. of America

ASP-DAC 2006 Best Papers

Best Paper Candidates

1B-1 **Constraint-Driven Bus Matrix Synthesis for MP-SoC**
Sudeep Pasricha, Nikil Dutt (Univ. of California, Irvine, United States), Mohamed Ben-Romdhane (Conexant, United States)

3C-1 **Post-Routing Redundant Via Insertion for Yield/Reliability Improvement**
Kuang-Yao Lee, Ting-Chi Wang (National Tsing Hua Univ., Taiwan)

7B-1 **Equivalent Circuit Modeling of Guard Ring Structures for Evaluation of Substrate Crosstalk Isolation**
Daisuke Kosaka, Makoto Nagata (Kobe Univ., Japan)

7C-2 **Speed Binning Aware Design Methodology to Improve Profit under Parameter Variations**
Animesh Datta (Purdue Univ., United States), Swarup Bhunia (Case Western Reserve Univ., United States), Jung Hwan Choi, Saibal Mukhopadhyay, Kaushik Roy (Purdue Univ., United States)

8A-1 **Fast Substrate Noise-Aware Floorplanning with Preference Directed Graph for Mixed-Signal SOCs**
Minsik Cho, Hongjoong Shin, David Z. Pan (Univ. of Texas, Austin, United States)

8B-1 **Finding Optimal L1 Cache Configuration for Embedded Systems**
Andhi Janapsatya, Aleksandar Ignjatovic, Sri Parameswaran (Univ. of New South Wales, Australia)

9A-1 **TAPHS: Thermal-Aware Unified Physical-Level and High-Level Synthesis**
Zhenyu (Peter) Gu (Northwestern Univ., United States), Yonghong Yang (Queen's Univ., Canada), Jia Wang, Robert P. Dick (Northwestern Univ., United States), Li Shang (Queen's Univ., Canada)

9C-3 **Statistical Leakage Minimization through Joint Selection of Gate Sizes, Gate Lengths and Threshold Voltage**
Sarvesh Bhardwaj, Yu Cao, Sarma Vrudhula (Arizona State Univ., United States)

Best Paper Award

1B-1 **Constraint-Driven Bus Matrix Synthesis for MP-SoC**
Sudeep Pasricha, Nikil Dutt (Univ. of California, Irvine, United States), Mohamed Ben-Romdhane (Conexant, United States)

3C-1 **Post-Routing Redundant Via Insertion for Yield/Reliability Improvement**
Kuang-Yao Lee, Ting-Chi Wang (National Tsing Hua Univ., Taiwan)

ASP-DAC 2006 Design Contest Award

Outstanding Design Award

1D-15 **A 52mW 1200MIPS Compact DSP for Multi-Core Media SoC**
Shih-Hao Ou, Tay-Jyi Lin, Chao-Wei Huang, Yu-Ting Kuo, Chie-Min Chao, Chih-Wei Liu (National Chiao Tung Univ., Taiwan), Chein-Wei Jen (STC, ITRI, Taiwan)

Special Feature Award

1D-1 **A Low Dynamic Power and Low Leakage Power 90-nm CMOS Square-Root Circuit**
Tadayoshi Enomoto, Nobuaki Kobayashi (Chuo Univ., Japan)

1D-8 **Adaptively-Biased Capacitor-Less CMOS Low Dropout Regulator with Direct Current Feedback**
Yat-Hei Lam, Wing-Hung Ki, Chi-Ying Tsui (Hong Kong Univ. of Science and Tech., Hong Kong)

Invitation to ASP-DAC 2007

On behalf of the Organizing Committee, it is my great pleasure and honor to invite all of you to ASP-DAC 2007, which is the 12th event of this conference series. The conference will be held from January 23 to 26, 2007 at Pacifico Yokohama, Japan. The conference site is the same as this year.

Technical Program Chair of this conference is Professor Yusuke Matsunaga from Kyushu University, Japan. Technical Program Vice Chair is Professor Kiyoung Choi from Seoul National University, Korea. Under their strong leadership, internationally organized Program Committee will structure ASP-DAC as a high-quality conference that emphasizes original contributions that open up new vistas in the field with significant theoretical and practical impact.

The conference will include a technical program, keynote talks, tutorials, and special sessions highlighting the latest issues and development in IC design technology and automation. I would like to invite you to actively participate in ASP-DAC by submitting cutting edge research results for publication, by proposing interesting topics for tutorials and special sessions, or simply by dropping by in January to enjoy a lively ASP-DAC event.

Hidetoshi Onodera
General Chair
ASP-DAC 2007

Keynote Addresses

Keynote Address I
Wednesday, January 25, 9:00-10:00,
Small Auditorium, 5F
"Automotive Electronics: Steady Growth for Years to Come!"
Alberto Sangiovanni-Vincentelli

The Edgar L. and Harold H. Buttner Chair of Electrical Engineering and Computer Science, University of California, Berkeley, and Chief Technology Advisor, Member of the Board and Co-founder, Cadence Design Systems, United States

The world of electronics is witnessing a revolution in the way products are conceived, designed and implemented. The ever growing importance of the web, the advent of microprocessors of great computational power, the explosion of wireless communication, the development of new generations of integrated sensors and actuators are changing the world in which we live and work. The new key words are:

- Disappearing electronics, i.e., electronics has to be invisible to the user, it has to help unobtrusively.
- Pervasive computing, i.e., electronics is everywhere, all common use objects will have an electronic dimension.
- Ambient intelligence, i.e., the environment will react to us with the use of electronic components. They will recognize who we are and what we like.
- Wearable computing, i.e., the new devices will be worn as a watch or a hat. They will become part of our clothes. Some of these devices will be tags that will contain all important information about us.
- Know more, carry less, i.e., the environment will know more about us so that we will not need to carry all the paraphernalia of keys, credit cards, personal I.D.s, access cards, access codes.

The car as a self-contained microcosm is experiencing a similar revolution: all the key words listed above are going to have a great impact on the automotive world. We need to rethink what a car really is and the role of electronics in it. Electronics is now essential to control the movements of a car, of the chemical and electrical processes taking place in it, to entertain the passengers, to establish connectivity with the rest of the world, to ensure safety. What will an automobile manufacturer's core competence become in the next few years? Will electronics be the essential element in car manufacturing and design? The challenges and opportunities are related to

- how to integrate the mechanical and the electronics worlds, i.e., how to make mechatronics a reality in the automotive world,
- how to integrate the different motion control and power-train control functions so that important synergies can be exploited,
- how to combine entertainment, communication and navigation subsystems,
- how to couple the world of electronics where the life time of a product is around 2 years and shrinking, with the automotive world, where the product life time is 10 years and possibly growing,
- how to develop new services based on electronics technology,
- how to exploit communication among cars and between cars and infrastructure such as Global Positioning Systems and cellular networks,

- how are the markets evolving (for example, what will be the size of the after-market sales for automotive electronics, if any?).

We will pose these questions while reviewing some of the most important technology and product developments of the past few years. We will also present new trends on how the design of electronics of the car should be carried out. We will finally analyze the dynamics of the automotive electronics industry that is bound to produce a major shake-up in the structure of the design chain with particular emphasis on the AUTOSAR consortium.

Keynote Address II
Thursday, January 26, 9:00-10:00,
Small Auditorium, 5F
"Challenging Device Innovation"

Satoru Ito
President & CEO
RENESAS Technology Corp., Japan

The semiconductor industry has continuously transformed our way of life, through a number of underlying technology breakthroughs and innovations over the past years. There are currently two challenges that this industry faces: a limitation of miniaturization technology and a difficulty in maintaining an economy of scale. To cope with these challenges, there is a growing need to work closely with partners and customers who have business related to semiconductors, in addition to semiconductor manufacturers. Especially in the area of semiconductor design, we see a need to create a new EDA methodology that broadens the definition of traditional EDA and re-defines the connection among system designers, SoC designers and development tool designers. As we move closer to the realm driven by the convergence of applications and advancements in miniaturization technology, I'd like to discuss the associated technological challenges as well as economical challenges, and present to you our strategy to overcome these issues.

Keynote Address III
Friday, January 27, 9:00-10:00,
Small Auditorium, 5F
"Effective Platform-based Development for Large-scale Systems Design"

Yukichi Niwa
Senior Advisory Director,
Group Executive of Platform Technology Development Headquarters
CANON INC., Japan

Platform-based development (PBD) aims to continuously add new value in both cases of incremental development and product planning based development. By adding new technology to previously existing technology and by storing the technologies as reusable assets, PBD enables high quality, low cost, and short turnaround time development. Furthermore, PBD allows target-oriented development where we can select and concentrate technology to eliminate unnecessary development.

In order to execute effective PBD, it is important to introduce the firm layer structuring of digital/analog technology so that individual professionals in independent layer can maximize their efficiency without any restraint. The act of layer structuring is nothing but the architectural design of the development methodology. Thus, it's no exaggeration to say that success in business profitability management directly depends on the presence of the good architect.

The important thing in the next stage is to optimize the design process by investing in computer resources. For example, it is necessary to thoroughly adapt simulation technology to the development of high quality imaging technology, embedded system (hardware/software) technology, or communication technology. The quantitative evaluation from the early design phase and the workflow based on the accumulated design know-how (IP, methodology) will accelerate technology innovation and strengthen the platform even further. Eventually, management can directly obtain absolute advantage of large-scale system design effectiveness.

Technical Program

Wednesday, January 25, 8:30 - 9:00

Wednesday, January 25, 8:30 - 9:00 Small Auditorium, 5F
Opening Session:

Wednesday, January 25, 9:00 - 10:00

Wednesday, January 25, 9:00 - 10:00 Small Auditorium, 5F
Keynote Address I :

Chair(s): ***Fumiyasu Hirose*** – Cadence, Japan

Automotive Electronics: Steady Growth for Years to Come!

Alberto Sangiovanni-Vincentelli (The Edgar L. and Harold H. Buttner Chair of Electrical Engineering and Computer Science, Univ. of California, Berkeley, and Chief Technology Advisor, Member of the Board and Co-founder, Cadence Design Systems, United States)

Wednesday, January 25, 10:15 - 12:20

Wednesday, January 25, 10:15 - 12:20 Room 411+412
Session 1A: Formal Methods for Coverage and Scalable Verification

Chair(s): ***Kiyoharu Hamaguchi*** – Osaka Univ., Japan
Valeria Bertacco – Univ. of Michigan, United States

1A-1 Transition-Based Coverage Estimation for Symbolic Model Checking
Xingwen Xu, Shinji Kimura (Waseda Univ., Japan), Kazunari Horikawa, Takehiko Tsuchiya (Toshiba, Japan)

1A-2 Word Level Functional Coverage Computation
Bijan Alizadeh (Microelectronic Research and Development Center of Iran, Iran)

1A-3 Discovering the Input Assumptions in Specification Refinement Coverage
Prasenjit Basu, Sayantan Das, Pallab Dasgupta, Partha P Chakrabarti (Indian Inst. of Tech. Kharagpur, India)

1A-4 Refinement Strategies for Verification Methods Based on Datapath Abstraction
Zaher Semon Andraus, Mark Hammond Liffiton, Karem Ahmad Sakallah (Univ. of Michigan, Ann Arbor, United States)

1A-5 Generation of Shorter Sequences for High Resolution Error Diagnosis Using Sequential SAT
Sung-Jui Pan, Kwang-Ting Cheng (Univ. of California, Santa Barbara, United States), John Moondanos, Ziyad Hanna (Intel Co., United States)

Wednesday, January 25, 10:15 - 12:20 Room 413
Session 1B: Interconnect for High-End SoC

Chair(s): ***Yoshinori Takeuchi*** – Osaka Univ., Japan
Juinn-Dar Huang – National Chiao-Tung Univ., Taiwan

1B-1 Constraint-Driven Bus Matrix Synthesis for MP-SoC
Sudeep Pasricha, Nikil Dutt (Univ. of California, Irvine, United States), Mohamed Ben-Romdhane (Conexant, United States)

1B-2 Improving Routing Efficiency for Network-on-Chip through Contention-Aware Input Selection
Dong Wu, Bashir M. Al-Hashimi, Marcus T. Schmitz (Univ. of Southampton, Great Britain)

1B-3 Physical Design Implementation of Segmented Buses to Reduce Communication Energy
Jin Guo, Antonis Papanikolaou, Pol Marchal, Francky Catthoor (IMEC, Belgium)

1B-4 Co-Synthesis of a Configurable SoC Platform based on a Network on Chip Architecture
Mário Pereira Véstias, Horácio Neto (INESC-ID, Portugal)

1B-5 Customized SIMD Unit Synthesis for System on Programmable Chip - A Foundation for HW/SW Partitioning with Vectorization
Muhammad Omer Cheema, Omar Hammami (ENSTA Paris, France)

Wednesday, January 25, 10:15 - 12:20 Room 414+415
Session 1C: Timing Analysis and Optimization

Chair(s): ***Ryuichi Yamaguchi*** – Matsushita, Japan
Atsushi Kurokawa – STARC, Japan

1C-1 Robust Analytical Gate Delay Modeling for Low Voltage Circuits
Anand Ramalingam (Univ. of Texas, Austin, United States), Sreekumar V. Kodakara (Univ. of Minnesota, United States), Anirudh Devgan (Magma, United States), David Z. Pan (Univ. of Texas, Austin, United States)

1C-2 CGTA: Current Gain-based Timing Analysis for Logic Cells
Shahin Nazarian, Massoud Pedram (Univ. of Southern California, United States), Tao Lin, Emre Tuncer (Magma, United States)

1C-3 Efficient Static Timing Analysis Using a Unified Framework for False Paths and Multi-Cycle Paths
Shuo Zhou, Bo Yao, Hongyu Chen, Yi Zhu, Chung-Kuan Cheng (Univ. of California, San Diego, United States), Mike Hutton (Altera Corp., United States)

1C-4 Crosstalk Analysis using Reconvergence Correlation
Sachin Shrivastava, Rajendra Pratap, Harindranath Parameswaran, Manuj Verma (Cadence Design Systems, India)

1C-5 Process-Induced Skew Reduction in Nominal Zero-Skew Clock Trees
Matthew R. Guthaus, Dennis Sylvester (Univ. of Michigan, United States), Richard B. Brown (Univ. of Utah, United States)

Wednesday, January 25, 10:15 - 12:20 Room 416+417
Session 1D: University Design Contest

Chair(s): ***Kazutoshi Kobayashi*** – Kyoto Univ., Japan
Takahiko Arakawa – Renesas, Japan

1D-1 A Low Dynamic Power and Low Leakage Power 90-nm CMOS Square-Root Circuit
Tadayoshi Enomoto, Nobuaki Kobayashi (Chuo Univ., Japan)

1D-2 A High-Throughput Low-Power Fully Parallel 1024-bit 1/2-Rate Low Density Parity Check Code Decoder in 3-Dimensional Integrated Circuits
Lili Zhou, Cherry Wakayama, Nuttorn Jangkrajarng, Bo Hu, Richard Shi (Univ. of Washington, United States)

1D-3 A 16-Bit, Low-Power Microsystem with Monolithic MEMS-LC Clocking
Robert M. Senger, Eric D. Marsman, Michael S. McCorquodale (Univ. of Michigan, United States), Richard B. Brown (Univ. of Utah, United States)

1D-4 Ultra-Low Voltage Power Management Circuit and Computation Methodology for Energy Harvesting Applications
Chi-Ying Tsui, Hui Shao, Wing-Hung Ki, Feng Su (Hong Kong Univ. of Science and Tech., Hong Kong)

1D-5 A 0.5-V Sigma-Delta Modulator Using Analog T-Switch Scheme for the Subthreshold Leakage Suppression
Koichi Ishida, Atit Tamtrakarn, Takayasu Sakurai (Univ. of Tokyo, Japan)

1D-6 An Implementation of a CMOS Down-Conversion Mixer for GSM1900 Receiver
Fangqing Chu, Wei Li, Junyan Ren (Fudan Univ., China)

1D-7 Integrated Direct Output Current Control Switching Converter using Symmetrically-Matched Self-Biased Current Sensors
Yat-Hei Lam (Hong Kong Univ. of Science and Tech., Hong Kong), Suet-Chui Koon (National Semiconductor Co., Hong Kong), Wing-Hung Ki, Chi-Ying Tsui (Hong Kong Univ. of Science and Tech., Hong Kong)

1D-8 Adaptively-Biased Capacitor-Less CMOS Low Dropout Regulator with Direct Current Feedback
Yat-Hei Lam, Wing-Hung Ki, Chi-Ying Tsui (Hong Kong Univ. of Science and Tech., Hong Kong)

1D-9 A Built-in Power Supply Noise Probe for Digital LSIs
Mitsuya Fukazawa, Koichiro Noguchi, Makoto Nagata, Kazuo Taki (Kobe Univ., Japan)

1D-10 A 476-gate-count Dynamic Optically Reconfigurable Gate Array VLSI chip in a standard 0.35um CMOS Technology
Minoru Watanabe, Fuminori Kobayashi (Kyushu Inst. of Tech., Japan)

1D-11 Measurement Results of Within-Die Variations on a 90nm LUT Array for Speed and Yield Enhancement of Reconfigurable Devices
Kazuya Katsuki, Manabu Kotani, Kazutoshi Kobayashi, Hidetoshi Onodera (Kyoto Univ., Japan)

1D-12 High-Throughput Decoder for Low-Density Parity-Check Code
Tatsuyuki Ishikawa, Kazunori Shimizu, Takeshi Ikenaga, Satoshi Goto (Waseda Univ., Japan)

1D-13 Hardware Implementation of Super Minimum All Digital FM Demodulator
Nursani Rahmatullah, Arif Nugroho (Institut Teknologi Bandung, Indonesia)

1D-14 Designing a Custom Architecture for DCT Using NISC Technology
Bita Gorjiara, Mehrdad Reshadi, Daniel Gajski (Univ. of California, Irvine, United States)

1D-15 A 52mW 1200MIPS Compact DSP for Multi-Core Media SoC
Shih-Hao Ou, Tay-Jyi Lin, Chao-Wei Huang, Yu-Ting Kuo, Chie-Min Chao, Chih-Wei Liu (National Chiao Tung Univ., Taiwan), Chein-Wei Jen (STC, ITRI, Taiwan)

1D-16 Implementation of H.264/AVC Decoder for Mobile Video Applications
Suh Ho Lee, Ji Hwan Park, Seon Wook Kim, Sung Jea Ko, Suki Kim (Korea Univ., Republic of Korea)

1D-17 A High-Performance Platform-Based SoC for Information Security
Min Wu, Xiaoyang Zeng, Jun Han, Yongyi Wu, Yibo Fan (Fudan Univ., China)

1D-18 Configurable Multi-Processor Architecture and its Processor Element Design
Tsutomu Nishimura, Takuji Miki, Hiroaki Sugiura, Yuki Matsumoto, Masatsugu Kobayashi, Toshiyuki Kato, Tsutomu Eda, Hironori Yamauchi (Ritsumeikan Univ., Japan)

1D-19 Design and Implementation of Transducer for ARM-TMS Communication
Hansu Cho, Samar Abdi, Daniel Gajski (Univ. of California, Irvine, United States)

Wednesday, January 25, 13:30 - 15:35

Wednesday, January 25, 13:30 - 15:35 Room 411+412
Session 2A: Software Techniques for Efficient SoC Design

Chair(s): ***Qiang Zhu*** – Fujitsu Lab., Japan
Ahmed Jerraya – TIMA Laboratory, France

2A-1 Energy Savings through Embedded Processing on Disk System
Seung Woo Son, Guangyu Chen, Mahmut Kandemir, Fehui Li (Pennsylvania State Univ., United States)

2A-2 Energy-Aware Computation Duplication for Improving Reliability in Embedded Chip Multiprocessors
Guilin Chen, Mahmut Kandemir, Feihui Li (Pennsylvania State Univ., United States)

2A-3 Object Duplication for Improving Reliability
Guilin Chen, Guangyu Chen, Mahmut Kandemir, Narayanan Vijaykrishnan, Mary Jane Irwin (Pennsylvania State Univ., United States)

2A-4 Mapping and Configuration Methods for Multi-Use-Case Networks on Chips
Srinivasan Murali (Stanford Univ., United States), Martijn Coenen, Andrei Radulescu, Kees Goossens (Philips, Netherlands), Giovanni De Micheli (EPFL, Switzerland)

2A-5 Conversion of Reference C Code to Dataflow Model: H.264 Encoder Case Study
Hyeyoung Hwang, Taewook Oh, Hyunuk Jung, Soonhoi Ha (Seoul National Univ., Republic of Korea)

Wednesday, January 25, 13:30 - 15:35 Room 413
Session 2B: Application Examples with Leading Edge Design Methodology

Chair(s): ***In-Cheol Park*** – KAIST, Republic of Korea
Hideharu Amano – Keio Univ., Japan

2B-1 SAVS: A Self-Adaptive Variable Supply-Voltage Technique for Process -Tolerant and Power-Efficient Multi-issue Superscalar Processor Design
Hai Li (Qualcomm Inc., United States), Yiran Chen (Synopsys Inc., United States), Kaushik Roy, Cheng-Kok Koh (Purdue Univ., United States)

2B-2 The Design and Implementation of a Low-Latency On-Chip Network
Robert Mullins, Andrew West, Simon Moore (Univ. of Cambridge, Great Britain)

2B-3 A Near Optimal Deblocking Filter for H.264 Advanced Video Coding
Shen-Yu Shih, Cheng-Ru Chang, Youn-Long Lin (National Tsing Hua Univ., Taiwan)

2B-4 Image Segmentation and Pattern Matching Based FPGA/ASIC Implementation Architecture of Real-Time Object Tracking
Kousuke Yamaoka, Takashi Morimoto, Hidekazu Adachi, Tetsushi Koide, Hans Juergen Mattausch (Hiroshima Univ., Japan)

2B-5 Prefetching-Aware Cache Line Turnoff for Saving Leakage Energy
Ismail Kadayif (Canakkale Onsekiz Mart Univ., Turkey), Mahmut Kandemir, Feihui Li (Pennsylvania State Univ., United States)

Wednesday, January 25, 13:30 - 15:35 Room 414+415
Session 2C: Placement

Chair(s): ***Evangeline F.Y. Young*** – Chinese Univ. of Hong Kong, Hong Kong
Shin'ichi Wakabayashi – Hiroshima City Univ., Japan

2C-1 A Robust Detailed Placement for Mixed-Size IC Designs
Jason Cong, Min Xie (Univ. of California, Los Angeles, United States)

2C-2 FastPlace 2.0: An Efficient Analytical Placer for Mixed-Mode Designs
Natarajan Viswanathan, Min Pan, Chris Chu (Iowa State Univ., United States)

2C-3 Timing-Driven Placement Based on Monotone Cell Ordering Constraints
Chanseok Hwang, Massoud Pedram (Univ. of Southern California, United States)

2C-4 Constraint Driven I/O Planning and Placement for Chip-package Co-design
Jinjun Xiong (Univ. of California, Los Angeles, United States), Yiu-Chung Wong, Egino Sarto (Rio Design Automation, United States), Lei He (Univ. of California, Los Angeles, United States)

2C-5 Simultaneous Block and I/O Buffer Floorplanning for Flip-Chip Design
Chih-Yang Peng, Wen-Chang Chao, Yao-Wen Chang (National Taiwan Univ., Taiwan), J.-H. Wang (Faraday Technology Corp., Taiwan)

Wednesday, January 25, 13:30 - 15:35 Room 416+417
Session 2D: Special Session: Electrothermal Design of Nanoscale Integrated Circuits

Chair(s): ***Dennis Sylvester*** – Univ. of Michigan, United States
Mongkol Ekpanyapong – Georgia Inst. of Tech., United States

2D-1 Electrothermal Analysis and Optimization Techniques for Nanoscale Integrated Circuits
Yong Zhan, Brent Goplen, Sachin S. Sapatnekar (Univ. of Minnesota, United States)

2D-2 Electrothermal Engineering in the Nanometer Era: From Devices and Interconnects to Circuits and Systems
Kaustav Banerjee, Sheng-Chih Lin, Navin Srivastava (Univ. of California, Santa Barbara, United States)

2D-3 Area Optimization for Leakage Reduction and Thermal Stability in Nanometer Scale Technologies
Ja Chun Ku, Yehea Ismail (Northwestern Univ., United States)

2D-4 Compact Thermal Models for Estimation of Temperature-dependent Power/Performance in FinFET Technology
Aditya Bansal, Mesut Meterelliyoz (Purdue Univ., United States), Siddharth Singh (Osmania Univerisity, India), Jung Hwan Choi, Jayathi Murthy, Kaushik Roy (Purdue Univ., United States)

Wednesday, January 25, 16:00 - 18:05

Wednesday, January 25, 16:00 - 18:05 Room 411+412
Session 3A: Logic Synthesis

Chair(s): ***Shinji Kimura*** – Waseda Univ., Japan
Shih-Chieh Chang – National Tsing Hua Univ., Taiwan

3A-1 An Anytime Symmetry Detection Algorithm for ROBDDs
Neil Kettle, Andy King (Univ. of Kent, Great Britain)

3A-2 High Level Equivalence Symmetric Input Identification
Ming-Hong Su, Chun-Yao Wang (National Tsing Hua Univ., Taiwan)

3A-3 Fast Multi-Domain Clock Skew Scheduling for Peak Current Reduction
Shih-Hsu Huang, Chia-Ming Chang, Yow-Tyng Nieh (Chung Yuan Christian Univ., Taiwan)

3A-4 Low Area Pipelined Circuits by Multi-clock Cycle Paths and Clock Scheduling
Bakhtiar Affendi Rosdi, Atsushi Takahashi (Tokyo Inst. of Tech., Japan)

3A-5 A Transduction-based Framework to Synthesize RSFQ Circuits
Shigeru Yamashita (NAIST, Japan), Katsunori Tanaka (NEC, Japan), Hideyuki Takada (Kyoto Univ., Japan), Koji Obata, Kazuyoshi Takagi (Nagoya Univ., Japan)

Wednesday, January 25, 16:00 - 18:05 Room 413
Session 3B: Future Technical Directions for Design Automation

Chair(s): ***Makoto Nagata*** – Kobe Univ., Japan
Ryuichi Fujimoto – Toshiba, Japan

3B-1 Fast Simulation of Large Networks of Nanotechnological and Biochemical Oscillators for Investigating Self-Organization Phenomena
Xiaolue Lai, Jaijeet Roychowdhury (Univ. of Minnesota, United States)

3B-2 Newton: A Library-Based Analytical Synthesis Tool for RF-MEMS Resonators
Michael S. McCorquodale (Mobius Microsystems, Inc., United States), James L. McCann (Carnegie Mellon Univ., United States), Richard B. Brown (Univ. of Utah, United States)

3B-3 Jitter Decomposition in Ring Oscillators
Qingqi Dou, Jacob Abraham (Univ. of Texas, Austin, United States)

3B-4 A Fast Methodology for First-Time-Correct Design of PLLs Using Nonlinear Phase-Domain VCO Macromodels
Prashant Goyal (Indian Inst. of Tech., Kanpur, India), Xiaolue Lai, Jaijeet Roychowdhury (Univ. of Minnesota, United States)

3B-5 Double Edge Triggered Feedback Flip-Flop in Sub 100nm Technology
Seid Hadi Rasouli, Amir Amirabadi, Azam Seyedi, Ali Afzali-Kusha (Univ. of Tehran, Iran)

Wednesday, January 25, 16:00 - 18:05 Room 414+415
Session 3C: Routing and Interconnect Optimization

Chair(s): ***Youichi Shiraishi*** – Gunma Univ., Japan
Tong Jing – Tsinghua Univ., China

3C-1 Post-Routing Redundant Via Insertion for Yield/Reliability Improvement
Kuang-Yao Lee, Ting-Chi Wang (National Tsing Hua Univ., Taiwan)

3C-2 Temperature-Aware Routing in 3D ICs
Tianpei Zhang, Yong Zhan, Sachin S. Sapatnekar (Univ. of Minnesota, United States)

3C-3 Closed Form Solution for Optimal Buffer Sizing Using The Weierstrass Elliptic Function
Sebastian Vogel (Darmstadt Univ. of Tech., Germany), Martin D.F. Wong (Univ. of Illinois, Urbana-Champaign, United States)

3C-4 An O(mn) Time Algorithm for Optimal Buffer Insertion of Nets with m Sinks
Zhuo Robert Li, Weiping Shi (Texas A&M Univ., United States)

3C-5 Spec-based Flip-Flop and Latch Repeater Planning
Man Chung Hon (Intel Co., United States)

Wednesday, January 25, 16:00 - 18:05 Room 416+417
Session 3D: Special Session: Flash Memory in Embedded Systems

Chair(s): ***Tohru Ishihara*** – Kyushu Univ., Japan
Hiroyuki Tomiyama – Nagoya Univ., Japan

3D-1 Current Trends in Flash Memory Technology
Sang Lyul Min, Eyee Hyun Nam (Seoul National Univ., Republic of Korea)

3D-2 Configurability of Performance and Overheads in Flash Management
Tei-Wei Kuo, Jen-Wei Hsieh (National Taiwan Univ., Taiwan), Li-Pin Chang (National Chiao-Tung Univ., Taiwan), Yuan-Hao Chang (National Taiwan Univ., Taiwan)

Thursday, January 26, 9:00 - 10:00

Thursday, January 26, 9:00 - 10:00 Small Auditorium, 5F
Keynote Address II :

Chair(s): ***Fumiyasu Hirose*** – Cadence, Japan

Challenging Device Innovation
Satoru Ito (President & CEO, RENESAS Technology Corp., Japan)

Thursday, January 26, 10:15 - 12:20

Thursday, January 26, 10:15 - 12:20 Room 411+412
Session 4A: Resolving Timing Issues: Design and Test

Chair(s): ***Masaki Hashizume*** – Tokushima Univ., Japan
Kazumi Hatayama – Renesas, Japan

4A-1 Delay Defect Screening for a 2.16GHz SPARC64 Microprocessor
Noriyuki Ito, Akira Kanuma, Daisuke Maruyama, Hitoshi Yamanaka, Tsuyoshi Mochizuki, Osamu Sugawara, Chihiro Endoh, Masahiro Yanagida, Takeshi Kono, Yutaka Isoda, Kazunobu Adachi, Takahisa Hiraide, Shigeru Nagasawa, Yaroku Sugiyama, Eizo Ninoi (Fujitsu, Japan)

4A-2 A Dynamic Test Compaction Procedure for High-quality Path Delay Testing
Masayasu Fukunaga (Fujitsu, Japan), Seiji Kajihara, Xiaoqing Wen (Kyushu Inst. of Tech., Japan), Toshiyuki Maeda, Shuji Hamada, Yasuo Sato (STARC, Japan)

4A-3 Delay Variation Tolerance for Domino Circuits
Kai-Chiang Wu, Cheng-Tao Hsieh, Shih-Chieh Chang (National Tsing Hua Univ., Taiwan)

4A-4 Efficient Identification of Multi-Cycle False Path
Kai Yang, Tim Cheng (Univ. of California, Santa Barbara, United States)

4A-5 IEEE Standard 1500 Compatible Interconnect Diagnosis for Delay and Crosstalk Faults
Katherine Shu-Min Li (National Chiao Tung Univ., Taiwan), Yao-Wen Chang (National Taiwan Univ., Taiwan), Chauchin Su, Chung-Len Lee (National Chiao Tung Univ., Taiwan), Jwu E Chen (National Central Univ., Taiwan)

Thursday, January 26, 10:15 - 12:20 Room 413
Session 4B: Leading Edge Design Methodology for SoCs and SiPs

Chair(s): ***Satoshi Matsushita*** – NEC, Japan

4B-1 High-Level Architecture Exploration for MPEG4 Encoder with Custom Parameters
Marius Bonaciu, Aimen Bouchhima, Wassim Youssef, Xi Chen (TIMA Laboratory, France), Wander Cesario (MND, France), Ahmed Jerraya (TIMA Laboratory, France)

4B-2 Programmable Numerical Function Generators Based on Quadratic Approximation: Architecture and Synthesis Method
Shinobu Nagayama (Hiroshima City Univ., Japan), Tsutomu Sasao (Kyushu Inst. of Tech., Japan), Jon Butler (Naval Postgraduate School, United States)

4B-3 An Automated Design Flow for 3D Microarchitecture Evaluation
Jason Cong, Ashok Jagannathan, Yuchun Ma, Glenn Reinman, Jie Wei, Yan Zhang (Univ. of California, Los Angeles, United States)

4B-4 Optimal Topology Exploration for Application-Specific 3D Architectures
Ozcan Ozturk, Feng Wang, Mahmut Kandemir, Yuan Xie (Pennsylvania State Univ., United States)

4B-5 Task Placement Heuristic Based on 3D-Adjacency and Look-Ahead in Reconfigurable Systems
Jesus Tabero (Instituto Nacional de Tecnica Aeroespacial, Spain), Julio Septien, Hortensia Mecha, Daniel Mozos (Univ. Complutense de Madrid, Spain)

Thursday, January 26, 10:15 - 12:20 Room 414+415
Session 4C: Advanced Circuit Simulation

Chair(s): ***Hideki Asai*** – Shizuoka Univ., Japan
C.J. Richard Shi – Washington Univ., United States

4C-1 A Quasi-Newton Preconditioned Newton-Krylov Method for Robust and Efficient Time-Domain Simulation of Integrated Circuits with Strong Parasitic Couplings
Zhao Li (Cadence Design Systems, United States), Richard Shi (Univ. of Washington, United States)

4C-2 An Efficient and Globally Convergent Homotopy Method for Finding DC Operating Points of Nonlinear Circuits
Kiyotaka Yamamura, Wataru Kuroki (Chuo Univ., Japan)

4C-3 Optimization of Circuit Trajectories: An Auxiliary Network Approach
Baohua Wang, Pinaki Mazumder (Univ. of Michigan, United States)

4C-4 SASIMI: Sparsity-Aware Simulation of Interconnect-Dominated Circuits with Non-Linear Devices
Jitesh Jain, Stephen F Cauley, Cheng-Kok Koh, Venkataramanan Balakrishnan (Purdue Univ., United States)

4C-5 An Unconditional Stable General Operator Splitting Method for Transistor Level Transient Analysis
Zhengyong Zhu, Rui Shi, Chung-Kuan Cheng (Univ. of California, San Diego, United States), Ernest S. Kuh (Univ. of California, Berkeley, United States)

Thursday, January 26, 10:15 - 12:20 Room 416+417
Session 4D: Special Session: Open Access Overview

Chair(s): ***John Darringer*** – IBM, United States

4D-1 An Introduction to OpenAccess -An Open Source Data Model and API for IC Design-
Michaela Guiney, Eric Leavitt (Cadence, United States)

4D-2 Open Access Overview "Industrial Experience"
Yoshio Inoue (Renesas, Japan)

4D-3 EDA Vendor Adoption
Hillel Ofek (Sagantec, United States)

4D-4 Utility of the OpenAccess Database in Academic Research
David Papa, Igor Markov (Univ. of Michigan, United States), Philip Chong (Cadence Design Systems, United States)

Thursday, January 26, 13:30 - 15:35

Thursday, January 26, 13:30 - 15:35 Room 411+412
Session 5A: Advances in Simulation Technologies

Chair(s): ***Shin'ichi Minato*** – Hokkaido Univ., Japan
Karem Sakallah – Univ. of Michigan, United States

5A-1 Depth-Driven Verification of Simultaneous Interfaces
Ilya Wagner, Valeria Bertacco, Todd Austin (Univ. of Michigan, United States)

5A-2 FSM-Based Transaction-Level Functional Coverage for Interface Compliance Verification
Man-Yun Su, Che-Hua Shih, Juinn-Dar Huang, Jing-Yang Jou (National Chiao Tung Univ., Taiwan)

5A-3 Hardware Debugging Method Based on Signal Transitions and Transactions
Nobuyuki Ohba, Kohji Takano (IBM Japan, Japan)

5A-4 Cycle Error Correction in Asynchronous Clock Modeling for Cycle-Based Simulation
Junghee Lee, Joonhwan Yi (Samsung Electronics, Republic of Korea)

5A-5 A Fast Logic Simulator Using a Look Up Table Cascade Emulator
Hiroki Nakahara, Tsutomu Sasao, Munehiro Matsuura (Kyushu Inst. of Tech., Japan)

Thursday, January 26, 13:30 - 15:35 Room 413
Session 5B: Scheduling for Embedded Systems

Chair(s): ***Sri Parameswaran*** – Univ. of New South Wales, Australia
Sang Lyul Min – Seoul National Univ., Republic of Korea

5B-1 Power-Aware Scheduling and Dynamic Voltage Setting for Tasks Running on a Hard Real-Time System
Peng Rong, Massoud Pedram (Univ. of Southern California, United States)

5B-2 Optimal TDMA Time Slot and Cycle Length Allocation for Hard Real-Time Systems
Ernesto Wandeler, Lothar Thiele (ETH Zurich, Switzerland)

5B-3 POSIX modeling in SystemC
Hector Posadas, Jesus Adamez, Pablo Sanchez, Eugenio Villar (Univ. of Cantabria, Spain), Francisco Blasco (DS2, Spain)

5B-4 PARLGRAN: Parallelism Granularity Selection for Scheduling Task Chains on Dynamically Reconfigurable Architectures
Sudarshan Banerjee, Elaheh Bozorgzadeh, Nikil Dutt (Univ. of California, Irvine, United States)

5B-5 Memory Optimal Single Appearance Schedule with Dynamic Loop Count for Synchronous Dataflow Graphs
Hyunok Oh, Nikil Dutt (Univ. of California, Irvine, United States), Soonhoi Ha (Seoul National Univ., Republic of Korea)

Thursday, January 26, 13:30 - 15:35 Room 414+415
Session 5C: High Frequency Interconnect Effects in Nanometer Technology

Chair(s): ***Charlie Chung-Ping Chen*** – National Taiwan Univ., Taiwan
Noel Menezes – Intel, United States

5C-1 Wire Sizing with Scattering Effect for Nanoscale Interconnection
Sean X. Shi, David Z. Pan (Univ. of Texas, Austin, United States)

5C-2 Adaptive Admittance-based Conductor Meshing for Interconnect Analysis
Ya-Chi Yang, Cheng-Kok Koh, Venkataramanan Balakrishnan (Purdue Univ., United States)

5C-3 Interconnect RL Extraction at a Single Representative Frequency
Akira Tsuchiya (Kyoto Univ., Japan), Masanori Hashimoto (Osaka Univ., Japan), Hidetoshi Onodera (Kyoto Univ., Japan)

5C-4 An Efficient Algorithm for 3-D Reluctance Extraction Considering High Frequency Effect
Mengsheng Zhang, Wenjian Yu (Tsinghua Univ., China), Yu Du (Synopsys Inc., United States), Zeyi Wang (Tsinghua Univ., China)

5C-5 Macromodelling Oscillators Using Krylov-Subspace Methods
Xiaolue Lai, Jaijeet Roychowdhury (Univ. of Minnesota, United States)

Thursday, January 26, 13:30 - 15:30 Small Auditorium, 5F
Session 5D: Designers' Forum: Low Power Design

Chair(s): ***Haruyuki Tago*** – Toshiba, Japan
Makoto Ikeda – Univ. of Tokyo, Japan

5D-1 Low-Power Design Methodology for Module-wise Dynamic Voltage and Frequency Scaling with Dynamic De-skewing Systems
Takeshi Kitahara, Hiroyuki Hara, Shinichiro Shiratake (Toshiba, Japan), Yoshiki Tsukiboshi (Toshiba Microelectronics Co., Japan), Tomoyuki Yoda, Tetsuaki Utsumi, Fumihiro Minami (Toshiba, Japan)

5D-2 Single-Chip Multi-Processor Integrating Quadruple 8-Way VLIW Processors with Interface Timing Analysis Considering Power Supply Noise
Satoshi Imai, Atsuki Inoue, Motoaki Matsumura, Kenichi Kawasaki, Atsuhiro Suga (Fujitsu Lab., Japan)

5D-3 A System-level Power-estimation Methodology based on IP-level Modeling, Power-level Adjustment, and Power Accumulation
Masafumi Onouchi, Tetsuya Yamada (Hitachi Ltd., Japan), Kimihiro Morikawa, Isamu Mochizuki, Hidetoshi Sekine (Renesas, Japan)

5D-4 PowerViP: SoC Power Estimation Framework at Transaction Level
Ikhwan Lee, Hyunsuk Kim, Peng Yang, Sungjoo Yoo (Samsung Electronics, Republic of Korea), Eui-Young Chung (Yonsei Univ., Republic of Korea), Kyu-Myung Choi, Jeong-Taek Kong, Soo-Kwan Eo (Samsung Electronics, Republic of Korea)

Thursday, January 26, 16:00 - 18:05

Thursday, January 26, 16:00 - 18:05 Room 411+412
Session 6A: Power Optimization of Large-Scale Circuits

Chair(s): ***Sheldon Tan*** – Univ. of California, Riverside, United States
David Z. Pan – Univ. of Texas, Austin, United States

6A-1 Mathematically Assisted Adaptive Body Bias (ABB) for Temperature Compensation in Gigascale LSI Systems
Sanjay V Kumar, Chris H Kim, Sachin S Sapatnekar (Univ. of Minnesota, United States)

6A-2 Analysis and Optimization of Gate Leakage Current of Power Gating Circuits
Hyung-Ock Kim, Youngsoo Shin (KAIST, Republic of Korea)

6A-3 Delay Modeling and Static Timing Analysis for MTCMOS Circuits
Naoaki Ohkubo, Kimiyoshi Usami (Shibaura Inst. of Tech., Japan)

6A-4 Switching-Activity Driven Gate Sizing and Vth Assignment for Low Power Design
Yu-Hui Huang, Po-Yuan Chen, TingTing Hwang (National Tsing Hua Univ., Taiwan)

6A-5 Power Driven Placement with Layout Aware Supply Voltage Assignment for Voltage Island Generation in Dual-Vdd Designs
Bin Liu, Yici Cai, Qiang Zhou, Xianlong Hong (Tsinghua Univ., China)

Thursday, January 26, 16:00 - 18:05 Room 413
Session 6B: Advanced Memory and Processor Architectures for MPSoC

Chair(s): ***Soonhoi Ha*** – Seoul National Univ., Republic of Korea
Youn-Long Lin – National Tsing Hua Univ., Taiwan

6B-1 Reusable Component IP Design using Refinement-based Design Environment
Sanggyu Park, Sang-Yong Yoon, Soo-Ik Chae (Seoul National Univ., Republic of Korea)

6B-2 An Interface-Circuit Synthesis Method with Configurable Processor Core in IP-Based SoC Designs
Shunitsu Kohara, Naoki Tomono, Jumpei Uchida, Yuichiro Miyaoka, Nozomu Togawa, Masao Yanagisawa, Tatsuo Ohtsuki (Waseda Univ., Japan)

6B-3 A Real-Time and Bandwidth Guaranteed Arbitration Algorithm for SoC Bus Communication
Chien-Hua Chen, Geeng-Wei Lee, Juinn-Dar Huang, Jing-Yang Jou (National Chiao Tung Univ., Taiwan)

6B-4 Hierarchical Memory Size Estimation for Loop Fusion and Loop Shifting in Data-Dominated Applications
Qubo Hu (Univ. of Trondheim, Norway), Arnout Vandecappelle, Martin Palkovic (IMEC, Belgium), Per Gunnar Kjeldsberg (Univ. of Trondheim, Norway), Erik Brockmeyer, Francky Catthoor (IMEC, Belgium)

6B-5 A Novel Instruction Scratchpad Memory Optimization Method based on Concomitance Metric
Andhi Janapsatya, Aleksandar Ignjatovic, Sri Parameswaran (Univ. of New South Wales, Australia)

Thursday, January 26, 16:00 - 18:05 Room 414+415
Session 6C: New Routing Techniques

Chair(s): ***Ting-Chi Wang*** – National Tsing Hua Univ., Taiwan
Vijay Pitchumani – Intel, United States

6C-1 DraXRouter: Global Routing in X-Architecture with Dynamic Resource Assignment
Zhen Cao, Tong Jing (Tsinghua Univ., China), Yu Hu, Yiyu Shi (Univ. of California, Los Angeles, United States), Xianlong Hong (Tsinghua Univ., China), Xiaodong Hu, Guiying Yan (Institute of Applied Mathematics, Chinese Academy of Sciences, China)

6C-2 Diagonal Routing in High Performance Microprocessor Design
Noriyuki Ito, Hideaki Katagiri, Ryoichi Yamashita, Hiroshi Ikeda, Hiroyuki Sugiyama, Hiroaki Komatsu, Yoshiyasu Tanamura, Akihiko Yoshitake, Kazuhiro Nonomura, Kinya Ishizaka, Hiroaki Adachi, Yutaka Mori, Yutaka Isoda, Yaroku Sugiyama (Fujitsu, Japan)

6C-3 CDCTree: Novel Obstacle-Avoiding Routing Tree Construction based on Current Driven Circuit Model
Yiyu Shi (Univ. of California, Los Angeles, United States), Tong Jing (Tsinghua Univ., China), Lei He (Univ. of California, Los Angeles, United States), Zhe Feng, Xianlong Hong (Tsinghua Univ., China)

6C-4 A Novel Framework for Multilevel Full-Chip Gridless Routing
Tai-Chen Chen, Yao-Wen Chang (National Taiwan Univ., Taiwan), Shyh-Chang Lin (SpringSoft, Inc., Taiwan)

6C-5 Monotonic Parallel and Orthogonal Routing for Single-Layer Ball Grid Array Packages
Yoichi Tomioka, Atsushi Takahashi (Tokyo Inst. of Tech., Japan)

Thursday, January 26, 16:30 - 18:00 Small Auditorium, 5F
Session 6D: Designers' Forum Panel: Functional Verification -now and future-

Organizer: ***Haruyuki Tago*** – TOSHIBA, Japan
Moderator: ***Yoshio Masubuchi*** – TOSHIBA, Japan
Panelists: ***Sanjay Gupta*** – IBM, United States
Michael Stellfox – Cadence, United States
Tetsuji Sumioka – Sony, Japan
Sunao Torii – NEC, Japan

Friday, January 27, 9:00 - 10:00

Friday, January 27, 9:00 - 10:00 Small Auditorium, 5F
Keynote Address III :

Chair(s): ***Fumiyasu Hirose*** – Cadence, Japan

Effective Platform-based Development for Large-scale Systems Design
Yukichi Niwa (Senior Advisory Director, Group Executive of Platform Technology Development Headquarters, CANON INC., Japan)

Friday, January 27, 10:15 - 12:20

Friday, January 27, 10:15 - 12:20 Room 411+412
Session 7A: Minimization of Test Cost and Power

Chair(s): ***Seiji Kajihara*** – Kyushu Inst. of Tech., Japan
Satoshi Ohtake – NAIST, Japan

7A-1 A Routability Constrained Scan Chain Ordering Technique for Test Power Reduction
Xuan-Lun Huang, Jiun-Lang Huang (National Taiwan Univ., Taiwan)

7A-2 FCSCAN: An Efficient Multiscan-based Test Compression Technique for Test Cost Reduction
Youhua Shi, Nozomu Togawa, Shinji Kimura, Masao Yanagisawa, Tatsuo Ohtsuki (Waseda Univ., Japan)

7A-3 Compaction of Pass/Fail-based Diagnostic Test Vectors for Combinational and Sequential Circuits
Yoshinobu Higami (Ehime Univ., Japan), Kewal K. Saluja (Univ. of Wisconsin-Madison, United States), Hiroshi Takahashi, Shin-ya Kobayashi, Yuzo Takamatsu (Ehime Univ., Japan)

7A-4 Low-Overhead Design of Soft-Error-Tolerant Scan Flip-Flops with Enhanced-Scan Capability
Ashish Goel (Purdue Univ., United States), Swarup Bhunia (Case Western Reserve Univ., United States), Hamid Mahmoodi (San Francisco State Univ., United States), Kaushik Roy (Purdue Univ., United States)

7A-5 A Memory Grouping Method for Sharing Memory BIST Logic
Masahide Miyazaki, Tomokazu Yoneda, Hideo Fujiwara (NAIST, Japan)

Friday, January 27, 10:15 - 12:20 Room 413
Session 7B: Substrate Coupling and Analog Synthesis

Chair(s): ***Jaijeet Roychowdhury*** – Univ. of Minnesota, United States
Tomohisa Kimura – Toshiba, Japan

7B-1 Equivalent Circuit Modeling of Guard Ring Structures for Evaluation of Substrate Crosstalk Isolation
Daisuke Kosaka, Makoto Nagata (Kobe Univ., Japan)

7B-2 A New Boundary Element Method for Accurate Modeling of Lossy Substrates with Arbitrary Doping Profiles
Xiren Wang, Wenjian Yu, Zeyi Wang (Tsinghua Univ., China)

7B-3 Parasitics Extraction Involving 3-D Conductors based on Multi-layered Green's Function
Zuochang Ye, Zhiping Yu (Tsinghua Univ., China)

7B-4 Signal-Path Driven Partition and Placement for Analog Circuit
Di Long, Xianlong Hong, Sheqin Dong (Tsinghua Univ., China)

7B-5 An Approach to Topology Synthesis of Analog Circuits Using Hierarchical Blocks and Symbolic Analysis
Xiaoying Wang, Lars Hedrich (Univ. of Frankfurt, Germany)

Friday, January 27, 10:15 - 12:20 Room 414+415
Session 7C: Statistical and Yield Analysis

Chair(s): ***Hiroo Masuda*** – STARC, Japan
Seijiro Moriyama – PDF Solutions, Japan

7C-1 Statistical Corner Conditions of Interconnect Delay (Corner LPE Specifications)
Kenta Yamada, Noriaki Oda (NEC Electronics, Japan)

7C-2 Speed Binning Aware Design Methodology to Improve Profit under Parameter Variations
Animesh Datta (Purdue Univ., United States), Swarup Bhunia (Case Western Reserve Univ., United States), Jung Hwan Choi, Saibal Mukhopadhyay, Kaushik Roy (Purdue Univ., United States)

7C-3 Yield-Area Optimizations of Digital Circuits Using Non-dominated Sorting Genetic Algorithm (YOGA)
Vineet Agarwal, Janet Wang (Univ. of Arizona, United States)

7C-4 A Probabilistic Analysis of Pipelined Global Interconnect Under Process Variations
Navneeth Kankani, Vineet Agarwal, Janet M Wang (Univ. of Arizona, United States)

7C-5 Yield-Preferred Via Insertion Based on Novel Geotopological Technology
Fangyi Luo (Univ. of California, Santa Cruz, United States), Yongbo Jia (Nannor Technologies, Inc., United States), Wayne Wei-Ming Dai (Univ. of California, Santa Cruz, United States)

Friday, January 27, 10:15 - 12:20 Room 416+417
Session 7D: Special Session: H.264/AVC Design Challenges and Solutions

Chair(s): ***Wayne Wolf*** – Princeton Univ., United States

7D-1 Introduction to H.264 Advanced Video Coding
Jian-Wen Chen, Chao-Yang Kao, Youn-Long Lin (National Tsing Hua Univ., Taiwan)

7D-2 Algorithms and DSP Implementation of H.264/AVC
Hung-Chih Lin, Yu-Jen Wang, Kai-Ting Cheng, Shang-Yu Yeh, Wei-Nien Chen, Chia-Yang Tsai, Tian-Sheuan Chang, Hsueh-Ming Hang (National Chiao-Tung Univ., Taiwan)

7D-3 Hardware Architecture Design of an H.264/AVC Video Codec
Tung-Chien Chen, Chung-Jr Lian, Liang-Gee Chen (National Taiwan Univ., Taiwan)

7D-4 ASIP Approach for Implementation of H.264/AVC
Sung Dae Kim, Jeong Hoo Lee, Chung Jin Hyun, Myung Hoon Sunwoo (Ajou Univ., Republic of Korea)

7D-5 Panel Discussion
Youn-Long Lin (National Tsing Hua Univ., Taiwan), Hsueh-Ming Hang (National Chiao-Tung Univ., Taiwan), Liang-Gee Chen (National Taiwan Univ., Taiwan), Myung Hoon Sunwoo (Ajou Univ., Republic of Korea)

Friday, January 27, 13:30 - 15:35

Friday, January 27, 13:30 - 15:35 Room 411+412
Session 8A: Floorplanning

Chair(s): ***Yao-Wen Chang*** – National Taiwan Univ., Taiwan
Shigetoshi Nakatake – Univ. of Kitakyushu, Japan

8A-1 Fast Substrate Noise-Aware Floorplanning with Preference Directed Graph for Mixed-Signal SOCs
Minsik Cho, Hongjoong Shin, David Z. Pan (Univ. of Texas, Austin, United States)

8A-2 A Fixed-die Floorplanning Algorithm Using an Analytical Approach
Yong Zhan, Yan Feng, Sachin S. Sapatnekar (Univ. of Minnesota, United States)

8A-3 A Multi-Technology-Process Reticle Floorplanner and Wafer Dicing Planner for Multi-Project Wafers
Chien-Chang Chen, Wai-Kei Mak (National Tsing Hua Univ., Taiwan)

8A-4 Design Space Exploration for Minimizing Multi-Project Wafer Production Cost
Rung-Bin Lin, Meng-Chiou Wu, Wei-Chiu Tseng, Ming-Hsine Kuo, Tsai-Ying Lin, Shr-Cheng Tsai (Yuan Ze Univ., Taiwan)

8A-5 SAT-Based Optimal Hypergraph Partitioning with Replication
Michael G. Wrighton (Tabula, Inc., United States), Andre M. DeHon (California Inst. of Tech., United States)

Friday, January 27, 13:30 - 15:35 Room 413
Session 8B: Memory Optimization for Embedded Systems

Chair(s): ***Hiroyuki Tomiyama*** – Nagoya Univ., Japan
Preeti Ranjan Panda – Indian Inst. of Tech., Delhi, India

8B-1 Finding Optimal L1 Cache Configuration for Embedded Systems
Andhi Janapsatya, Aleksandar Ignjatovic, Sri Parameswaran (Univ. of New South Wales, Australia)

8B-2 Memory Size Computation for Multimedia Processing Applications
Hongwei Zhu, Ilie I. Luican, Florin Balasa (Univ. of Illinois, Chicago, United States)

8B-3 Maximizing Data Reuse for Minimizing Memory Space Requirements and Execution Cycles
Mahmut Kandemir, Guangyu Chen, Feihui Li (Pennsylvania State Univ., United States)

8B-4 Compiler-Guided Data Compression for Reducing Memory Consumption of Embedded Applications
Ozcan Ozturk, Guangyu Chen, Mahmut Kandemir (Pennsylvania State Univ., United States), Ibrahim Kolcu (Univ. of Manchester, Great Britain)

8B-5 Analysis of Scratch-Pad and Data-Cache Performance Using Statistical Methods
Javed Absar (IMEC, Katholieke Universiteit Leuven, Belgium), Francky Catthoor (IMEC, Belgium)

Friday, January 27, 13:30 - 15:35 Room 414+415
Session 8C: Inductive Issues in Power Grids and Packages

Chair(s): ***Takashi Sato*** – Renesas, Japan
Yehea Ismail – Northwestern Univ., United States

8C-1 Efficient Early Stage Resonance Estimation Techniques for C4 Package
Jin Shi, Yici Cai (Tsinghua Univ., China), Shelton X-D Tan (Univ. of California, Riverside, United States), Xianlong Hong (Tsinghua Univ., China)

8C-2 Parallel-Distributed Time-Domain Circuit Simulation of Power Distribution Networks with Frequency-Dependent Parameters
Takayuki Watanabe (Univ. of Shizuoka, Japan), Yuichi Tanji (Kagawa Univ., Japan), Hidemasa Kubota, Hideki Asai (Shizuoka Univ., Japan)

8C-3 Power Distribution Techniques for Dual VDD Circuits
Sarvesh Hemchandra Kulkarni, Dennis Sylvester (Univ. of Michigan, United States)

8C-4 Calculating Frequency-Dependent Inductance of VLSI Interconnect by Complete Multiple Reciprocity Boundary Element Method
Changhao Yan, Wenjian Yu, Zeyi Wang (Tsinghua Univ., China)

8C-5 Controlling Inductive Cross-talk and Power in Off-chip Buses using CODECs
Brock LaMeres (Agilent Technologies Inc., United States), Kanupriya Gulati, Sunil Khatri (Texas A&M Univ., United States)

Friday, January 27, 13:30 - 15:30 Small Auditorium, 5F
Session 8D: Designers' Forum: "Cell" Processor

Chair(s): ***Haruyuki Tago*** – Toshiba, Japan
Makoto Ikeda – Univ. of Tokyo, Japan

8D-1 A New Test and Characterization Scheme for 10+ GHz Low Jitter Wide Band PLL
Kazuhiko Miki (Toshiba, Japan), David Boerstler, Eskinder Hailu, Jieming Qi, Sarah Pettengill (IBM Microelectronics, United States), Yuichi Goto (Toshiba, Japan)

8D-2 An SPU Reference Model for Simulation, Random Test Generation and Verification
Yukio Watanabe (Toshiba, Japan), Balazs Sallay, Brad Michael, Daniel Brokenshire, Gavin Meil, Hazim Shafi (IBM, United States), Daisuke Hiraoka (Sony Computer Entertainment Inc., Japan)

8D-3 A Cycle Accurate Power Estimation Tool
Rajat Chaudhry, Daniel Stasiak, Stephen Posluszny, Sang Dhong (IBM, United States)

8D-4 Key Features of the Design Methodology Enabling a Multi-Core SoC Implementation of a First-Generation CELL Processor
Dac Pham, Hans-Werner Anderson, Erwin Behnen, Mark Bolliger, Sanjay Gupta, Peter Hofstee, Paul Harvey, Charles Johns, Jim Kahle (IBM, United States), Atsushi Kameyama (Toshiba America Electronic Components, United States), John Keaty, Bob Le, Sang Lee, Tuyen Nguyen, John Petrovick, Mydung Pham, Juergen Pille, Stephen Posluszny, Mack Riley, Joseph Verock, James Warnock, Steve Weitzel, Dieter Wendel (IBM, United States)

Friday, January 27, 16:00 - 18:05

Friday, January 27, 16:00 - 18:05 Room 411+412
Session 9A: High-Level Synthesis

Chair(s): ***Shigeru Yamashita*** – NAIST, Japan
Youngsoo Shin – KAIST, Republic of Korea

9A-1 TAPHS: Thermal-Aware Unified Physical-Level and High-Level Synthesis
Zhenyu (Peter) Gu (Northwestern Univ., United States), Yonghong Yang (Queen's Univ., Canada), Jia Wang, Robert P. Dick (Northwestern Univ., United States), Li Shang (Queen's Univ., Canada)

9A-2 An Automated, Efficient and Static Bit-width Optimization Methodology Towards Maximum Bit-width-to-Error Tradeoff With Affine Arithmetic Model
Yu Pu, Yajun Ha (National Univ. of Singapore, Singapore)

9A-3 Abridged Addressing: A Low Power Memory Addressing Strategy
Preeti Ranjan Panda (Indian Inst. of Tech., Delhi, India)

9A-4 Using Speculative Computation and Parallelizing Techniques to Improve Scheduling of Control based Designs
Roberto Cordone (Univ. degli studi di Crema, Italy), Fabrizio Ferrandi, Gianluca Palermo, Marco Domenico Santambrogio, Donatella Sciuto (Politecnico di Milano, Italy)

9A-5 Worst Case Execution Time Analysis for Synthesized Hardware
Jun-hee Yoo, Xingguang Feng, Kiyoung Choi (Seoul National Univ., Republic of Korea), Eui-Young Chung, Kyu-Myung Choi (Samsung Electronics, Republic of Korea)

Friday, January 27, 16:00 - 18:05 Room 413
Session 9B: Modeling, Compilation and Optimization of Embedded Architectures

Chair(s): ***Hiroyuki Tomiyama*** – Nagoya Univ., Japan
Lovic Gauthier – FLEETS, Japan

9B-1 Workload Prediction and Dynamic Voltage Scaling for MPEG Decoding
Ying Tan, Parth Malani, Qinru Qiu, Qing Wu (State Univ. of New York, Binghamton, United States)

9B-2 Lazy BTB: Reduce BTB Energy Consumption Using Dynamic Profiling
Yen-Jen Chang (National Chung-Hsing Univ., Taiwan)

9B-3 Cache Size Selection for Performance, Energy and Reliability of Time-Constrained Systems
Yuan Cai (Univ. of Iowa, United States), Marcus T. Schmitz, Alireza Ejlali, Bashir M. Al-Hashimi (Univ. of Southampton, Great Britain), Sudhakar M. Reddy (Univ. of Iowa, United States)

9B-4 Reducing Dynamic Compilation Overhead by Overlapping Compilation and Execution
Priya Unnikrishnan (IBM Toronto, Canada), Mahmut Kandemir, Feihui Li (Pennsylvania State Univ., United States)

9B-5 Functional Modeling Techniques for Efficient Sw Code Generation of Video Codec Application
Sang-Il Han (TIMA Laboratory, France), Soo-Ik Chae (Seoul National Univ., Republic of Korea), Ahmed Amine Jerraya (TIMA Laboratory, France)

Friday, January 27, 16:00 - 18:05 Room 414+415
Session 9C: Statistical Design

Chair(s): ***Sachin Sapatnekar*** – Univ. of Minnesota, United States
Sunil Khatri – Texas A&M Univ., United States

9C-1 Convergence-Provable Statistical Timing Analysis with Level-Sensitive Latches and Feedback Loops
Lizheng Zhang, Jengliang Tsai, Weijen Chen, Yuhen Hu, Charlie Chungping Chen (Univ. of Wisconsin-Madison, United States)

9C-2 Parameterized Block-Based Non-Gaussian Statistical Gate Timing Analysis
Soroush Abbaspour, Hanif Fatemi, Massoud Pedram (Univ. of Southern California, United States)

9C-3 Statistical Leakage Minimization through Joint Selection of Gate Sizes, Gate Lengths and Threshold Voltage
Sarvesh Bhardwaj, Yu Cao, Sarma Vrudhula (Arizona State Univ., United States)

9C-4 Statistical Bellman-Ford Algorithm With An Application to Retiming
Mongkol Ekpanyapong (Georgia Inst. of Tech., United States), Thaisiri Watewai (Univ. of California, Berkeley, United States), Sung Kyu Lim (Georgia Inst. of Tech., United States)

9C-5 An Exact Algorithm for the Statistical Shortest Path Problem
Liang Deng, Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, United States)

Friday, January 27, 16:30 - 18:00 Small Auditorium, 5F
Session 9D: Designers' Forum Panel: Top 10 Design Issues by LSI Designers versus EDA Developers

Organizer: ***Haruyuki Tago*** – TOSHIBA, Japan
Moderator: ***Yoshiaki Hagihara*** – Sony, Japan
Panelists: ***Raul Camposano*** – Synopsys, United States
Soo-Kwan Eo – SAMSUNG, Republic of Korea
Joe Sawichi – Mentor, United States
Hirofumi Taguchi – Matsushita, Japan
Yasuhiro Tani – CANON, Japan
Ted Vucurevich – Cadence, United States

Tutorials

Tutorial 1 (FULL DAY)
Tuesday, January 24, 9:30-17:00 Room 411+412
DFM Tools and Methodologies for 65nm and Below

Organizer: ***Andrew B. Kahng*** – UCSD and Blaze DFM, Inc., United States

Speakers: ***Andrew B. Kahng*** – UCSD and Blaze DFM, Inc., United States
Louis K. Scheffer – Cadence Design Systems, Inc., United States
Michael Orshansky – Univ. of Texas at Austin, United States
Andrzej Strojwas – PDF Solutions, Inc. and CMU, United States

This tutorial will present a view of key tool technologies and methodologies that are likely to become mainstream for the 65nm node and beyond. Topics include: (1) taxonomy of yield detractors and variability sources; (2) statistical extraction and performance analysis, (3) parametric yield optimizations for timing, power and reliability; (4) manufacturing simulations and analyses for shape (litho and etch), thickness (planarization), and defectivity (critical area); (5) manufacturing-aware capabilities in placement, routing, and post-route optimization tools; and (6) layout synthesis methodologies that range from restricted design rules to flexible layout and liquid libraries.

Tutorial 2 (FULL DAY)
Tuesday, January 24, 9:30-17:00 Room 413
High Performance Interconnect and Packaging

Organizers: ***Chung-Kuan Cheng*** – Univ. of California, San Diego, United States
Howard Chen – IBM, United States

Speakers: ***Paul M. Harvey*** – IBM, United States
Howard Chen – IBM, United States
Chung-Kuan Cheng – Univ. of California, San Diego, United States
Manjit Borah – Fastrack, United States
Lei He – Univ. of California, Los Angeles, United States
Sheldon Tan – Univ. of California, Riverside, United States

With the advance of the VLSI technology, interconnect and packaging are becoming dominant factors in deciding system performance and power consumption. The scalability of interconnect and packaging is recognized as a principal challenge in ITRS Roadmap. This tutorial will provide an overview of new and emerging packaging and interconnect technologies and how they will impact silicon performance. A detailed discussion of the critical factors in the packaging and interconnect design that influence chip performance will be included. The tutorial will provide a comprehensive list of simple, often overlooked design methods to get the most out of many of today's most promising new packaging technologies.

Tutorial 3 (HALF DAY)
Tuesday, January 24, 9:30-12:30 Room 414+415
Low Power / Low Leakage Technologies for Nanometer Era: System and Architecture Level Approaches

Organizer: ***Kimiyoshi Usami*** – Shibaura Institute of Technology, Japan

Speakers: ***Naohiko Irie*** – Hitachi Ltd., Japan
Hiroshi Nakamura – Univ. of Tokyo, Japan

Energy-efficient design is strongly required in SoC's for portable applications. Even for high-end microprocessors, power dissipation becomes a critical hurdle when increasing the performance. This tutorial discusses technical challenges and approaches for low-power / low-leakage design at system and architecture levels. Topics include: dynamic voltage and frequency scaling (DVFS), queue resizing, pipeline balancing and scaling, cache and memory optimizations, globally asynchronous locally synchronous (GALS) architecture, trade-offs between power and reliability, etc.

Tutorial 4 (HALF DAY)
Tuesday, January 24, 14:00-17:00 Room 414+415
Low Power / Low Leakage Technologies for Nanometer Era: Circuit and Device Level Approaches

Organizer: ***Kimiyoshi Usami*** – Shibaura Institute of Technology, Japan

Speakers: ***Kimiyoshi Usami*** – Shibaura Institute of Technology, Japan
Tohru Mogami – NEC Corporation, Japan

Power dissipation is one of the most critical issues in nanometer devices. In addition to dynamic power, leakage power becomes a major concern. This tutorial discusses technical challenges and approaches for low-power / low-leakage design at circuit and device levels. Topics include: circuit and CAD techniques for power gating (MTCMOS), physical implementation and CAD techniques for multi-voltage design, high-k gate dielectric stucks, Cu/low-k interconnects, 3-D device structures, new materials such as SiGe, etc.

Tutorial 5 (HALF DAY)
Tuesday, January 24, 9:30-12:30 Room 416+417
Basics and Practice of Current Functional Verification Methods

Organizer: ***Kiyoharu Hamaguchi*** – Osaka Univ., Japan

Speakers: ***Kiyoharu Hamaguchi*** – Osaka Univ., Japan
Erich Marschner – Cadence Design Systems, Inc., United States

This tutorial 1) summarizes basic concepts and currently available techniques in modern functional verification, 2) presents, in particular, practice of assertion-based verification, and 3) overviews advanced topics in formal verification methods.

Part 1. Basics of Functional Verification (Hamaguchi).
This part overviews currently available techniques in functional verification, which includes functional coverage, assertion, constrained ramdom simulation and bounded/unbounded model checking. Rather than underlying algorithms of the techniques, we mainly dis-

cuss what can be done with the techniques from a point of designers' view.

Part 2. Practice of Assertion-Based Verification (Marschner).
This part presents various techniques for utilizing assertions and functional coverage monitors to achieve higher quality verification in less time. This includes guidelines for writing assertions and coverage monitors, recommendations for where to apply them, and how to leverage them most effectively in typical verification flows.

Part 3. Advanced Topics in Formal Functional Verification (Hamaguchi).
The last part introduces emerging techniques for functional validation or verification, which will be used in functional verification in near-future. This includes abstraction-refinement techniques for large-scale verification, and also formal verification techniques for high-level languages such as SpecC or UML.

Tutorial 6 (HALF DAY)
Tuesday, January 24, 14:00-17:00 Room 416+417
SoC Communication Architectures: Current Practice, Research and Trends

Organizer: ***Nikil Dutt*** – Univ. of California, Irvine, United States

Speakers: ***Nikil Dutt*** – Univ. of California, Irvine, United States
Sudeep Pasricha – Univ. of California, Irvine, United States

The increasing complexity of Systems-on-Chip (SoCs) has led to the critical "design productivity gap" problem. Several strategies are being employed to cope with this problem, including an IP-based design flow, as well as platform-based designs for application domains. These approaches have critically increased the amount of on-chip communication. Since on-chip communication architectures have a significant impact on system performance, power dissipation and time-to-market, system designers, as well as the research community have focused on the issue of exploring, evaluating, and designing SoC communication architectures to meet the targeted design goals. This tutorial will focus on the current design practices, research efforts and emerging trends in the area of on-chip communication architectures. In the first part

of the tutorial, we will first motivate the need for a communication architecture-centric design flow for SoC designs. We will then present a survey of the communication architectures currently used in industry and discuss commonly used protocols and standards such as OCP-IP, VSIA, AMBA, CoreConnect, STBus and Sonics. This will be followed by a case study of a typical industrial design methodology that incorporates communication architecture design in their flow. In the second part of the tutorial, we will present a survey of research efforts in the area of communication architecture exploration, synthesis and implementation, with the goal of improving system performance, reducing power dissipation, cost and design cycle time. The focus of this part will be on variants of bus based and bus-matrix based communication architectures. In the final part of the tutorial, we will outline emerging trends in the area of on-chip communication architectures design and review research efforts on the topics of network-on-chips and on-chip optical interconnects.

ASP-DAC 2006 at a Glance

Tuesday, January 24

FULL-DAY Tutorials

TUTORIAL 1	(9:30-17:00)	Room 411+412
DFM Tools and Methodologies for 65nm and Below		
TUTORIAL 2	(9:30-17:00)	Room 413
High Performance Interconnect and Packaging		

HALF-DAY Tutorials

TUTORIAL 3	(9:30-12:30)	Room 414+415
Low Power / Low Leakage Technologies for Nanometer Era: System and Architecture Level Approaches		
TUTORIAL 4	(14:00-17:00)	Room 414+415
Low Power / Low Leakage Technologies for Nanometer Era: Circuit and Device Level Approaches		
TUTORIAL 5	(9:30-12:30)	Room 416+417
Basics and Practice of Current Functional Verification Methods		
TUTORIAL 6	(14:00-17:00)	Room 416+417
SoC Communication Architectures: Current Practice, Research and Trends		

Wednesday, January 25

	A	B	C	D
8:30	**Opening Session** (Small Auditorium, 5F)			
9:00	**Keynote Address I** (Small Auditorium, 5F)			
10:00	**Break**			
10:15	1A (Room 411+412) Formal Methods for Coverage and Scalable Verification	1B (Room 413) Interconnect for High-End SoC	1C (Room 414+415) Timing Analysis and Optimization	1D (Room 416+417) University Design Contest
12:20	**Lunch Break / University Design Contest Discussion at ASP-DAC Site (Room 418)**			
13:30	2A (Room 411+412) Software Techniques for Efficient SoC Design	2B (Room 413) Application Examples with Leading Edge Design Methodology	2C (Room 414+415) Placement	2D (Room 416+417) Special Session: Electrothermal Design of Nanoscale Integrated Circuits
15:35	**Coffee Break (Room 418)**			
16:00	3A (Room 411+412) Logic Synthesis	3B (Room 413) Future Technical Directions for Design Automation	3C (Room 414+415) Routing and Interconnect Optimization	3D (Room 416+417) Special Session: Flash Memory in Embedded Systems
18:05				

Thursday, January 26

	A	B	C	D
9:00	**Keynote Address II** (Small Auditorium, 5F)			
10:00	**Break**			
10:15	4A (Room 411+412) Resolving Timing Issues: Design and Test	4B (Room 413) Leading Edge Design Methodology for SoCs and SiPs	4C (Room 414+415) Advanced Circuit Simulation	4D (Room 416+417) Special Session: Open Access Overview
12:20	**Lunch Break / Ph.D. Forum (Room 418)**			
13:30	5A (Room 411+412) Advances in Simulation Technologies	5B (Room 413) Scheduling for Embedded Systems	5C (Room 414+415) High Frequency Interconnect Effects in Nanometer Technology	5D (Small Auditorium, 5F) 13:30-15:30 Designers' Forum: Low Power Design
15:35	**Coffee Break (Room 418)**			
16:00	6A (Room 411+412) Power Optimization of Large-Scale Circuits	6B (Room 413) Advanced Memory and Processor Architectures for MPSoC	6C (Room 414+415) New Routing Techniques	6D (Small Auditorium, 5F) 16:30-18:00 Designers' Forum Panel: Functional Verification —now and future—
18:05	Banquet 18:30–20:30 (Room 501+502)			

Friday, January 27

	A	B	C	D
9:00	**Keynote Address III** (Small Auditorium, 5F)			
10:00	**Break**			
10:15	7A (Room 411+412) Minimization of Test Cost and Power	7B (Room 413) Substrate Coupling and Analog Syntesis	7C (Room 414+415) Statistical and Yield Analysis	7D (Room 416+417) Special Session: H.264/AVC Design Challenges and Solutions
12:20	**Lunch Break**			
13:30	8A (Room 411+412) Floorplanning	8B (Room 413) Memory Optimization for Embedded Systems	8C (Room 414+415) Inductive Issues in Power Grids and Packages	8D (Small Auditorium, 5F) 13:30-15:30 Designers' Forum: "Cell" Processor
15:35	**Coffee Break (Room 418)**			
16:00	9A (Room 411+412) High-Level Synthesis	9B (Room 413) Modeling, Compilation and Optimization of Embedded Architectures	9C (Room 414+415) Statistical Design	9D (Small Auditorium, 5F) 16:30-18:00 Designers' Forum Panel: Top 10 Design Issues by LSI Designers versus EDA Developers
18:05				

Information

Proceedings:

ASP-DAC 2006 will be producing two versions of the ASP-DAC 2006 Proceedings; a bound paper version and a CD-ROM version. All papers will be included in both versions. Conference registration in any of the categories will include copies of both versions of the ASP-DAC 2006 Proceedings. Additional Proceedings will be available for purchase at the Conference. Prices are as follows:

Paper Form: ¥5,000; CD-ROM Form: ¥2,000;

Both versions of the proceedings will also be available for purchase after the conference; please contact IEEE for the bound version and ACM SIGDA for the CD-ROM version.

Banquet:

Conference registrants are invited to attend a banquet to be held on January 26, 2006. The banquet will be held from 18:30 to 20:30 at the fifth floor of conference center. Regular Member and Non-member Conference registrants receive a ticket to the banquet when they register at the conference. Full-time students, Designers' Forum-only registrants, and Tutorial-only registrants wishing to attend the banquet will be required to pay ¥5,000 for a ticket when they register on site.

Visa Application:

Without a legal visa, foreign participants may be denied entry into Japan. Please contact your nearest Japanese embassy in order to ensure entry. Notice that the ASP-DAC 2006 Organizing Committee issues the invitation letters and supports the VISA applications only for presenters of the conference papers. All the other attendees have to apply for VISA through their travel agents or by yourself. In some cases it may take two months to obtain a legal visa. The following Web page of Japanese embassy may be helpful.

http://www.mofa.go.jp/j_info/visit/visa/index.html

Customs:

Japanese customs are fairly lenient and allow bringing in items necessary for personal use. Duty-free imports are: 3 bottles of liquor; 400 cigarettes or 100 cigars; 2 ounces of perfume; gifts and souvenirs other than the above whose total market value does not exceed 200,000 yen. Strictly prohibited are firearms, other types of weapons and narcotics.

Insurance:

The organizer cannot accept responsibility for accidents which might occur. Delegates are encouraged to obtain travel insurance (medical, personal accident, and luggage) in their home country prior to departure.

Climate:

The temperature in Yokohama during the period of the Conference ranges between 5°C and 12°C.

Currency Exchange:

Only Japanese Yen(¥) is accepted at ordinary stores and restaurants. Certain foreign currencies may be accepted at a limited number of hotels, restaurants and souvenir shops. You can exchange your currency for Japanese Yen at foreign exchange banks and other authorized money exchange offices with your passport.

Electrical Appliances:

Electrical appliances are supplied on 100 volts in Japan. The frequency is 50 Hz in eastern Japan including Tokyo, Yokohama and 60 Hz in western Japan including Kyoto and Osaka.

Shopping:

The business hours of most department stores are from 10:00 to 20:00. They are open on Sundays and national holidays, but may close on some weekday. Business hours of retail shops differ from one another, but most shops operate from 10:00 to 20:00. Shops are open on Sundays and national holidays.

Sightseeing:

http://www.city.yokohama.jp/ne/info/hotspotE.html

Participants can get sightseeing information at the Nippon Express Co., Ltd. Travel desk in the Conference site during the Conference period.

Yokohama Bay Sightseeing Cruise

You can ride a cruise boat at Yamashita Park sightseeing Boat Terminal, Minato Mirai Pukarisanbashi Pier (MM21), etc. For more information, reference the home page at:
http://www.welcome.city.yokohama.jp/eng/tourism/walking/1070.html

CHINA TOWN

Being the largest Chinese settlement in Japan, Chinatown is always alive with people who come to enjoy Chinese food. It is also a fun place for shopping or just walking around its many streets and alleys lined with colorful restaurants, shops overflowing with Chinese goods and stores that sell exotic ingredients and Chinese medicines.

LANDMARK TOWER

296 meters high with 70 stories above ground and three levels underground. It is Japan's tallest skyscraper. A 40-second ride on the world's fastest elevator skyrockets you to the 69th floor's Sky Garden, the highest observatory in Japan.
Hours: 10:00-21:00 Admission: ¥1,000
Access: 7min. walk from Sakuragicho station

SANKEIEN GARDEN

A purely Japanese-style landscape garden. Accenting the main garden is an impressive three-story pagoda and graceful garden bridges. Inside contains several old houses and farm buildings as well as Important Cultural Properties such as Rinshunkaku Villa and Chosukaku House.
Hours:9:00-16:00 Admission:¥300 for each garden
Access: From Sakuragicho Sta., take Bus NO.8 or No.125 to Honmoku-Sankeien-mae.

MARINE TOWER

106 meters, the tallest inland lighthouse in the world, with an observatory located 100 meters above ground.
Hours: 10:00-21:00 Admission: ¥700
Access: 15min. Walk from JR Ishikawacho station

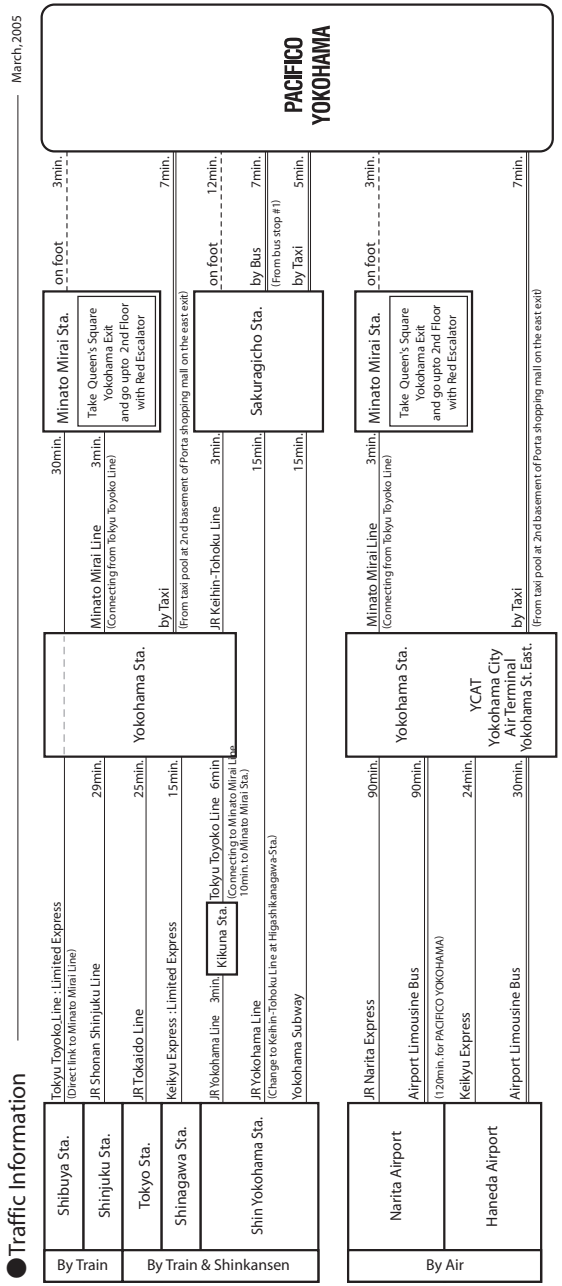
MARITIME MUSEUM

The site of the previous Nippon Maru, the former training ship for Japan's Maritime Defense Force. The Yokohama Maritime Museum, which specializes in ports and ships, is located next to the Nippon Maru.
Hours: 10:00-17:00 (Closed Monday) Admission: ¥600
Access: 7 min. walk from JR Sakuragicho station

Other Information:

JAPANTOURIST ORGANIZATION
http://www.jnto.go.jp/
YOKOHAMA CONVENTION & VISITORS BUREAU
http://www.welcome.city.yokohama.jp/tourism/
NARITA AIRPORT
http://www.narita-airport.or.jp/airport_e/index.html
YES ! TOKYO
http://www.tcvb.or.jp/en/index_en.htm

Access to Pacifico Yokohama



■Driving To Pacifico

[From Tokyo]

Metropolitan Expressway

- Toward Yokohama Park, Yokohane Route
- Toward Yokohama (over Bay bridge), Wangan Route

[From Kansai or Chubu]

Tomei Expressway Yokohama Machida IC

- Hodogaya Bypass,20min.
- Kariba IC

PACIFICO YOKOHAMA

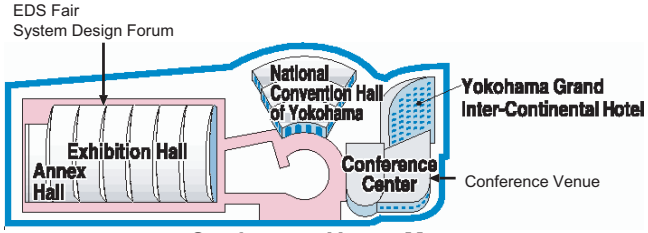
- Minato Mirai Ramp,3min.
- Minato Mirai Ramp,3min.
- Toward Yokohama,Metropolitan Expressway,Kariba Route,10min.
- Minato Mirai Ramp,3min

■Parking Lot

Minato Mirai Public Parking Lot +81-45-221-1301	Capacity:1,200 (Standard-sized cars only)	Open 24 hours	Rates:Standard-sized car 260yen/30min. (1,300yen for max. 15hours between 8 and 23 on weekdays.)
Bus/Large Vehicles Parking Lot +81-45-221-1302	Capacity:40	Open 24 hours	Rates:Large vehicle 500yen/30min.

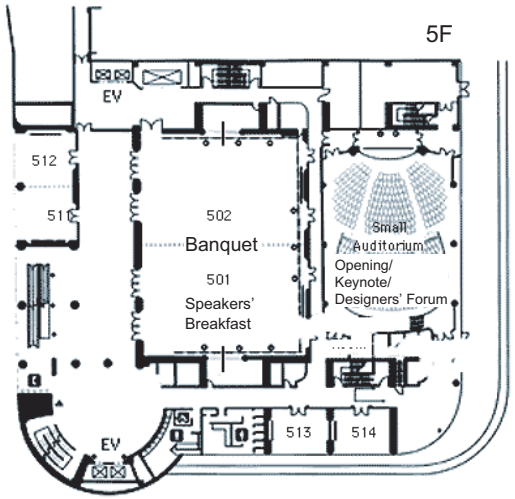
Venue Map/Room Assignment

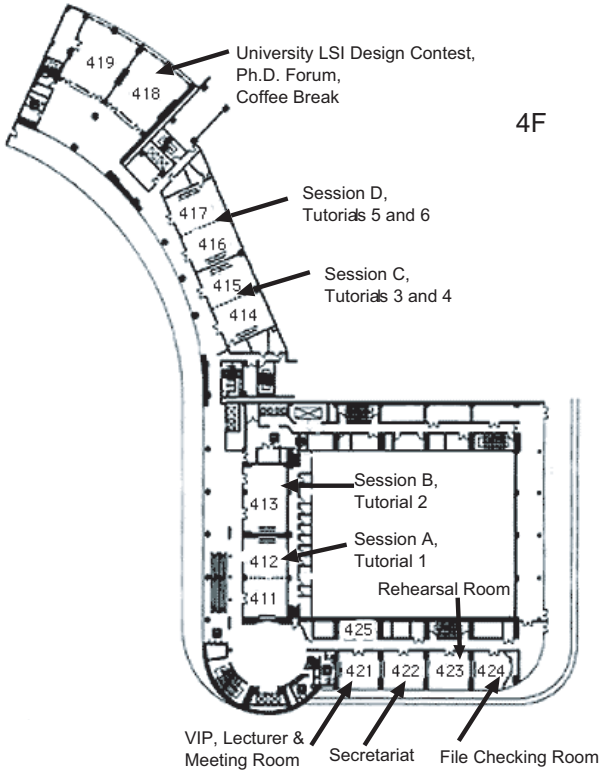
- ASP-DAC Conference is held at “Conference Center.”
- EDS Fair 2006 and System Design Forum 2006 are held at “Exhibition Hall/Annex Hall.” (2min. walk from Conference Center.)

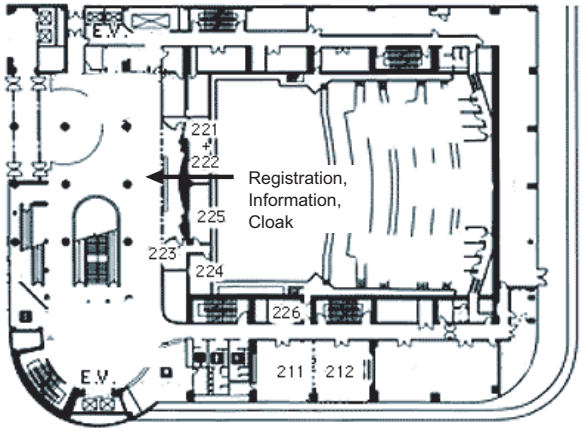


Conference Venue Map

Location	Event
Entrance Hall (2F)	Registration, Information, Cloak
Small Auditorium (5F)	Opening, Keynote, Deginers' Forum
411+412 (4F)	Session A, Tutorial 1
413 (4F)	Session B, Tutorial 2
414+415 (4F)	Session C, Tutorials 3 and 4
416+417 (4F)	Session D, Tutorials 5 and 6
418 (4F)	Poster Discussion, Ph.D. Forum, Coffee Break
421 (4F)	VIP, Lecturer & Meeting Room
422 (4F)	Secretariat
423 (4F)	Rehearsal Room
424 (4F)	File Checking Room
501+502 (5F)	Banquet
501 (5F)	Speakers' Breakfast
Exhibition Hall/Annex Hall	EDS Fair 2006, System Design Forum 2006







Conference Center Map

Electronic Design and Solution Fair 2006

The Japan Electronics and Information Technology Industries Association (JEITA) will hold the Electronic Design and Solution Fair 2006 on January 26 and 27, 2006, in Pacifico Yokohama. When JEITA was known as the Electronic Industries Association of Japan (EIAJ), we held the EDA TechnoFair for seven consecutive years from 1993 to 2000. This exhibition showcased design solutions, design technologies, and EDA technologies required for the latest electronic systems or semiconductors.

In 2001, the EDA TechnoFair and the FPGA/PLD Design Conference and Exhibit were combined to form the Electronic Design and Solution Fair. The Fair will be held for the sixth time in 2006 as the only exhibition of its kind in Japan.

Today, semiconductors not only play a core supporting role throughout industry and the economy, but they are also an indispensable part of our daily lives. The emergence of computers, the Internet, digital communications, cellular telephones, and digital home appliances would not have been possible without advances in semiconductors. Progress in digital technology, underpinned by innovations in semiconductor technology, is bringing huge changes to society, culture, and lifestyles. In fact, we now stand on the threshold of a ubiquitous age, in which people can communicate anywhere and at any time.

Furthermore, the semiconductor industry will grow even more important as it embraces the challenge of new technological development to supply new products in its quest to remain at the vanguard of the digital networking age.

The theme of Electronic Design and Solution Fair 2006 is ”Touch the 65 Nano-World” The Fair will feature a full range of events and exhibitions, which we will be widely publicizing in coming months. In addition to displays and content that meet demand for new solutions, we will open University Plaza to enhance technological interchange between industry, academia and government organizations. The Fair will also feature a special section for the exhibits of overseas emerging companies. Two conferences will be held simultaneously with the Fair: the FPGA/PLD Design Conference and System Design Forum 2006.

JEITA is confident that Electronic Design and Solution Fair 2006 will promote effective and meaningful discussions and interchange between exhibitors and visitors alike, and that it will provide unique opportunities for business development. All of us involved with the Fair look forward to seeing you there.

Tadashi Okamura
Chairman
Japan Electronics and
Information Technology Industries Association

General Information

Name:
Electronic Design and Solution Fair 2006

Schedule:
Thursday, January 26, and Friday, January 27, 2006
10:00a.m. to 6:00p.m.

Location:
Pacifico Yokohama (Exhibition Hall, Annex Hall)
1-1-1, Minato Mirai, Nishi-ku, Yokohama 220-0012, Japan

Exhibition Category:
- IC design tools
- Methodologies
- Design for manufacturing solutions
- IPs
- Embedded software in SoCs
- Various design services and many other topics that affect today’s design of electronic circuits and systems

Admission:
Exhibition: Free (registration required at show entrance)
Conferences: Fees will be charged for some conferences

Sponsor:
Japan Electronics and Information Technology Industries Association (JEITA)

Cooperation:
Electronic Design Automation Consortium (EDAC)

Support:
Ministry of the Economy, Trade and Industry, Japan (METI)
Embassy of the United States of America in Japan
Distributors Association of Foreign Semiconductors (DAFS)
City of Yokohama

Assistance:
Institute of Electronics, Information and Communication Engineers (IEICE)
Information Processing Society of Japan (IPSJ)
Japan Electronics Packaging and Circuits Association (JPCA)

Management:
Japan Electronics Show Association (JESA)

URL:
http://www.edsfair.com

System Design Forum 2006 at EDS Fair

Friday, January 27, 10:00–12:00, 13:30-15:30
Annex Hall, Pacifico Yokohama

Registration: On line registration will be available from November 2005 at URL: **http://www.edsfair.com**
Sponsor: Japan Electronics and Information Technology Industries Association (JEITA)
Support: Accellera, Open SystemC Initiative (OSCI)

System Design Forum 2006 will be held on January 27, 2006 at the Pacifico Yokohama, Kanagawa, Japan, organized by EDA Technical Committee (EDA-TC) of JEITA. This year at this Forum two sessions are going to be held, focusing on the system level design language, SystemC and SystemVerilog. Up-date information about standardization of each language, tutorials, and design examples of the state-of-the-art SOC designs using SystemC or SystemVerilog will be presented.

Session 1: SystemVerilog Users Forum 2006, 10:00-12:00
Chair: **K. Hamaguchi (JEITA SystemVerilog Task Group)**

SystemVerilog, successor language of VerilogHDL (IEEE Std-1364), is drawn LSI designer attention as next-generation LSI Design/Verification language. And, SystemVerilog was approved as IEEE Std-1800 in November. In this session a member of IEEE P1800, SystemVerilog Standardization Working Group will give an update of standardization and the use status of SystemVerilog. Then, members of JEITA SystemVerilog Task Group will explain the technical trends about SystemVerilog Assertions. This session also includes presentations about design/verification examples using SystemVerilog.

Session 2: SystemC Users Forum 2006, 13:30-15:30
Chair: **T. Hasegawa (JEITA SystemC Task Group)**

SystemC, C-based language, is now widely used in the industry as a de facto standard system level design language. In addition, IEEE P1666 SystemC Standardization Working Group is working on the standardization of SystemC for the final approval by December 2005. In this session, the representative of Open SystemC Initiative (OSCI) will give an update of standardization and the road map of SystemC. And the representative of JEITA SystemC Task Group will explain the technical trends about SystemC, and new features of SystemC 2.1. This session also includes the latest user presentations with the practical design examples using SystemC.

Note: The most of the presentations at the System Design Forum2006 will be presented in Japanese.

Related to System Design Forum 2006, two paper sessions and two panel sessions are organized as **Designers' Forum in ASP-DAC 2006**:

5D: Thursday, January 26, 13:30-15:30, Small Auditorium, 5F
"Designers' Forum: Low Power Design"
6D: Thursday, January 26, 16:30-18:00, Small Auditorium, 5F
"Designers' Forum Panel: Functional Verification—now and future—"
8D: Thursday, January 27, 13:30-15:30, Small Auditorium, 5F
"Designers' Forum: 'Cell' Processor"
9D: Thursday, January 27, 16:30-18:00, Small Auditorium, 5F
"Designers' Forum Panel: Top 10 Design Issues by LSI Designers versus EDA Developers"

For more information, visit the following web site:
http://www.edsfair.com.