


Fast and Accurate OPC for Standard-Cell Layouts

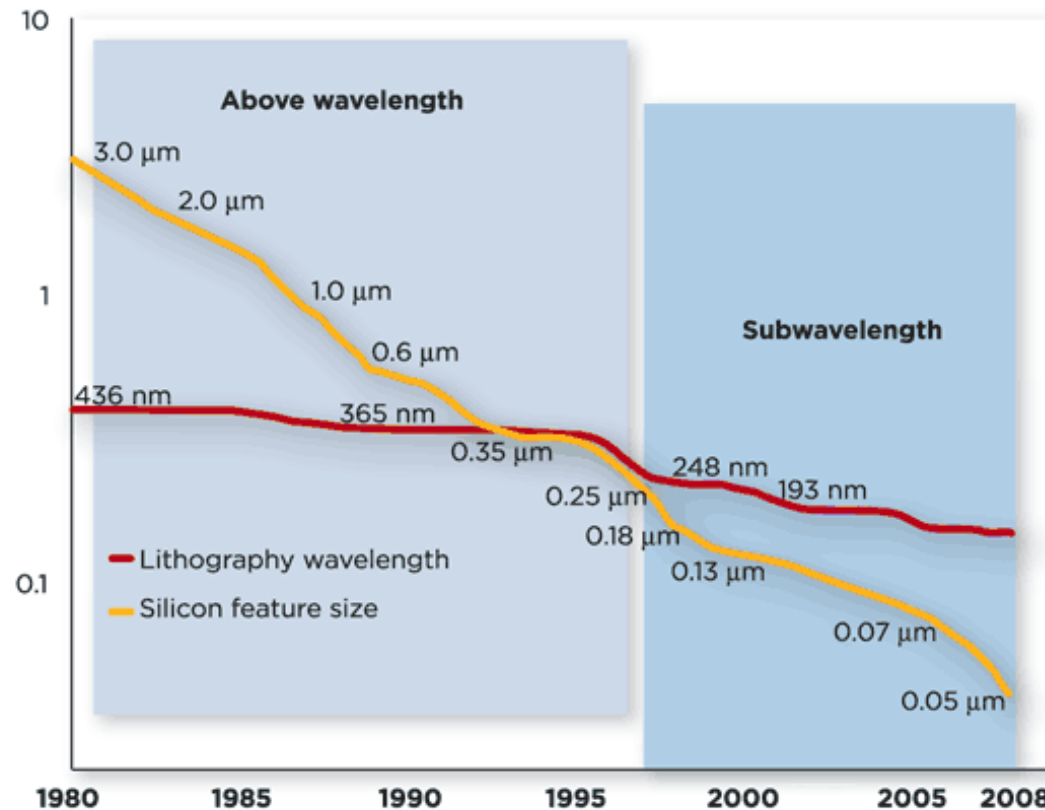


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Lithography and Technology Scaling

As feature sizes shrink, chipmaking woes grow

Optical litho can exist only with CAD-based correction tools



Note: vertical scale is in microns.

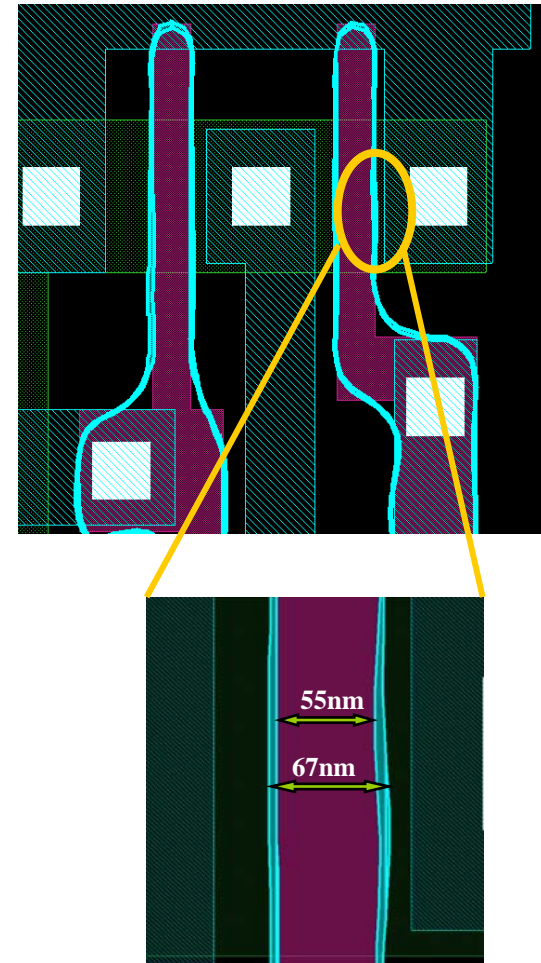
Source: Mentor Graphics Corp.

Lithography and Design

- ❑ Sub-wavelength lithography: 193nm light is used in 65nm and 45nm nodes, and will be used in 32nm technology nodes!
- ❑ Resolution enhancement techniques (RET) (e.g., OPC, PSM, OAI) are the key enabling technology
- ❑ Design tools should “plan” for RETs
- ❑ Requires new methodologies and algorithms

Lithography and Variations

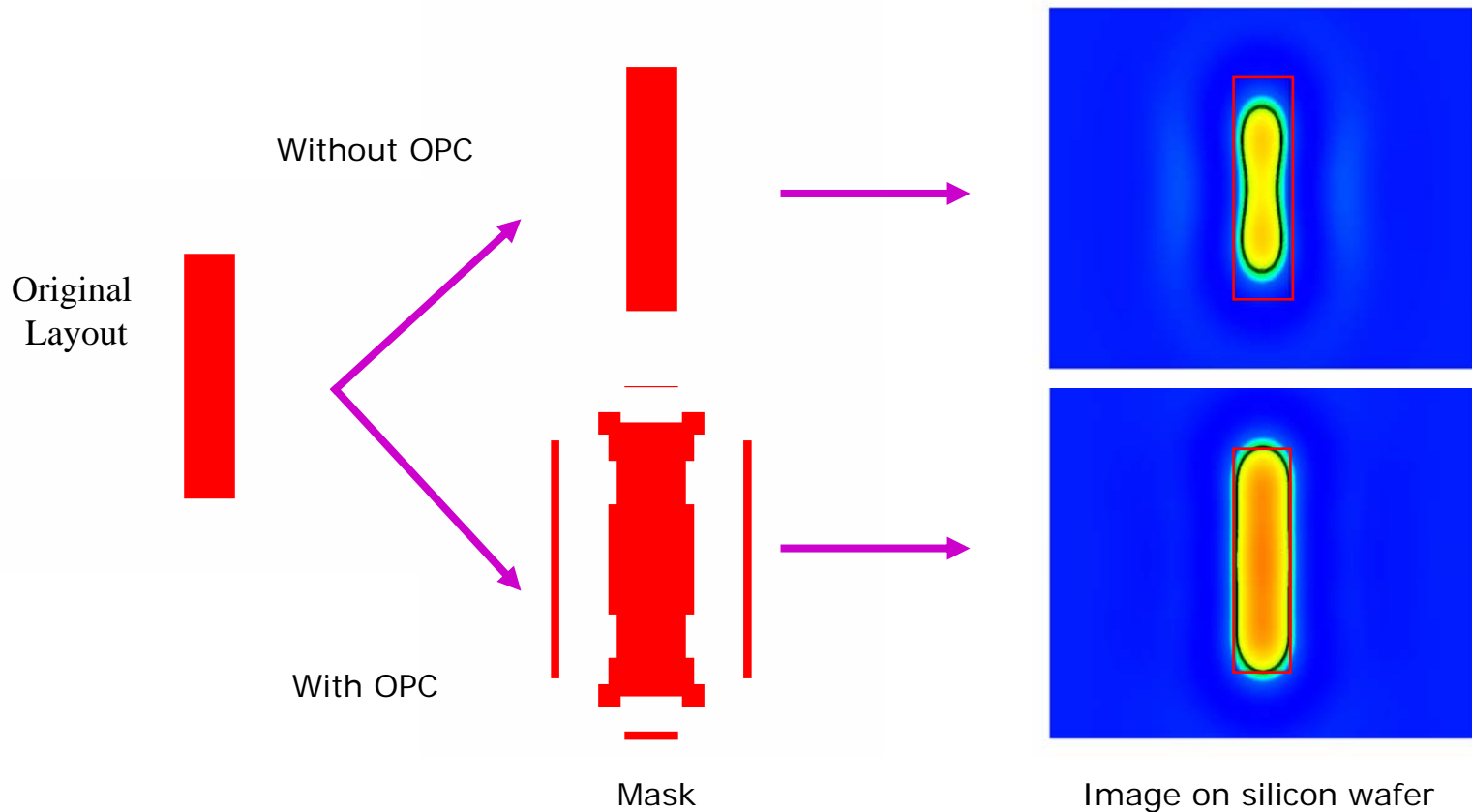
- ❑ Lithography – a main source of process variations
- ❑ Gate length variation will change the delay, threshold voltage, and leakage ...
- ❑ This issue will only become more critical in future technology nodes



Ke Cao and etc. DAC06

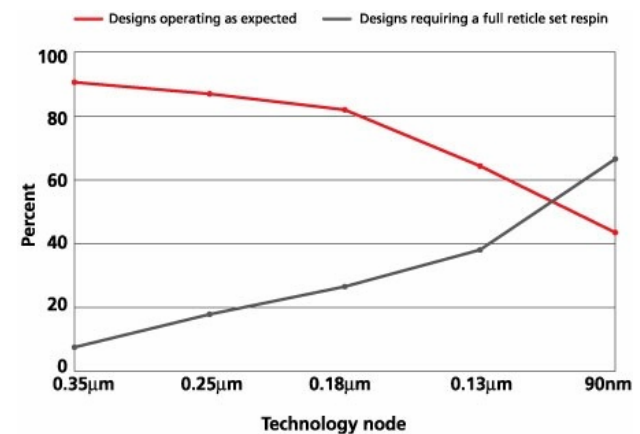
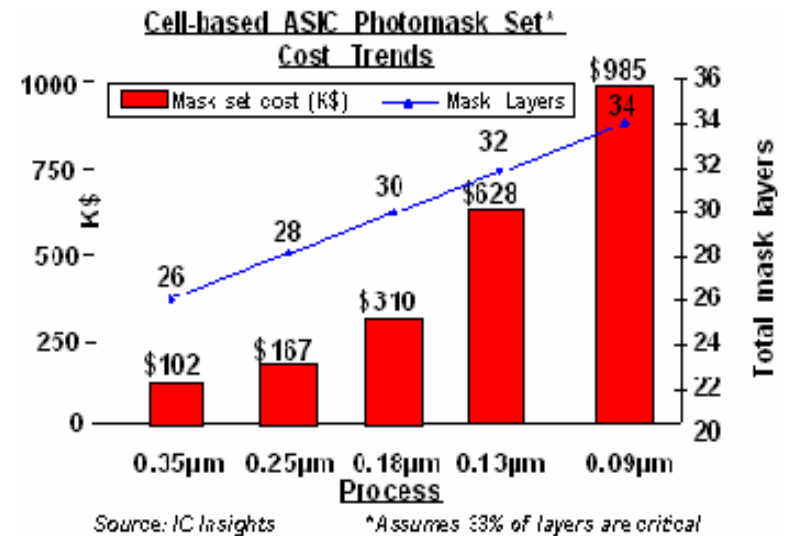
Optical Proximity Correction (OPC)

- Manipulate mask geometry to compensate for image distortions
- Model-based OPC are required for 65nm node and beyond



Manufacturing Cost

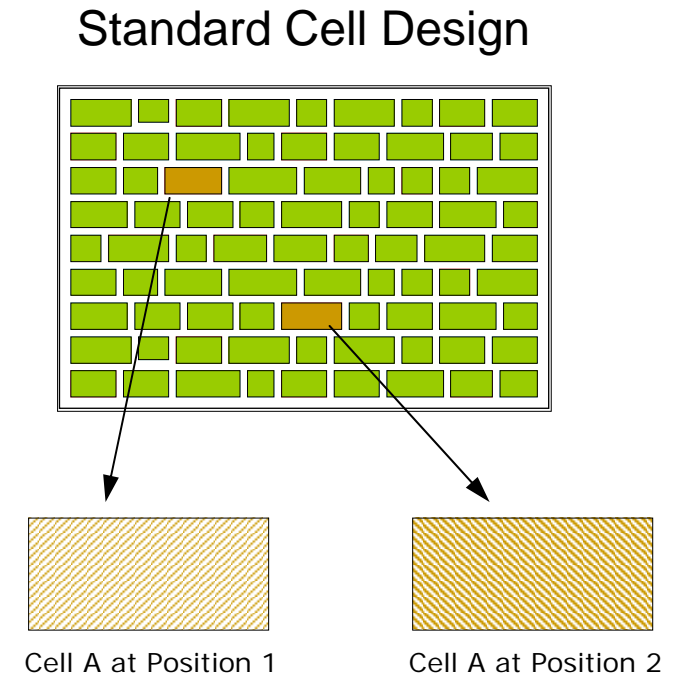
- Skyrocketing Mask Cost
 - Long OPC runtime
 - Exponentially increased features on the mask
- More design/fabrication loop needed
 - Less design can work right after the first tape-out
 - Mask set respin required
 - Manufacturing cost may be doubled or even tripled



Source: EETime

Standard Cell and OPC

- Standard cell based designs accept full-chip OPC
- Even for the same cell after full-chip OPC
 - Different environments
 - Different OPC solutions
 - Different print errors
 - Different characterizations



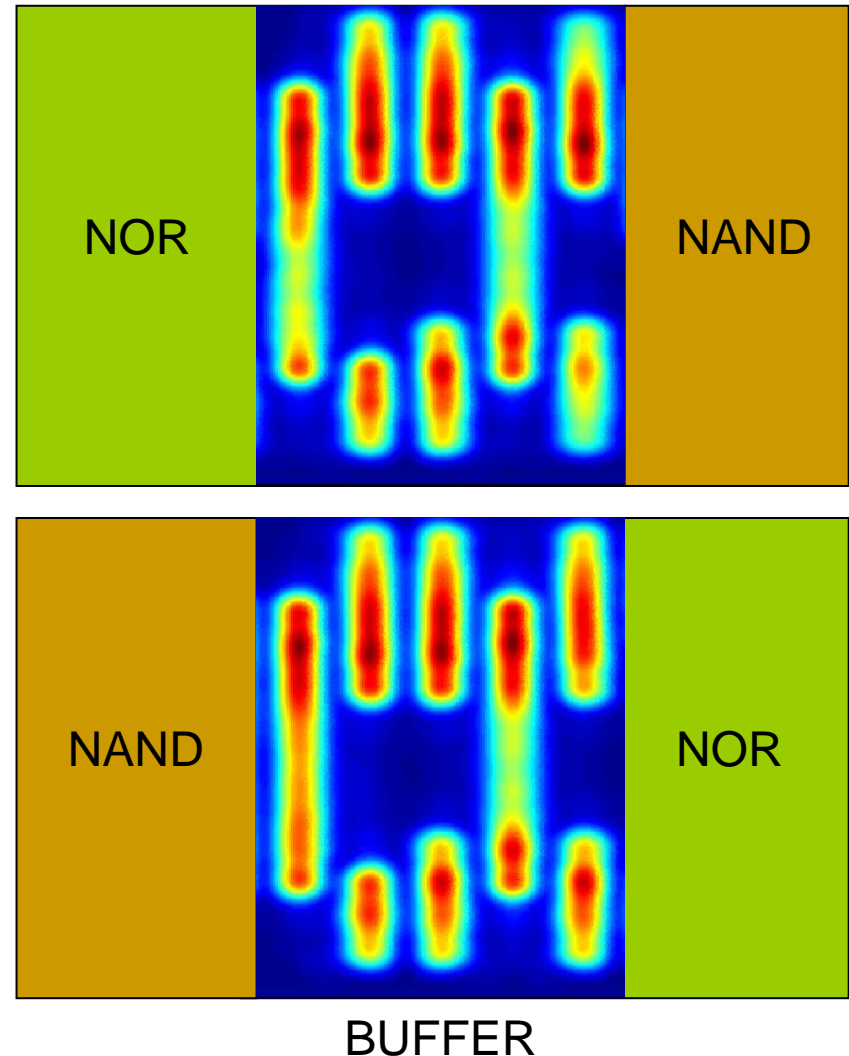
Cellwise OPC Methodology

- Problems with full-chip OPC
 - Large storage requirement (due to numerous complex geometries representing the corrections)
 - Long computation time (e.g., days of OPC computations on computers running in parallel)
 - Simulation models do not account for all possible printing variations → unexpected imaging failures

- *We propose a cellwise OPC methodology to fix all these problems for standard-cell design*

OPC for a Cell Depends on its Neighbors

- ❑ The buffer cell sees very different optical influence from different neighboring cells
- ❑ Center features almost remain the same
- ❑ Boundary features vary a lot due to the different environment
- ❑ A boundary-based cellwise OPC approach is required for future technologies

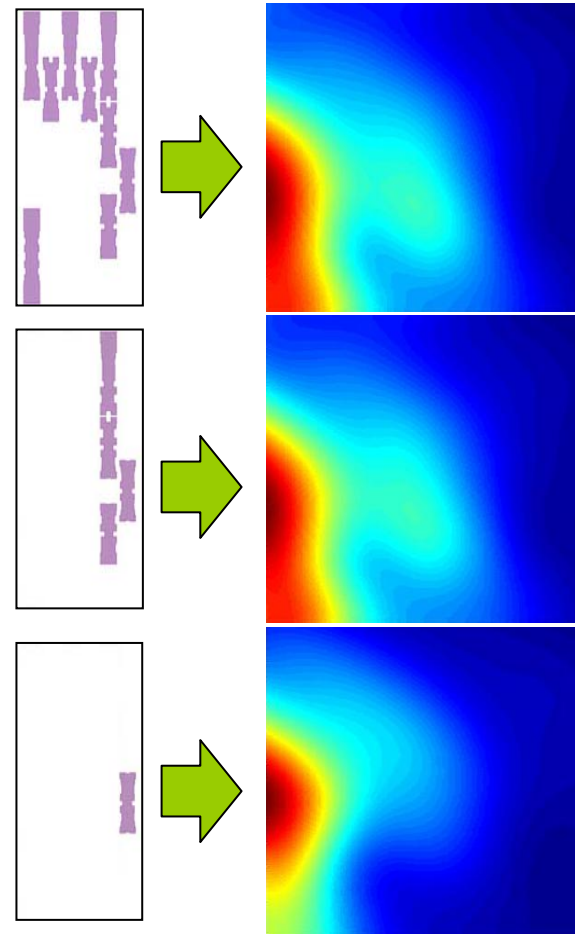


Boundary-Based Cellwise OPC

- ❑ Pre-compute and store the corrected cell layouts
- ❑ Each cell has multiple versions of OPC corrections obtained in the presence of representative environments (modeling optical influence from neighboring cells)
- ❑ In full chip layout, OPC is done cellwise where each cell uses a pre-computed correction based on its neighboring environment
- ❑ **Challenges:** How to design small number of OPC versions and yet have high-degree of accuracy?

Representative Features

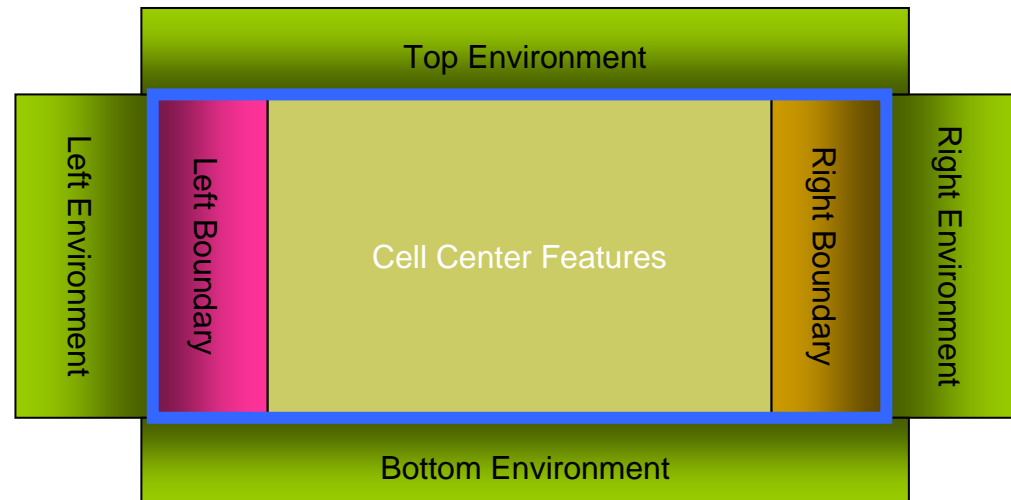
- ❑ Radius of influence (ROI) is typically $< 1000\text{nm}$ in current lithography system
- ❑ Limiting boundary of standard cell helps cellwise OPC
- ❑ The outmost two column can be representative features for the cell



The aerial images outside a NOR logic gate (metal1 features)

Boundary-Based Cellwise OPC

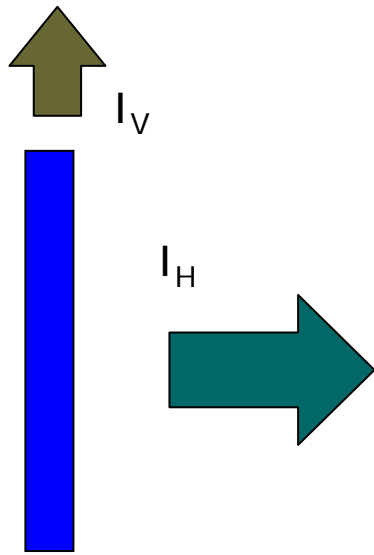
- ❑ Center features accept cellwise OPC without boundaries
- ❑ Left and Right boundaries have OPC solutions according to its neighboring environments
 - Two columns of features for cell boundary
 - Two columns of features for neighboring environment
- ❑ Top and Bottom Environment can be ignored



Top and Bottom Representative Features

- ❑ Top and bottom representative feature can be ignored
- ❑ Relatively smaller optical influence on vertical direction than horizontal direction
- ❑ Power and ground tracks make the features further apart

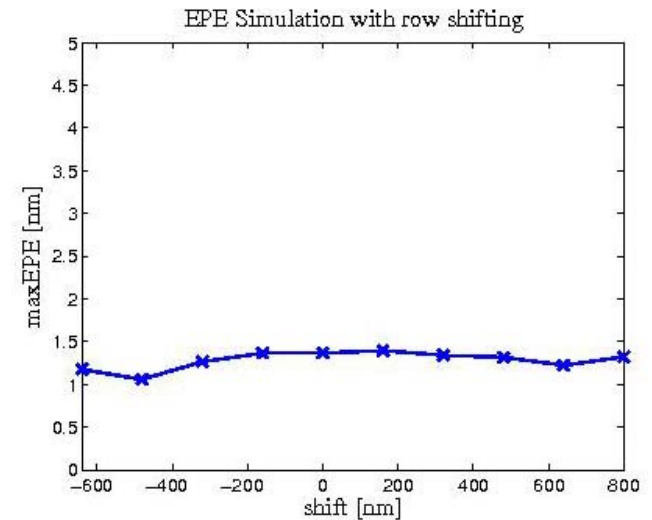
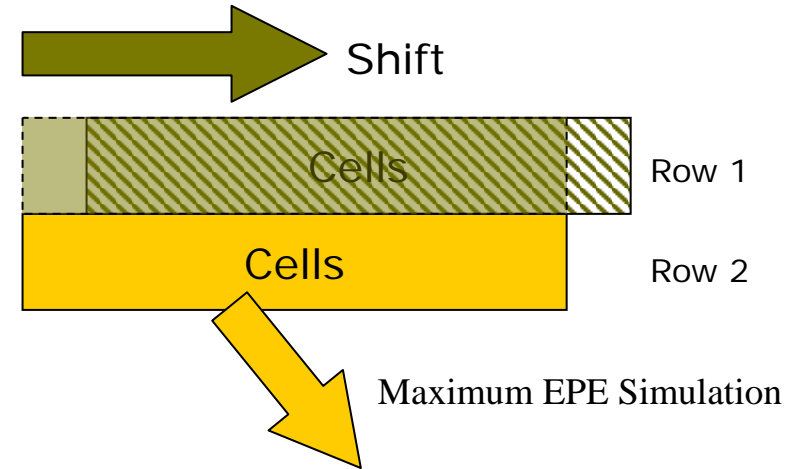
Simulation Results



One Metal feature after OPC

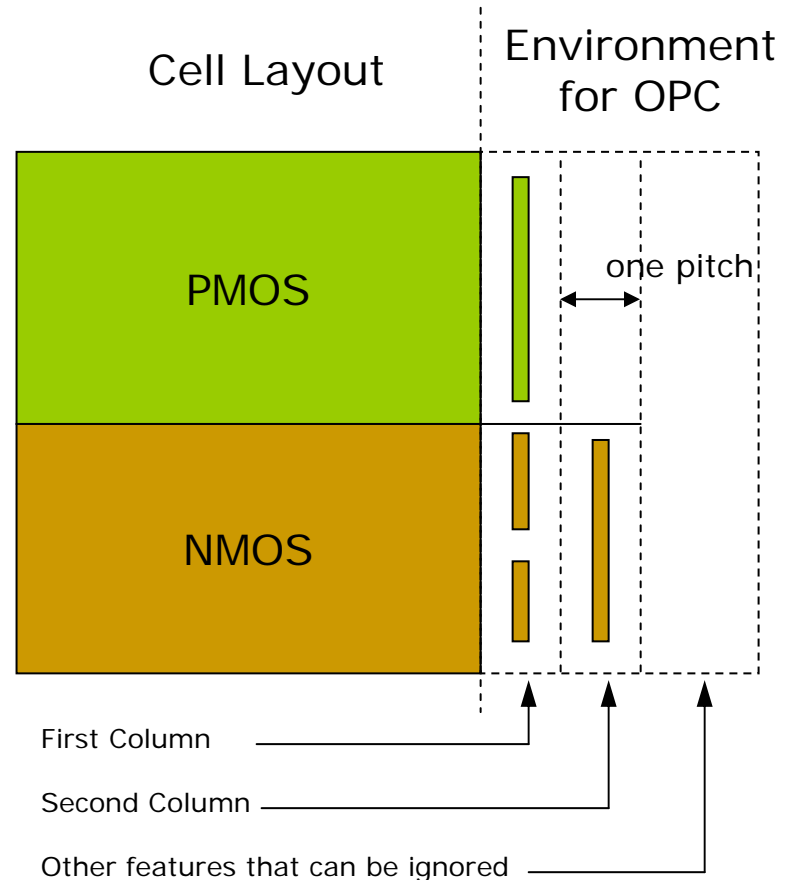
D	10nm	200nm	400nm	600nm
I_V	0.298	7.0e-3	2.8e-4	1.7e-5
I_H	0.300	1.8e-3	1.6e-3	3.4e-4

D is the simulation point from the feature edge



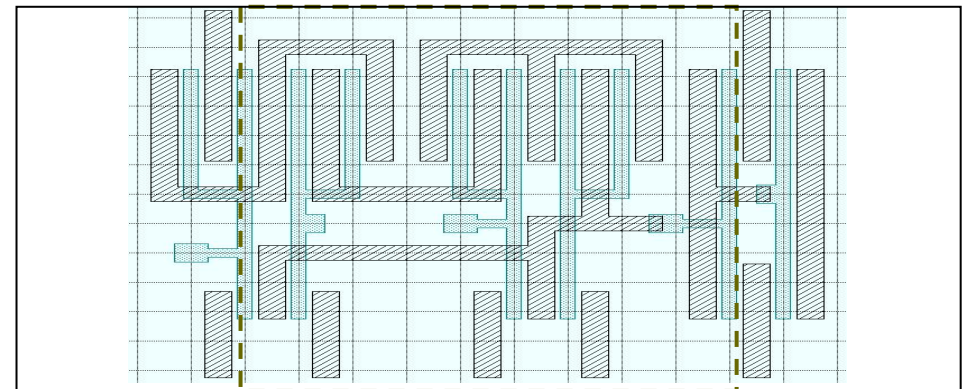
Number of Representative Features

- ❑ Two columns of features as representative environment
- ❑ Environment NMOS and PMOS layout can be separated
- ❑ Features in the most adjacent column are directly from cell boundaries
- ❑ Features in the second column are either full or empty for representative purpose
- ❑ The number of total representative environments are limited due to the nature of standard cell layout

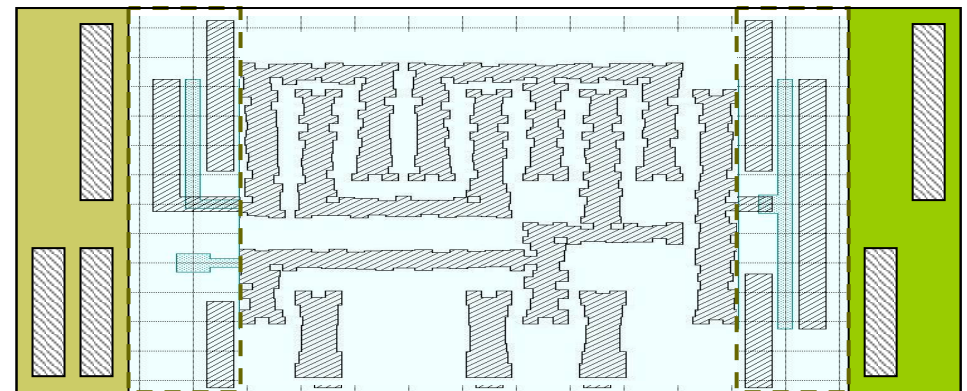


Incremental OPC for Cell Boundary

- OPC is performed on each cell with no boundaries to obtain the center part OPC solution
- Column by column OPC is performed on cell boundaries with representative environments



OPC for center part



Incremental OPC



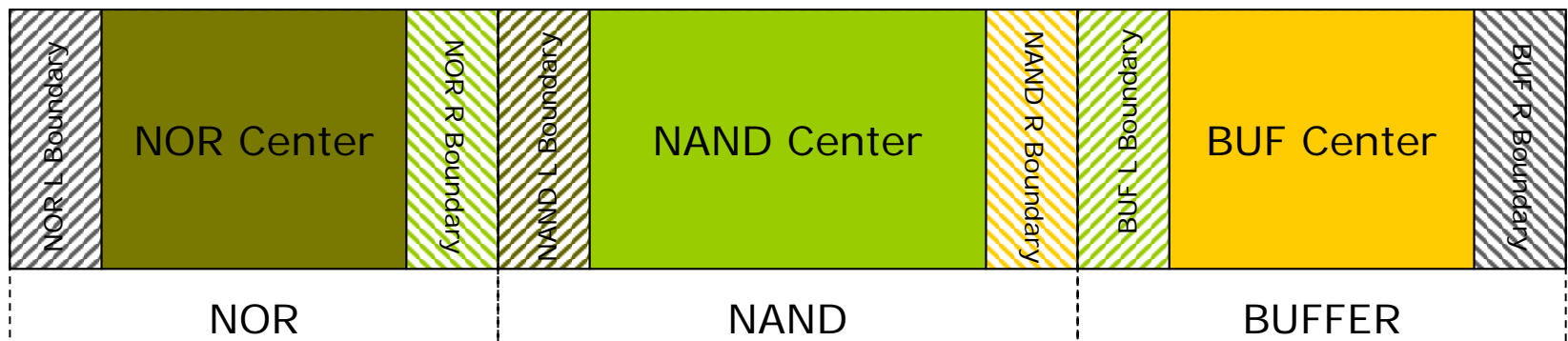
Incremental OPC

Special Cases (Narrow Cells)

- ❑ Some cells have smaller width
 - INV, BUF cells have only 2-3 columns of Metal1 features
- ❑ Only one column as the cell boundary
 - Other approaches are also tested
 - This technique achieved the best accuracy
- ❑ The cellwise OPC procedure remain the same

Full-chip OPC Solution by Table-Look-Up

- ❑ Full-chip OPC can be done right after placement
- ❑ Center Part of OPC solution is decided by the cell
- ❑ OPC for boundaries are decided by the cell and its environments
- ❑ All done by simple table-look-up!

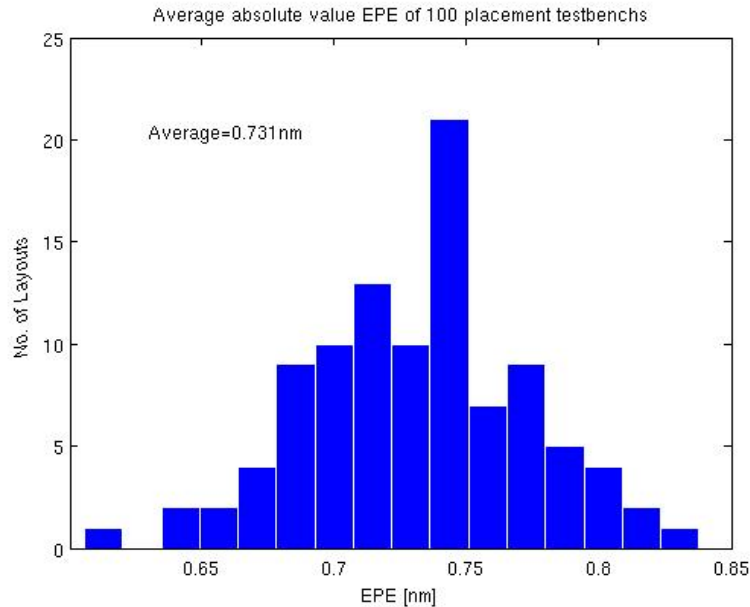


Advantages of Cellwise OPC

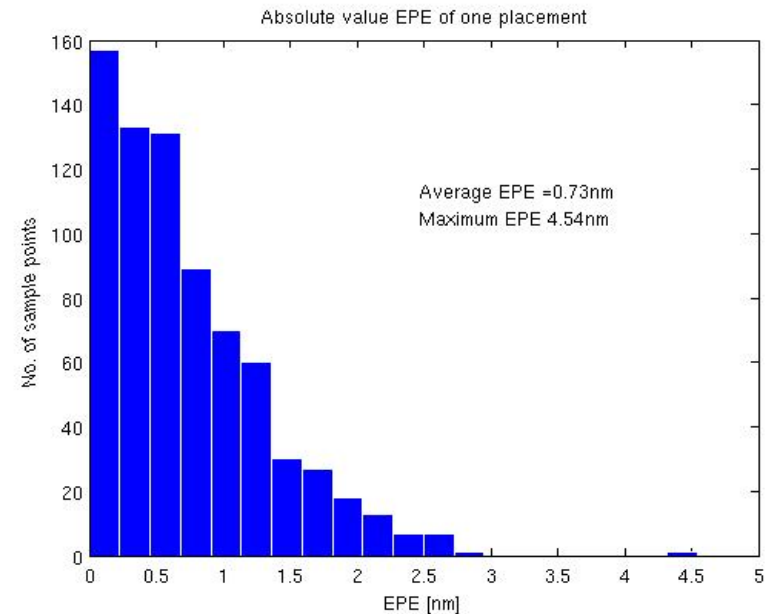
- ❑ More accurate than full-chip OPC (since it is a one-time-only computation so we can use long CPU time)
- ❑ Accuracy of simulation models can be completely verified (on silicon)
- ❑ Predictable timing (since the delay of each OPC version of a cell can be pre-determined)

Full-chip Simulation Results

- ❑ EPE simulation results for Metal1 layer
- ❑ Average EPE (edge placement error) – 0.731nm
- ❑ <1% of the metal1 feature width 80nm
- ❑ 4.67nm average EPE without boundary-based method



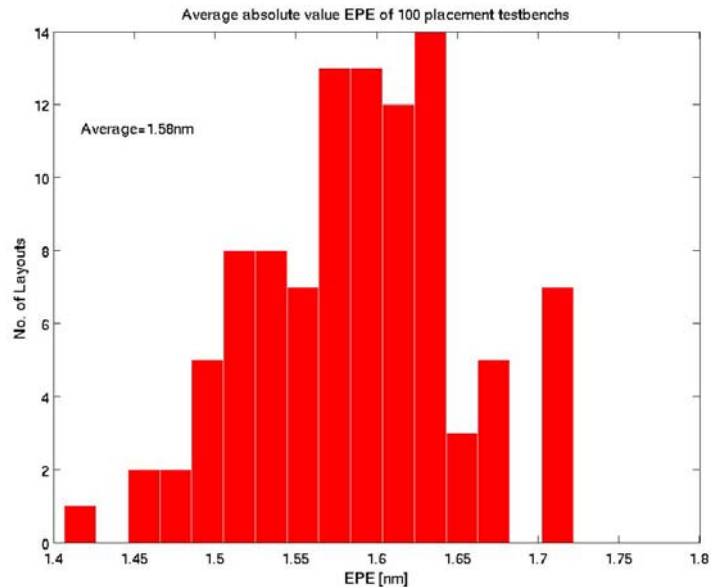
Average EPE distribution for 100 layouts



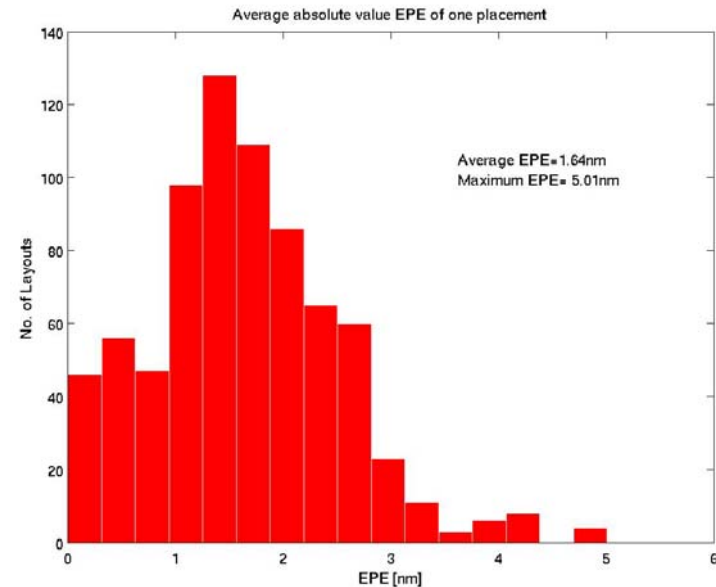
EPE distribution for sample points in one layout

Full-chip simulation results

- ❑ EPE simulation results for Poly layer
- ❑ Average EPE – 1.59nm, Average maxEPE – 4.83
- ❑ 3.5% of the poly feature width 45nm
- ❑ Average EPE – 1.96nm, Average maxEPE – 14.23 without boundary-based method



Average EPE distribution for 100 layouts



EPE distribution for sample points in one layout

Conclusions

- A promising OPC methodology for future technology nodes
 - Currently for 45nm and will be extended to 32nm and 22nm nodes
- Many benefits
 - Significantly reduced full-chip OPC runtime
 - Smaller storage requirement
 - Improved OPC accuracy
 - More predictable cell characterization