A Global Minimum Clock Distribution Network Augmentation Algorithm for Guaranteed Clock Skew Yield

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Outline

- **Background**

- Problem formulation

- Theoretical results

- New method

- Experiment

- Future works and summary

# Clock Distribution Network

- **Goal: Circuit synchronization**

- *Design objectives*
  - ⊙ **Zero skew**
  - ⊙ **Minimum wirelength**
    - ➔ **minimum power consumption**
  - ⊙ **Minimized insertion delay**

- *Objective under process variation*
  - ⊙ **Bounded skew**
   - ○ **Localization**
    - ○ **Symmetry**
    - ➔ **H-Tree**
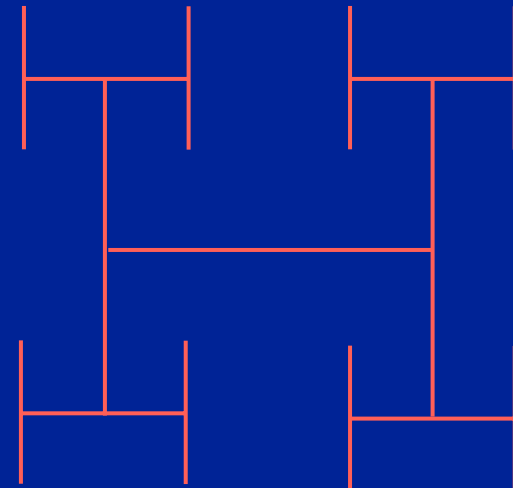
Clock Distribution Network

- *Clock tree* (ASICs)
  - Matching / clustering
  - DME
  - Minimum wirelength
  - Larger skew (variation)

- *Clock grid* (CPUs)
  - Larger wirelength
  - Minimum skew (variation)

- *Hybrid* (recent)
  - Symmetric tree on top
  - Grid in the middle
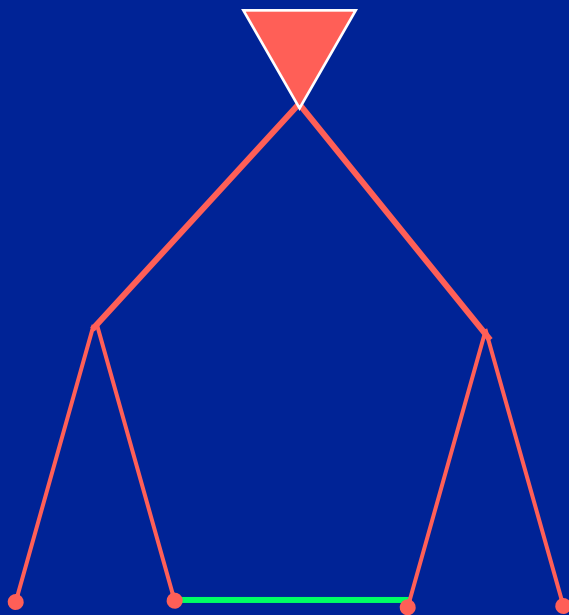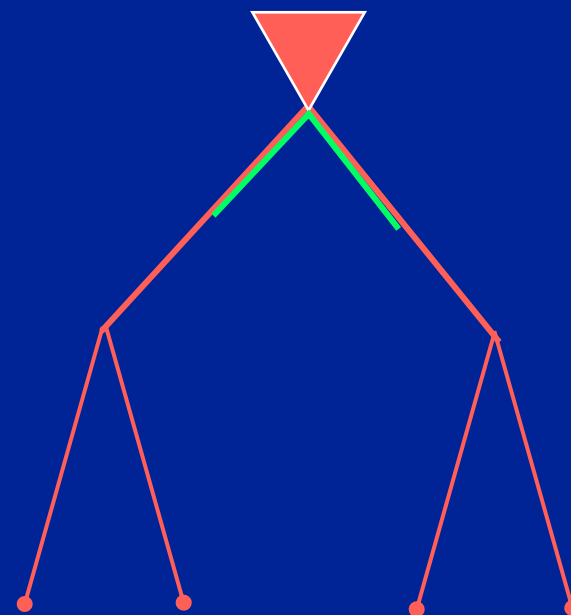 - Steiner minimum trees at bottom
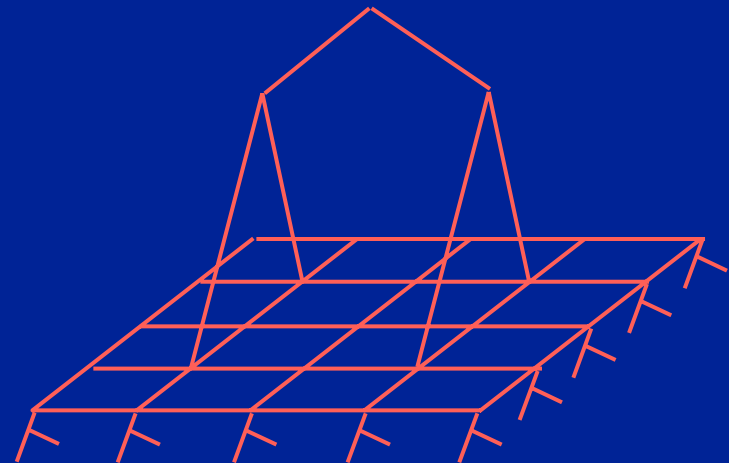
Clock Tree Link Insertion

- **Link insertion reduces clock skew**
  - Signal propagation delay is a weighted sum of the delays of the two paths

- *Pros*:
  - Reduces clock skew (variation)
  - Relatively low cost overhead

- *Cons*:
  - Wirelength increase
  - Polarity / short circuit
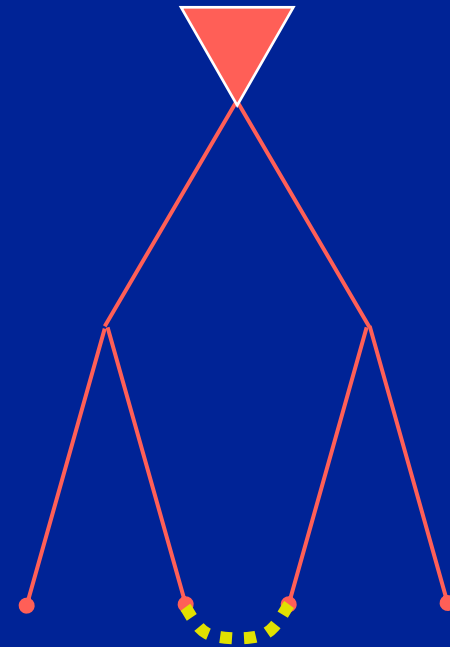
Link Insertion vs. Wire Sizing

Synchronize two
subtrees

Speedup two
subtrees

Previous Works on Link Based Clock Network

- **Rule based link insertion** [*Rajaram*, *Hu* and *Mahapatra*, DAC 04; *Rajaram*, *Pan* and *Hu*, ISPD 05]
  - ⊙ **All links are inserted at one time**
  - ⊙ **Links are inserted between equal delay nodes**
  - ⊙ **Role of the rules: find short links, distribute links evenly in clock network**

- **Incremental link insertion** [*Lam*, *Jain*, *Koh*, *Balakrishnan* and *Chen*, ICCAD 05]
  - ⊙ **Guided by statistical skew analysis, long runtime**

- **Link insertion in buffered network** [*Venkataraman*, et al., ICCAD05; *Rajaram* and *Pan*, ISPD 06]
  - ⊙ **Short circuit risk and slew rate are discussed**

Our Contributions

- We formulate the problem as clock network augmentation *for required clock skew yield*

- *Observations* on the effect of resistive link insertion on local skew reduction for general structure clock networks

- *New heuristic*: insert many links and then selectively remove links

  - *More accurate* – guided by skew analysis

  - *More efficient* – removal sees a more global view

- Our method achieves *dominant results* on skew yield, wirelength, max skew and skew variability

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Problem Formulation

- **Given**
  - (buffered) clock distribution network *N* (in forms of electrical schematic and geometric embedding)
  - electrical parameter variations
  - clock skew yield Y_s for bound *U*

- **Find** an augmented clock network *N'* of
  - minimum wirelength and
  - skew *s* which satisfies clock skew yield requirement

$$\text{Pr}(s < U) > Y_s$$

Modeling

- **Parasitic extraction ➔ interconnect RLC networks**

- **Device models ➔ buffer circuits**

- **SPICE simulation ➔ best accuracy**

- **Variations: buffer gate length, supply voltage, wire width and sink capacitance**

$$p = p_0 + \varepsilon_1 + \varepsilon_2$$

- p_0**: nominal**
- ε_1**: intra-chip (local), spatially correlated**
- ε_2**: purely random**

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Analysis: Skew Reduction Between Two Nodes

- **Inserting a purely resistive link in an unbuffered RC clock network scales down the skew and the skew variation between the two nodes by a ratio of $r/(r+\gamma)$, where r is the resistance of the inserted link, $\gamma = G_{ii}^{-1} + G_{jj}^{-1} - 2G_{ij}^{-1}$**
  - **Conductance matrix G_{nxn} includes**
    - **$G_{ij} = -1/r_{ij}$ and**
    - **$G_{ii} = \Sigma_{j!=i} 1/r_{ij} + 1/r_{is}$**

    for n nodes excluding the clock source s
  - **Apply *rank one update for matrix inverses***
  - ***Consistent with previous observations in a clock tree***
    - **G_{ii}^{-1} is the resistance of path *(s, i)***
    - **G_{jj}^{-1} is the resistance of path *(s, j)***
    - **G_{ij}^{-1} is the common path resistance of paths *(s, i)* and *(s, j)***

Analysis: Global Skew Reduction

- *Local skew*
  - Clock signal arrival time at two specific sinks
- *Global skew*
  - Maximum of local skews

- *Effect of resistive augmentation*
  - *Reduces local skew*
  - No guarantee of global skew reduction
- *Effect of capacitive augmentation*
  - *Capacitive balancing impact*
- ➔ *Iterative link insertion does not reduce global skew monotonically*

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Overview of Our Method

- *Link insertion* between all pairs of sinks which are within a short distance ε

- *Link removal* based on statistical yield analysis and two heuristic rules, for minimum wirelength and skew yield compromise

- *Link consolidation* by replacing minimum spanning trees with Steiner minimum trees for further wirelength reduction

Advantages of Our Method

- *Smooth and monotonic optimization process*
  - starting from the "batch" augmented clock network
  - remove links iteratively

- *Accurate analysis*
  - based on the augmented clock network
  - (not on initial tree)

- *Ease of physical routing of the inserted links*
  - minimum wirelength increase
  - (unconfirmed with P&R flow)

Clock Network Augmentation for Clock Skew Yield

Input: Clock network N in electrical schematic and geometric embedding

           electrical parameter variations

           clock skew yield Y_s for bound U

Output: augmented clock network N'

1. **Link insertion** between nearest sink pairs within a distance of ε
2. **Statistical clock skew analysis**
3. **Rule based link removal**
4. **Iterative link removal**
5. **Link consolidation** by forming Steiner trees
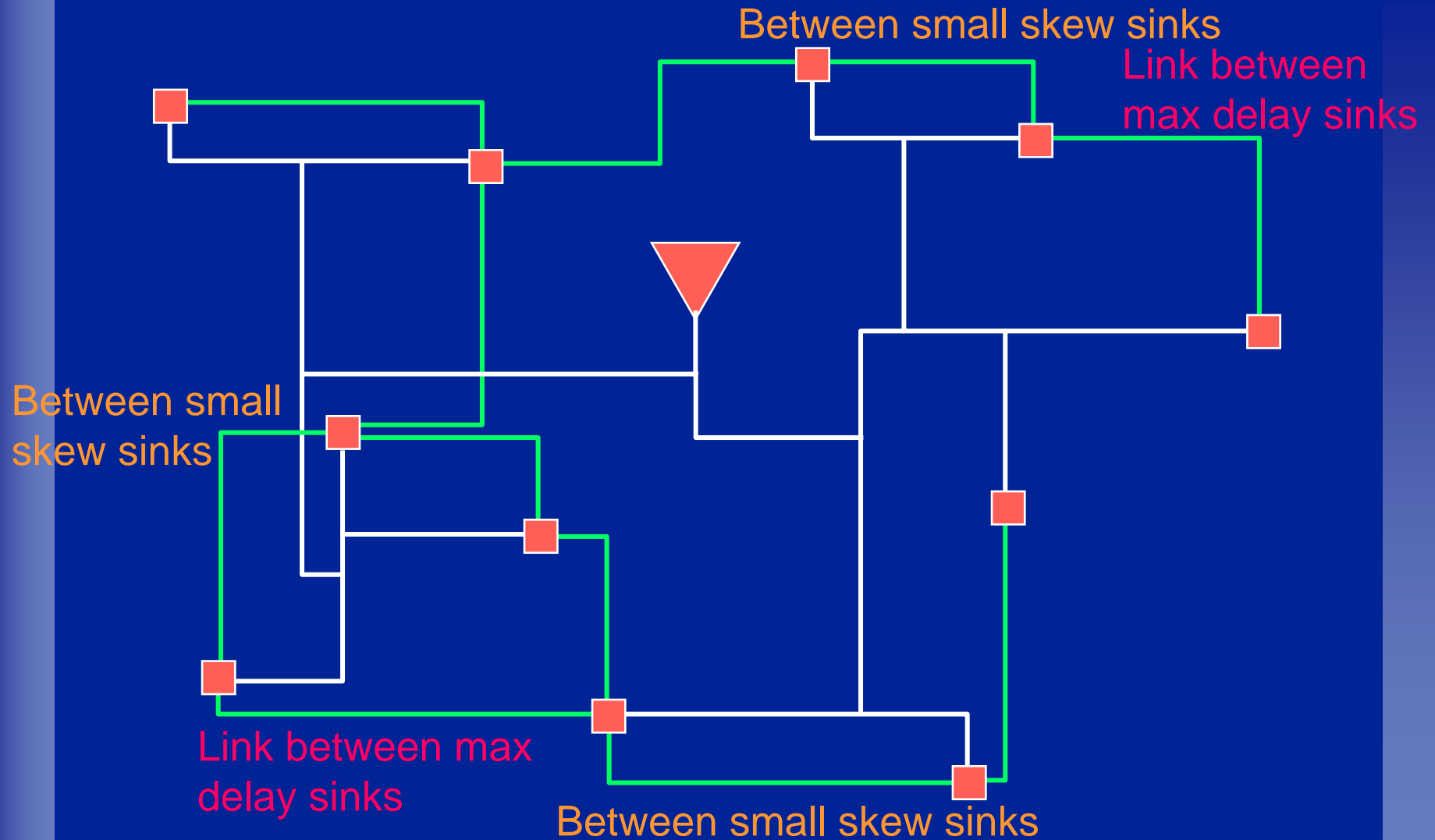6. **Final statistical clock skew yield evaluation**

Initial Link Insertion

- *Shortest links between clock tree sinks*
  - Minimum routing resource consumption
    - Minimum routing complexity
  - Minimum capacitance balance effect
    - Minimum optimization complexity

- *Increase distance threshold ε until the required clock skew yield is achieved*
  - (Intuition: more connections helps reduce skew)

Example of Link Insertion

Rule-Based Link Removal

- **Rule 1: remove links between two *maximum delay sinks* which have maximum delay in at least one of the Monte Carlo SPICE simulation runs**
  - Reduce capacitance in longest paths so that source-sink delay is reduced

- **Rule 2: remove links between two *comparable delay sinks* which have maximum delay difference no larger than a threshold α in all Monte Carlo SPICE simulation runs**
  - Remove redundant links of virtually no effect

Example of Link Removal

Between small skew sinks

Link between max delay sinks

Between small skew sinks

Link between max delay sinks

Between small skew sinks

Link Consolidation

- **If the bounding boxes of two links overlap, the two links can be merged into a *Steiner tree***
  - ⊙ **Reduce wirelength**
  - ⊙ **Implemented in a *line-scanning* algorithm**

Example of Link Consolidation

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Experimental Setup

- **ISCAS'89 circuits synthesized by SIS and placed by mPL**

- **180nm technology electrical parameters extracted by SPACE 3D**

- **Process variations $3\sigma = 15\%$**

- **Spatial correlation degrades linearly**

- **Monte Carlo simulation by 1000 HSPICE runs**

- **Initial trees are obtained as in [11] G. Venkataraman et al., "Practical Techniques to Reduce Skew and Its Variations in Buffered Clock Networks," ICCAD, pp. 592-596, 2005.**

	#sinks	Delay (ps)	Skew (ps)	WL (um)	Cap (pF)
s9234	135	367	0.5	37043	6.44
s5378	164	379	2.9	42522	7.41
s13207	500	662	11.7	129203	23.01

Main Experimental Results

	Initial Tree	Previous Method [11]	Our Method
Skew Yield	1	2.02	2.34
Wire Length	1	1.21	1.21
Max Skew	1	0.69	0.63
Skew Std. Deviation	1	1.03	0.77

Dominant results compared with previous method [11]

[11] G. Venkataraman et al., "Practical Techniques to Reduce Skew and Its Variations in Buffered Clock Networks," ICCAD, pp. 592-596, 2005.
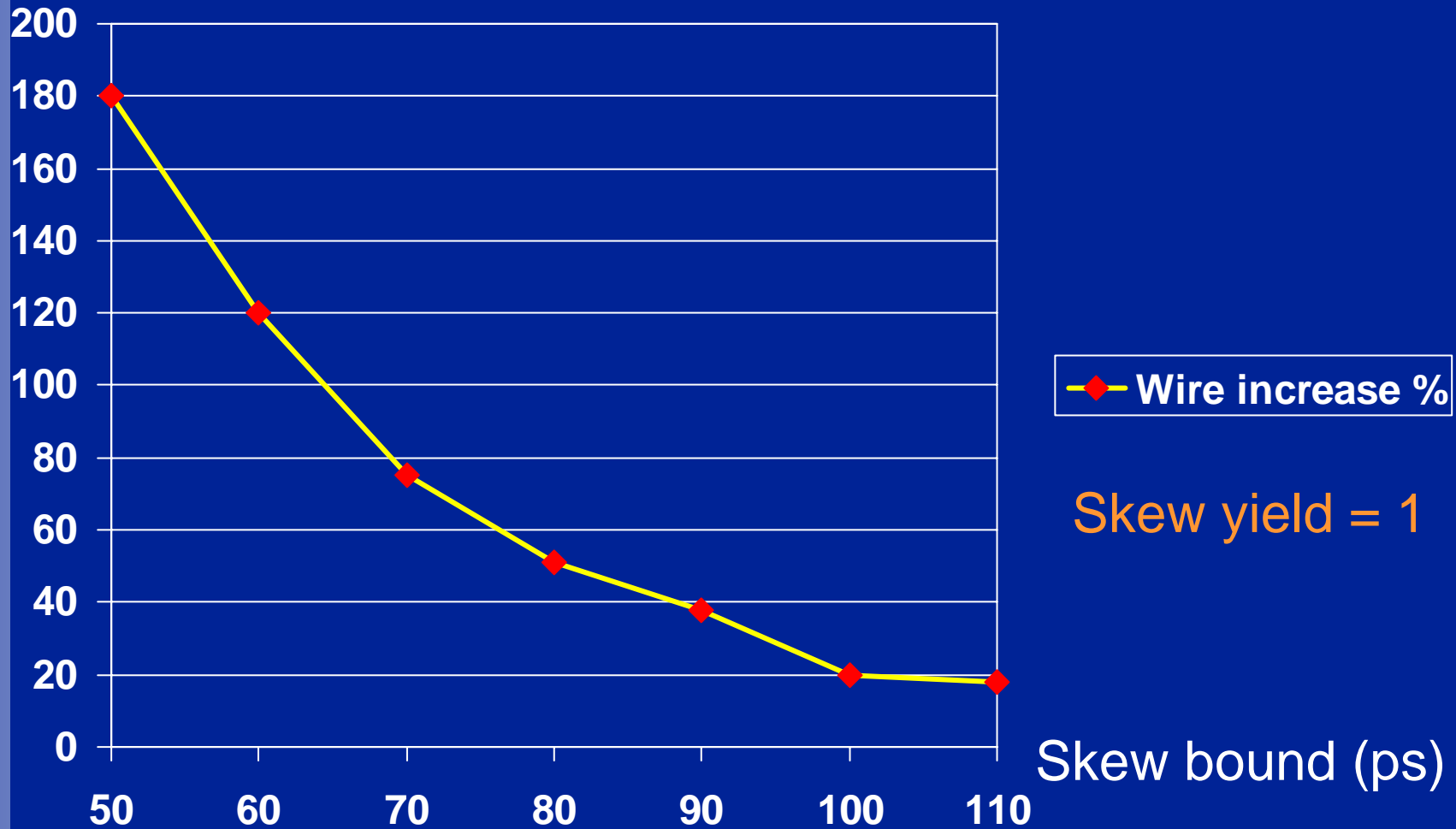
Effects of Each Step

	Tree	+ link insertion	+ insertion + link removal	+ insertion + removal + consolidation
Wirelength	1	1.89	1.28	1.21
Max skew	1	0.61	0.63	0.63
Skew std deviation	1	0.63	0.77	0.77

Skew bound is equal to 50ps for s9234 and s5378, and is 100ps for s13207

Skew yield is retained after link removal and consolidation

Skew-Wirelength Tradeoff for s13207

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Discussion and Future Work

- **Impact to signal routing**
  - Clock wirelength is usually one order of magnitude less than signal wirelength → impact of link wirelength is limited
  - Integrating method with P&R flow to confirm feasibility

- **Skew yield analysis**
  - Currently use SPICE-based Monte Carlo simulation
  - Investigating statistical skew analysis to improve estimation efficiency

- **Comparison and integration with wire sizing**

- **More comprehensive experiments with different variation models**

Summary

- **We present *minimum clock distribution network augmentation for required clock skew yield***

- ***New analysis results* on resistive link insertion on local skew reduction for general clock networks**

- ***New clock network augmentation method***
  - **Achieves dominant results**
  - **Average of *16%* clock skew yield increase, *9%* maximum skew reduction, and *25%* clock skew standard deviation reduction with identical wirelength increase compared with [11]**

Thank you !

More Discussions (1)

- **Q: Is there any risk of ringing because of the existence of loops in the linked clock network?**

- **A: such risk can be easily avoided**
  - **Initial tree: should be balanced, buffers are inserted level by level**
  - **Links are inserted between subtrees of the same level**
  - **Then, no feedback loop is induced and no risk of ringing**

More Discussions (2)

- **Q**: How to choose parameters in the proposed method? For example, how to choose the skew threshold for the second rule of link removal?

- **A**:
  - The results of our method are not sensitive to the change of the parameters. For example, if the skew threshold is small, less links are removed based on rule 2. However, the rule based removal is followed by skew analysis guided link removal, which can still remove those inefficient links. So, there is no need to meticulously tune the parameters.
  - On a coarse level, the parameters can be selected by wrapping our method with a binary search of the parameters.