Hierarchical Optimization Methodology for Wideband Low Noise Amplifiers

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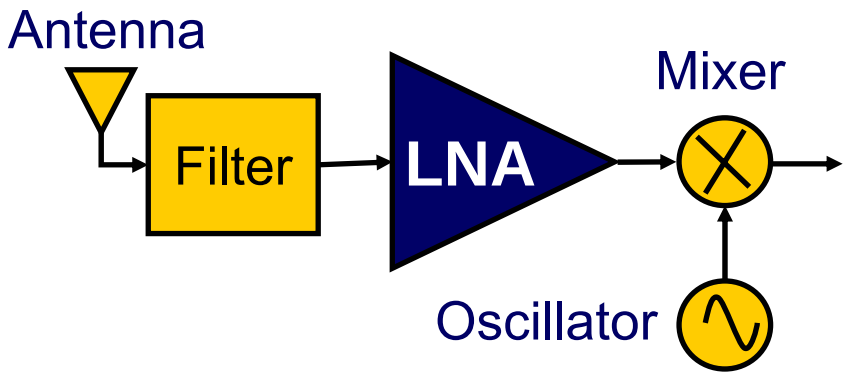
Low Noise Amplifiers: A Critical RF Front-End Component

- Low Noise Amplifiers (LNA) are a critical RF front-end component
  - Need to amplify weak signal from antenna while limiting noise
  - Greatly impacts the performance of the RF receiver



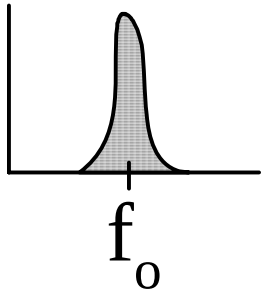
Typical RF Front-End

- On-chip wireless solutions need high performance LNAs
- Several figures of merit to simultaneously optimize
- Need to constrain passive component values for on-chip integration

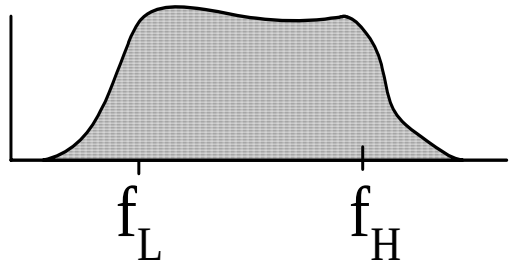
Wideband LNA Design

- Narrow-band LNA design
  - Optimize performance at single frequency depending on resonance conditions
- Wideband LNA design
  - Important for new wireless technologies implementing the ultrawideband standard (802.15.3a): 3.1 – 10.6 GHz
  - Challenging to satisfy performance constraints across large bandwidth
- Leverage design automation techniques for wideband LNA design
  - Complexity limits the effectiveness of manual design techniques
  - Better performance, greater reliability, and decreased power

Narrow-band LNA



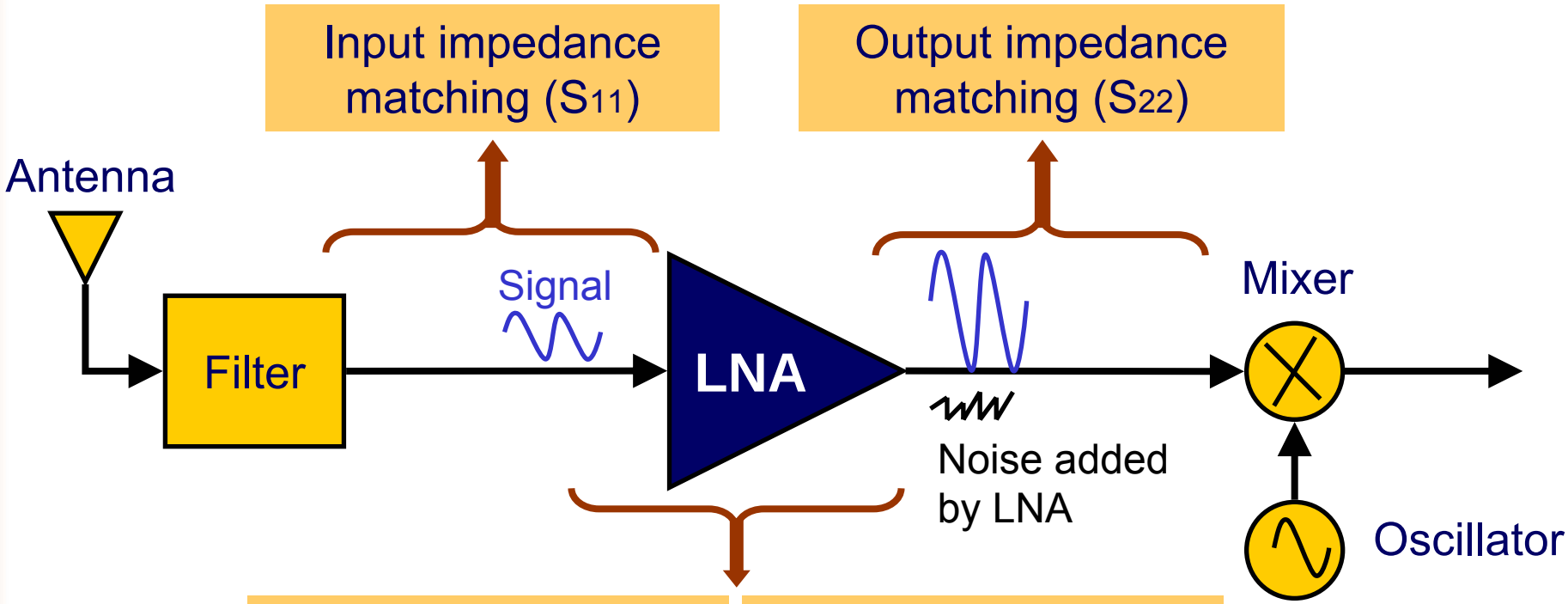
Wideband LNA



Overview

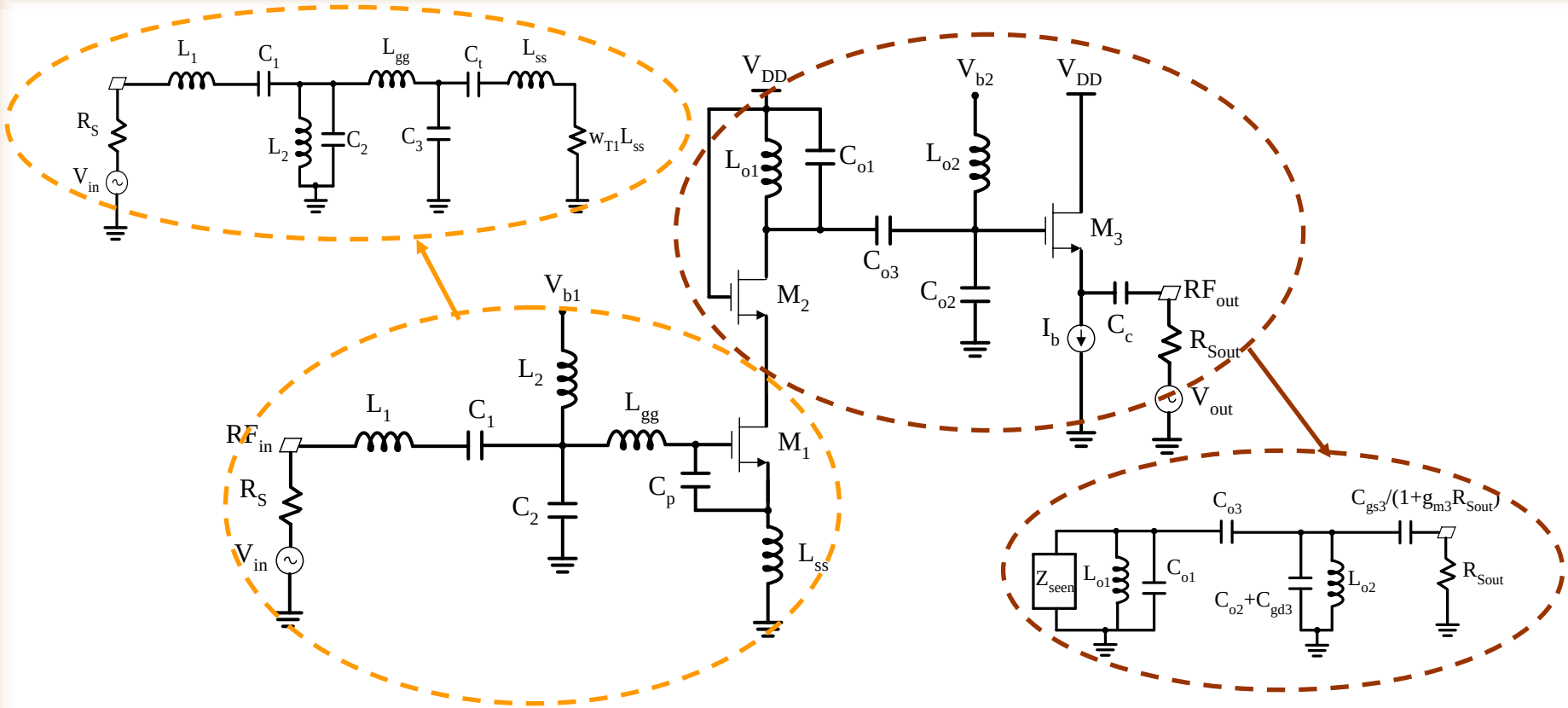
- Wideband LNA modeling and design
- Wideband LNA optimization and synthesis methodology
  - Passive component design
  - Optimization problem formulation
  - Optimization techniques and synthesis methodology
- Results
- Conclusions

LNA Performance Metrics in RF Front-End



Performance needs to be achieved across the entire wideband frequency range

Filter-Based Wideband LNA Circuit Topology



- Filter-based inductive source degeneration LNA topology has demonstrated good performance relative to alternative circuit topologies
- Filters in impedance matching network provide wideband behavior

A. Bevilacqua and A. Niknejad, IEEE JSSC, Dec. 2004.

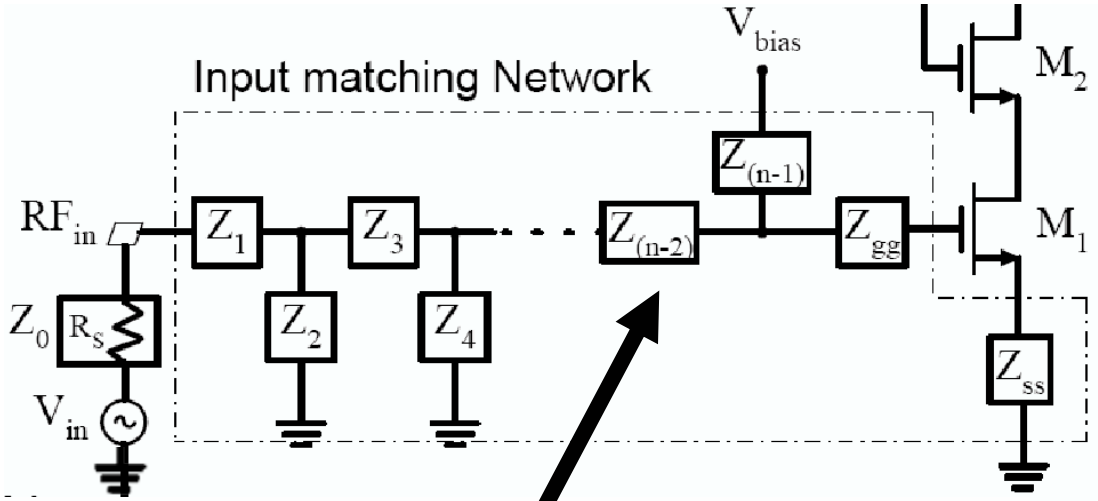
Traditional LNA Design Techniques

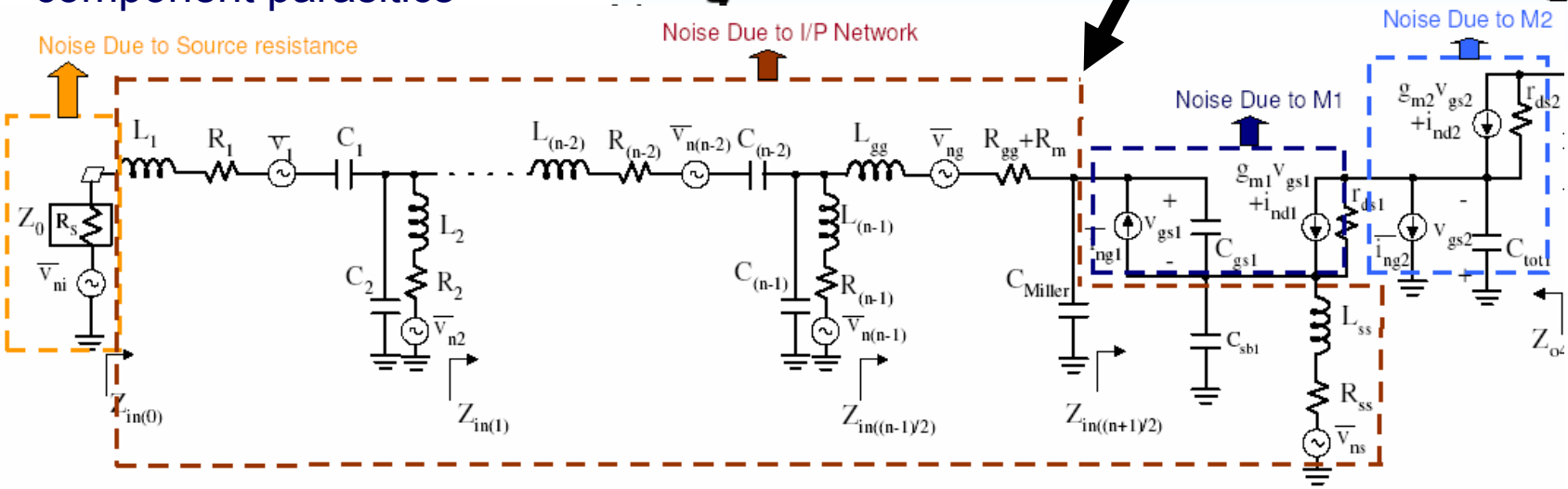
- Model figures of merit using analytical expressions [1,2]
- Manipulate models to find explicit expressions for transistor and passive element values
  - Provides design guidelines
  - Portions of the LNA circuit still require manual design
- Limited accuracy
  - Limits the complexity of models
  - Short channel effects and passive component parasitics difficult to model
- Does not take advantage of the additional degrees of freedom in design
- Determining explicit performance trade-offs difficult
- Difficult to constrain passive element values for SoC integration

1 A. Bevilacqua and A. Niknejad, IEEE JSSC, Dec. 2004.
2 A Ismail and A. Abidi, IEEE JSSC, Dec. 2004.

Accurate Analytical LNA Modeling

- Wideband LNA numerical optimization method leverages accurate analytical LNA model [1,2]
- Modeling methodology supports generalized impedance matching networks
- Captures device and passive component parasitics

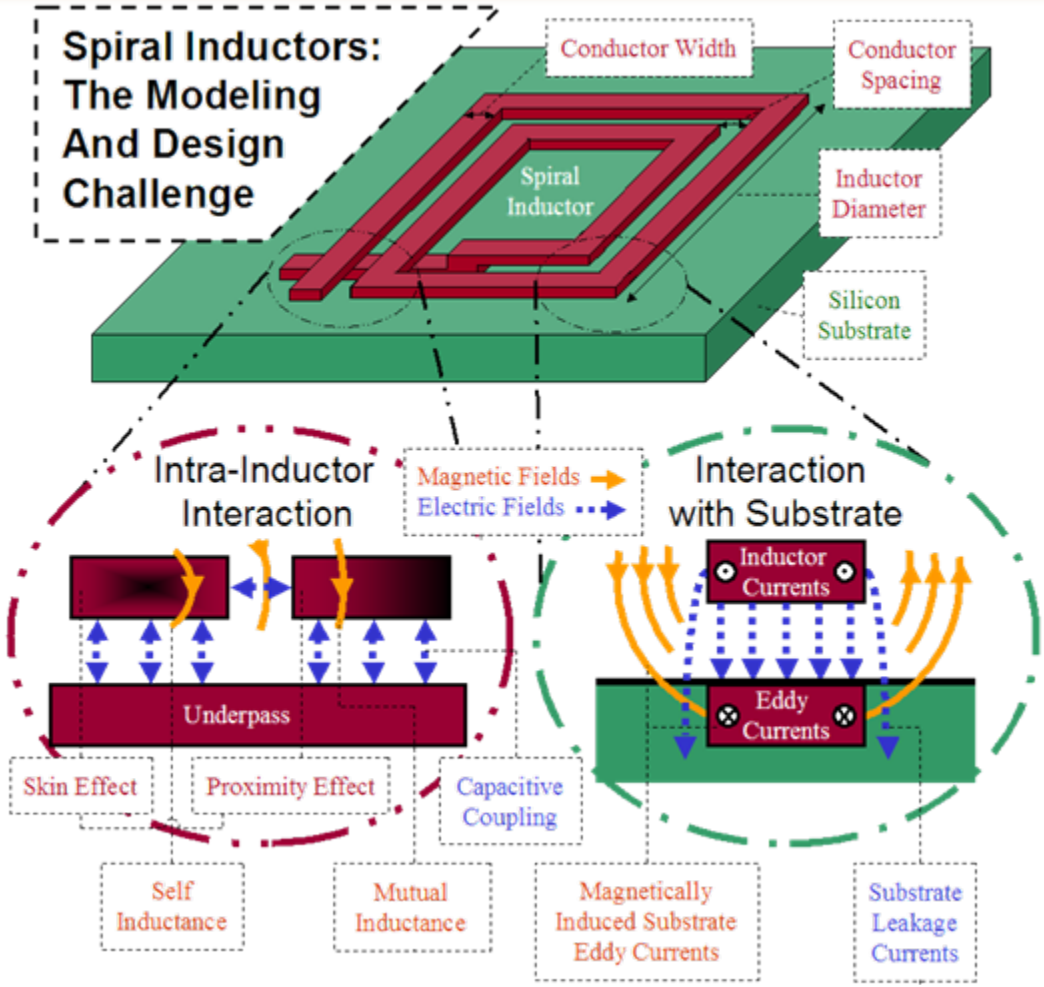




1 H. Nejati, T. Ragheb, A. Nieuwoudt and Y. Massoud, ISCAS, 2007.
2 T. Ragheb, A. Nieuwoudt and Y. Massoud, WAMICON, 2006.

Design of Passive Components for LNAs

- Passive components employed in impedance matching networks
- Modeling and design of integrated inductors challenging
- Developed an accurate and efficient compact inductor modeling method [1,2]
  - Captures complex loss mechanisms in the conductors and substrate
  - Physically verified using fabricated spiral inductor data from Mobius Microsystems
- Inductor parasitics generate noise and limit on-chip inductor values
- Low quality factors necessitate inductor optimization



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1 A. Nieuwoudt, M. McCorquodale, R. Borno, and Y. Massoud, CICC, 2005.
2 A. Nieuwoudt, M. McCorquodale, R. Borno, and Y. Massoud, IEEE EDL, Dec. 2006.

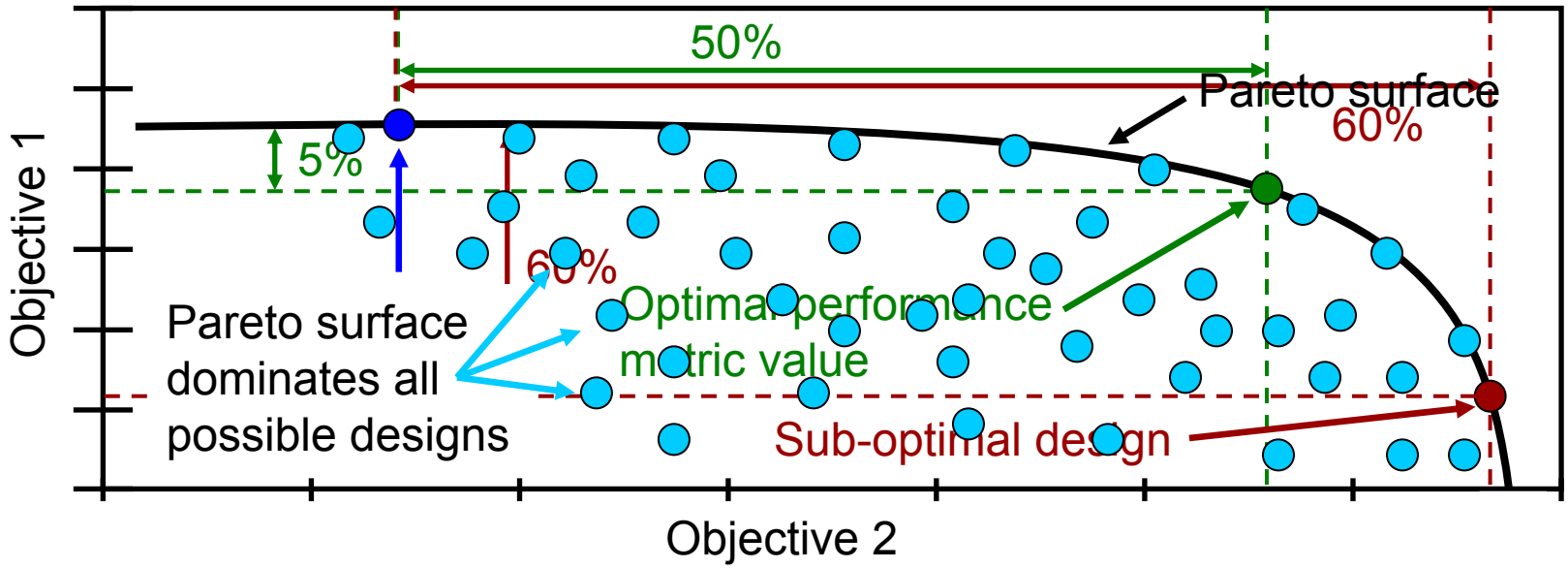
Inductor Design for Wideband LNAs

- Need to determine inductor's effective parasitic resistance [R = Real(Z_{in})] for a given effective inductance value [L = Imag(Z_{in})/2πf]
  - Relationship determined by inductor's quality factor (Q) and the operating frequency (f): $R = \frac{\omega L}{Q}$
  - For integrated inductors, the highest attainable Q is a function of L and f
  - Captures all resistive and capacitive effects
  - Valid in optimization methodology since performance is evaluated at a discrete set of frequencies
  - Use ladder circuits or 2-π model for wideband circuit simulation in SpectreRF[1,2]
- Need to find Q(L,f)
  - **Option 1:** Optimize inductor geometry for the given values of L and f during each iteration of the LNA optimization loop – computationally expensive
  - **Option 2:** Generate Pareto-optimal surrogate function [Q(L,f)] using inductor synthesis with Pareto optimization

1 A. Nieuwoudt and Y. Massoud, Analog Integrated Circuits and Signal Processing, Feb. 2007.
2 Y Cao et al., IEEE JSSC, Mar. 2003.

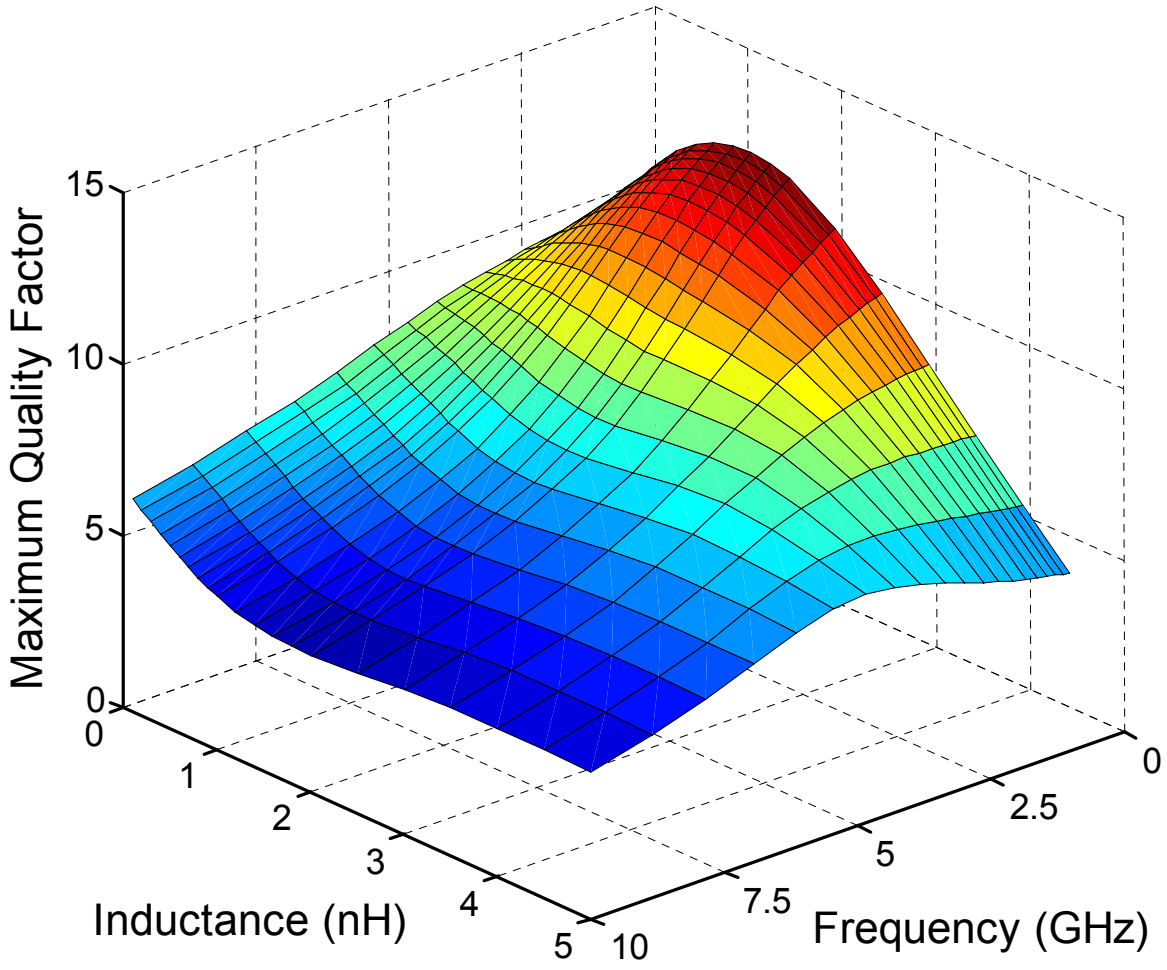
Background: Pareto Surfaces to Analyze Performance Trade-offs

- Pareto surfaces balance performance objectives without producing wasteful designs



- Generated using multi-objective optimization techniques
- Important information for circuit designers
- Can be used as a modeling tool in higher level designs

Inductor Synthesis using Surrogate Functions

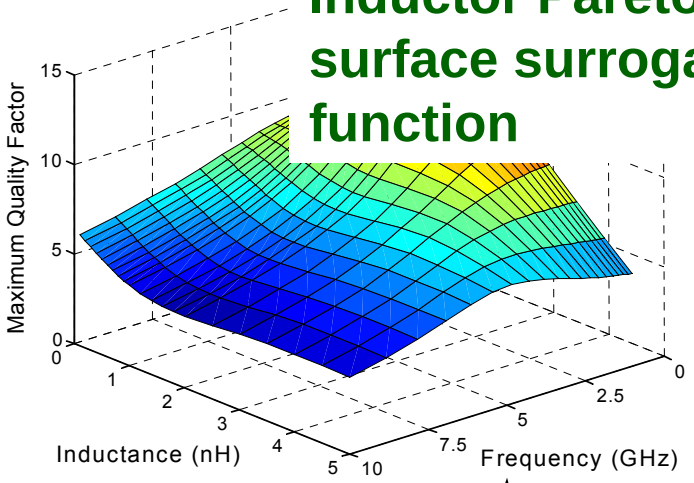


- Determine Pareto surface for Q(L,f)
- Map Pareto surface to surrogate function
  - Only must be done once during LNA design process
  - Efficiently determines optimal Q(L,f) during LNA synthesis
  - Based on inductor optimization methodology [1,2,3]

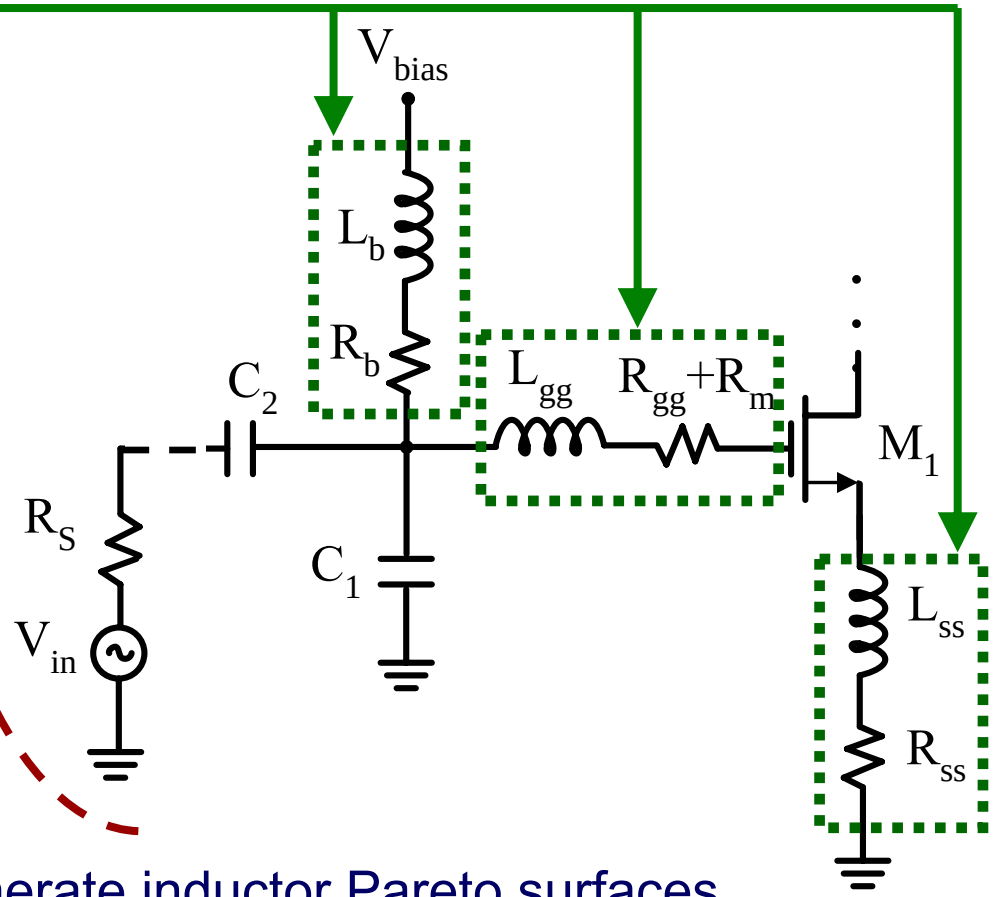
1 A. Nieuwoudt and Y.Massoud, *IEEE Trans. CAD*, Dec. 2006.
2 A. Nieuwoudt and Y. Massoud, ICCAD, 2005.
3 A. Nieuwoudt and Y. Massoud, DAC, 2005.

Using Pareto-Optimal Surrogate Functions for Integrated Inductors

Inductor Pareto surface surrogate function



LNA Model:
noise figure, impedance matching, power, gain



- Relatively inexpensive to generate inductor Pareto surfaces
- Valid for multiple LNA optimization runs in a given process technology
- Can be used hierarchically in LNA optimization process

Integrated Wideband LNA Synthesis Methodology

- Simultaneously design the input and output impedance matching networks and transistor design parameters
- Maximize LNA performance: impedance matching, noise figure, gain, and power consumption
- Must meet performance constraints across the entire frequency band
- Guarantee LNA design suitability for SoC integration
  - Use constrained optimization to limit inductor and capacitor values to reduce parasitic resistance and area
  - Consider impact of device and passive component parasitic resistances and other deep sub-micron effects

Multi-Objective Wideband LNA Synthesis Problem Formulation

$$\text{Minimize} \quad \begin{bmatrix} \overrightarrow{F}\left(\overrightarrow{x}, \overrightarrow{f}\right) \\ \overrightarrow{G}\left(\overrightarrow{x}, \overrightarrow{f}\right) \\ \overrightarrow{P}\left(\overrightarrow{x}\right) \end{bmatrix}$$

Noise Figure

Gain

Power Consumption

Optimize performance at all in-band frequencies

$$\text{Subject to} \quad \begin{pmatrix} (\overrightarrow{Z_{in}}(\overrightarrow{x}, \overrightarrow{f})) \leq (Z_{sin}) \\ (\overrightarrow{Z_{out}}(\overrightarrow{x}, \overrightarrow{f})) \leq (Z_{sout}) \\ \overrightarrow{x_{min}} \leq \overrightarrow{x} \leq \overrightarrow{x_{max}} \end{pmatrix}$$

Input and Output Impedance Matching

Constraints on linearity, area, etc.

Bound Constraints on Design Parameters

Design Parameters:

$$\overrightarrow{x} = \left[W_1, W_2, W_3, V_{gs1}, V_{gs3}, \overrightarrow{Z_{ic}}, \overrightarrow{Z_{oc}}\right]^T$$

f – Vector of frequencies

Transistor width and biasing

Input Matching Network Components

Output Matching Network Components

Single-Objective Wideband LNA Optimization

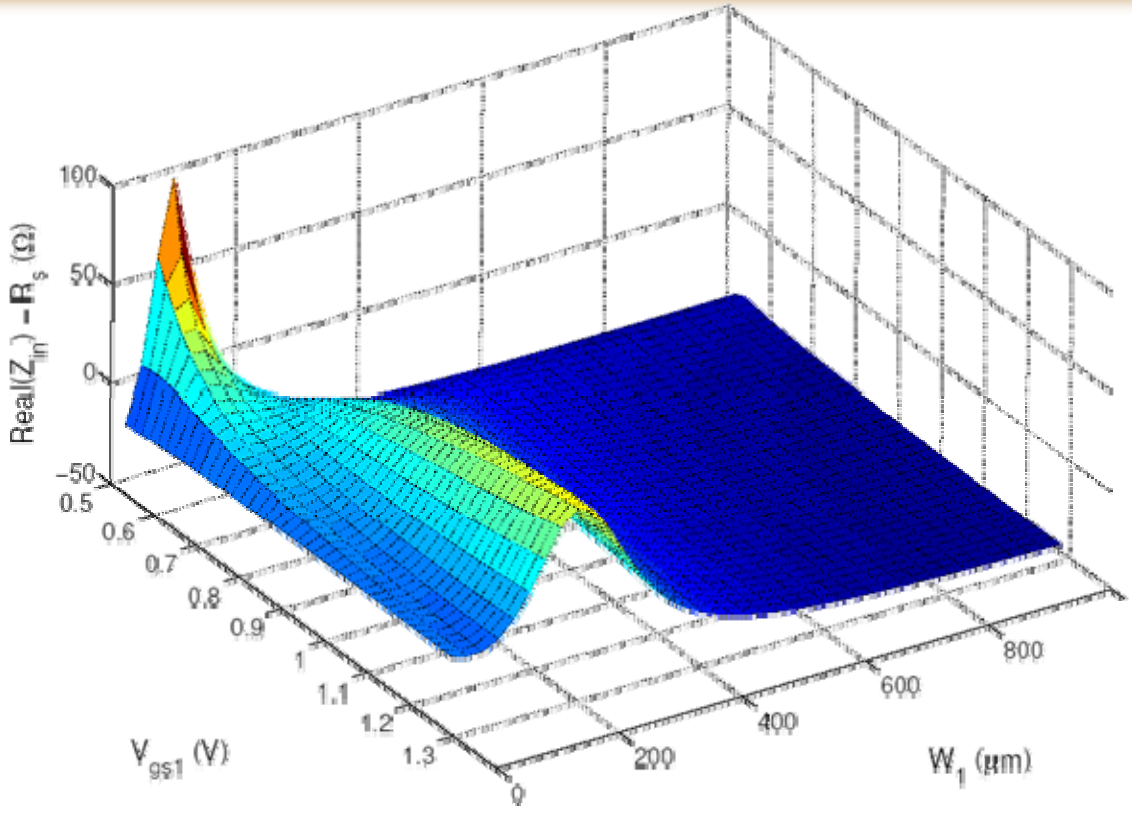
- Multi-objective optimization typically requires the solution to multiple single-objective problems
- Recast figures of merit into nonlinear constraints
  - Used for synthesis problems with fixed constraints or during the multi-objective optimization process
  - Typical problem formulation for noise figure minimization

$$\text{Minimize} \quad \| \vec{F}\left(\vec{x}, \vec{f}\right) \|_2$$

$$\text{Subject to} \quad \begin{pmatrix} \overrightarrow{Gain}\left(\vec{x}, \vec{f}\right) \geq G_{min} \\ \overrightarrow{Gain}\left(\vec{x}, \vec{f}\right) \leq G_{max} \\ \vec{P}\left(\vec{x}\right) \leq P_{max} \\ (\overrightarrow{Z_{in}}(\vec{x}, \vec{f})) \leq (Z_{sin}) \\ (\overrightarrow{Z_{out}}(\vec{x}, \vec{f})) \leq (Z_{sout}) \\ \overrightarrow{x_{min}} \leq \vec{x} \leq \overrightarrow{x_{max}} \end{pmatrix}$$

Design Space Characteristics for Wideband LNAs

- Design space characteristics important for employing appropriate optimization techniques
- Noise figure and power consumption functions are generally convex
- Input and output impedance matching and gain functions are not typically convex for wideband designs
  - Passive elements and transistor parasitics resonate with other components as values are changed in wideband design
- Non-convex constraint functions impact convergence of gradient-based optimization algorithms



Hierarchical Wideband LNA Optimization

- Since the wideband LNA design space is non-convex, cannot used gradient-based optimization alone
  - Statistical global optimization methods may not quickly approach the neighborhood of the optimal value
  - Utilize deterministic global optimization based on branch and bound
- Hierarchical multi-level wideband LNA single-objective optimization
  - Combine global optimization with gradient-based local optimization to exploit design space properties
  - Use branch and bound coupled with local gradient-based optimization for wideband LNA optimization
    - Exploit the fact that design space has a relatively small number of convex sets
    - Converge to optimal solutions
  - Hierarchically utilizes inductor Pareto surfaces in LNA optimization
- Use method of ε-constraints for multi-objective optimization since design space is not convex
  - Transforms design objectives into a series of constraints

Local Gradient-Based Optimization

- Use Sequential Quadratic Programming for local gradient-based optimization
  - Exploits gradient of objective functions and constraints
  - Significantly faster than stochastic methods for constrained optimization
    - Suitable for noisy and/or poorly behaved objective and constraint functions
    - LNA objective and constraint functions relatively well-behaved
- Employ hierarchical modeling
  - When far from the solution, use low complexity model that does not capture certain passive component and device parasitics
  - When close to the solution, use high complexity model
  - Threshold on solution derivative and maximum constraint violation used to switch between models
- Monte Carlo simulation of random LNA designs demonstrates accuracy of optimized solutions

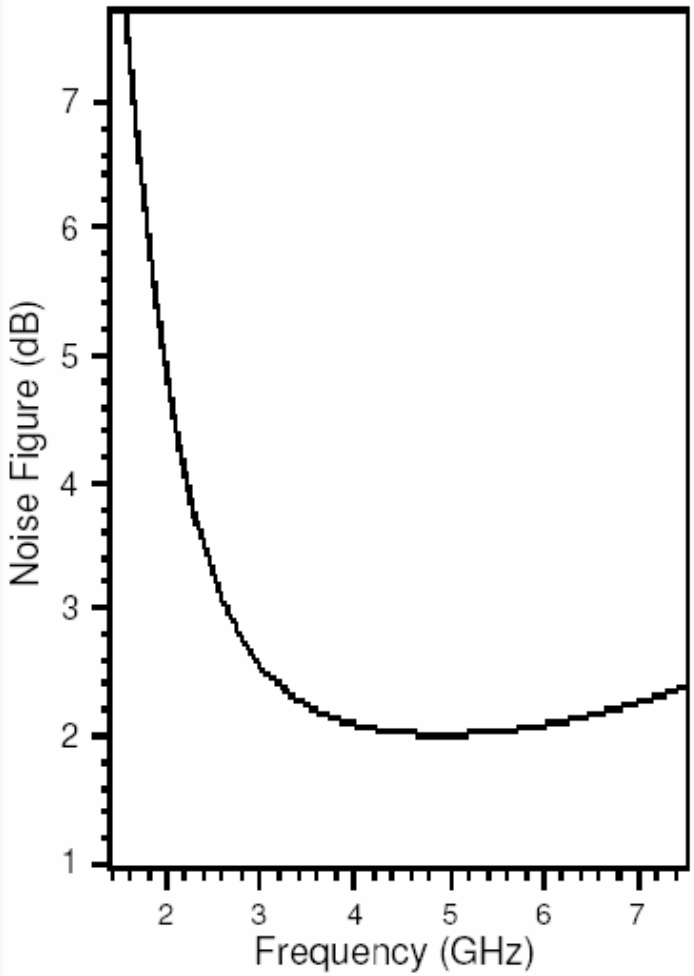
Wideband LNA Synthesis Results

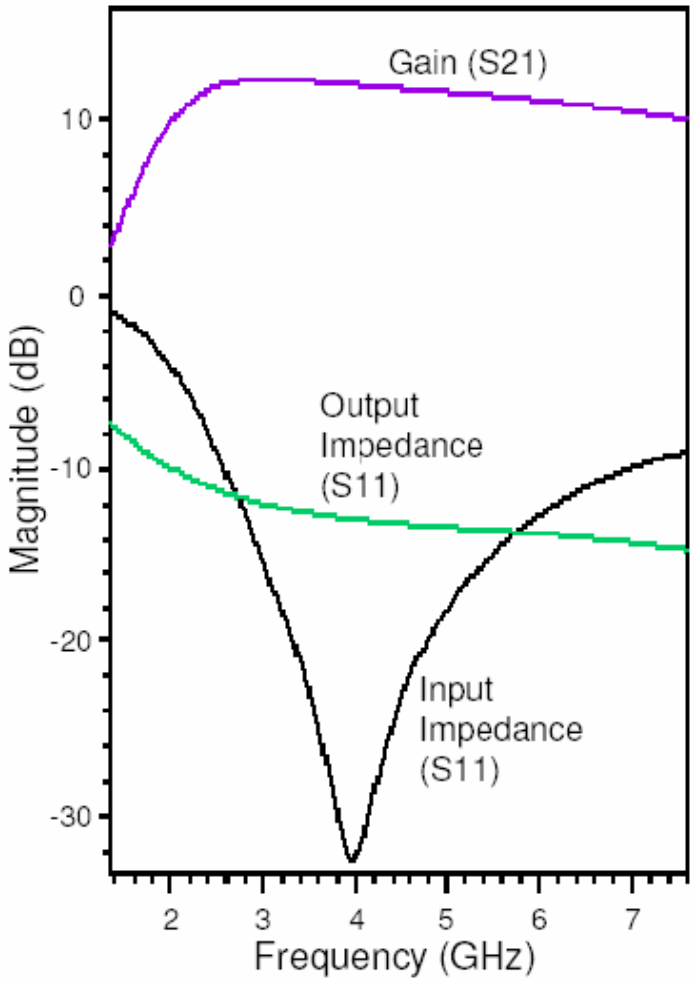
- Several design examples demonstrate efficacy of automated design technique
  - Generate designs with different operating frequencies and performance constraints
  - Simulated circuits using analytical model and Cadence SpectreRF
  - Compared results with previously proposed modeling techniques
- Generated Pareto optimal trade-off surface for noise figure and power dissipation
- Results demonstrate the versatility of the LNA synthesis approach

Design Examples

- General design problem parameters
  - Minimize noise figure
  - TSMC 0.18 μm process
  - Constrained maximum inductor and capacitor element values to 5 nH and 2 pF
- Design example 1
  - Operating frequency range: 2.5 – 7.0 GHz
  - -10 dB input/output impedance matching
- Design example 2
  - Operating frequency range: 3.1 – 10.6 GHz
  - Power constraint: 10 mW
  - -10 dB input/output impedance matching
- Design example 3
  - Operating frequency range: 3.1 – 5.1 GHz
  - Power constraint: 15 mW
  - Gain constraint: 10 dB
  - -8 dB input/output impedance matching

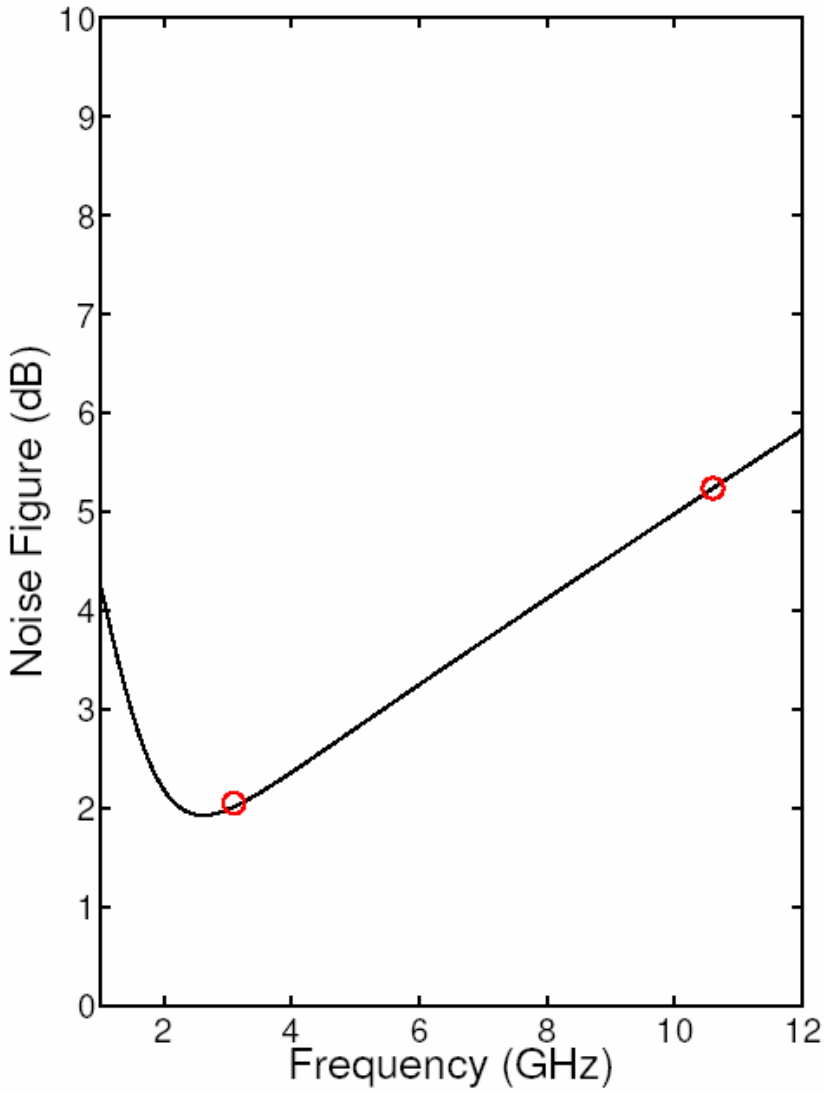
LNA Design Example 1 Results

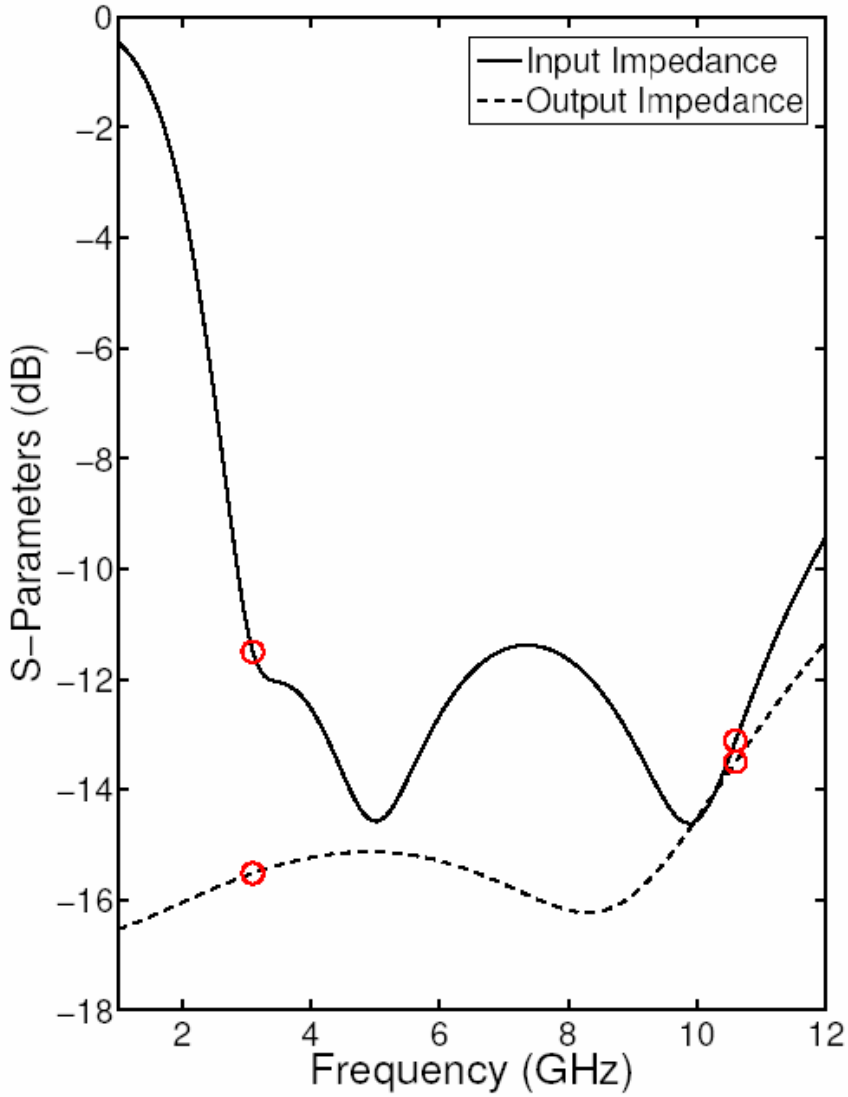




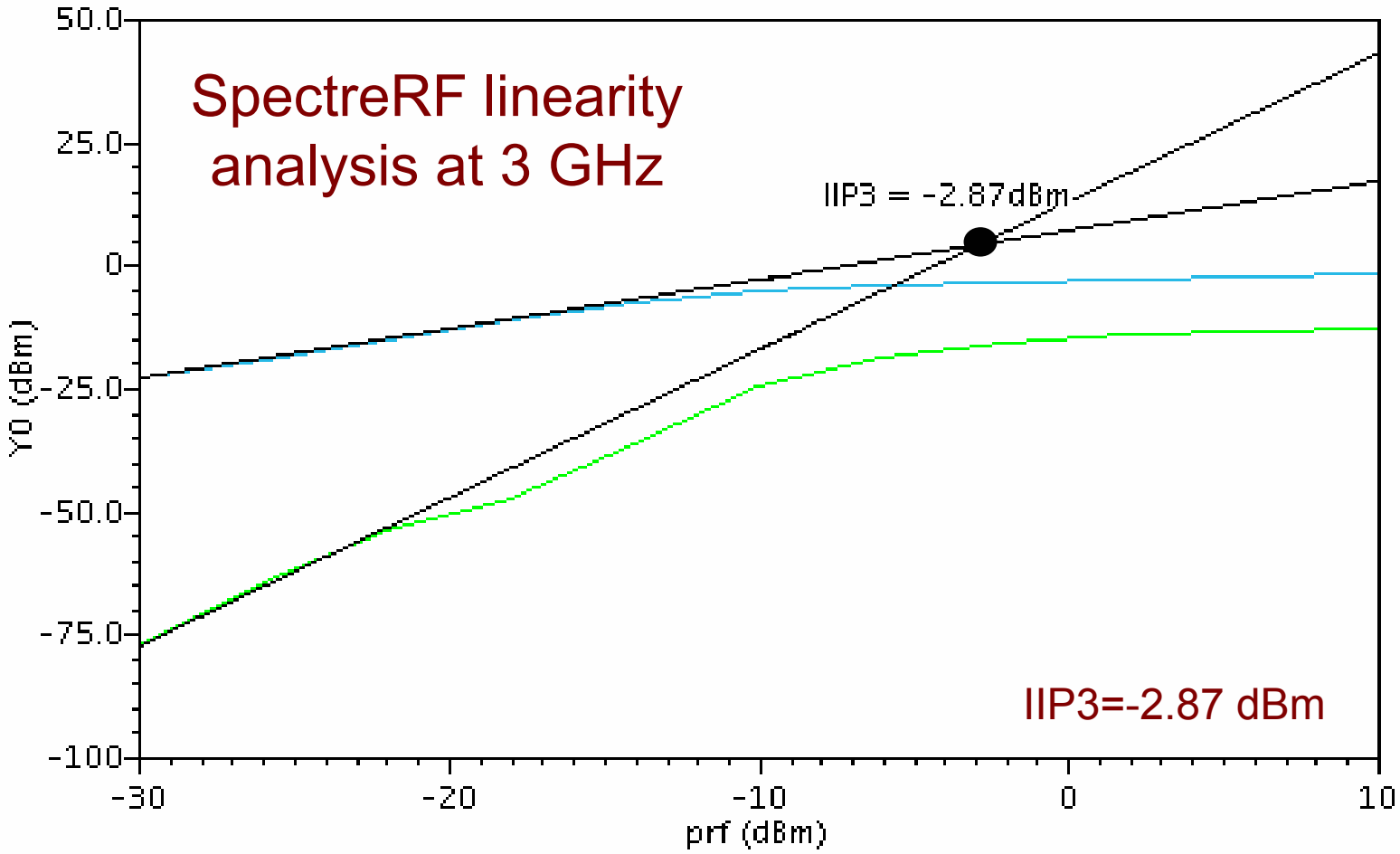
- Simulation results from SpectreRF
- Design achieves impedance matching constraints
- Low in-band noise figure

LNA Design Example 2 Results

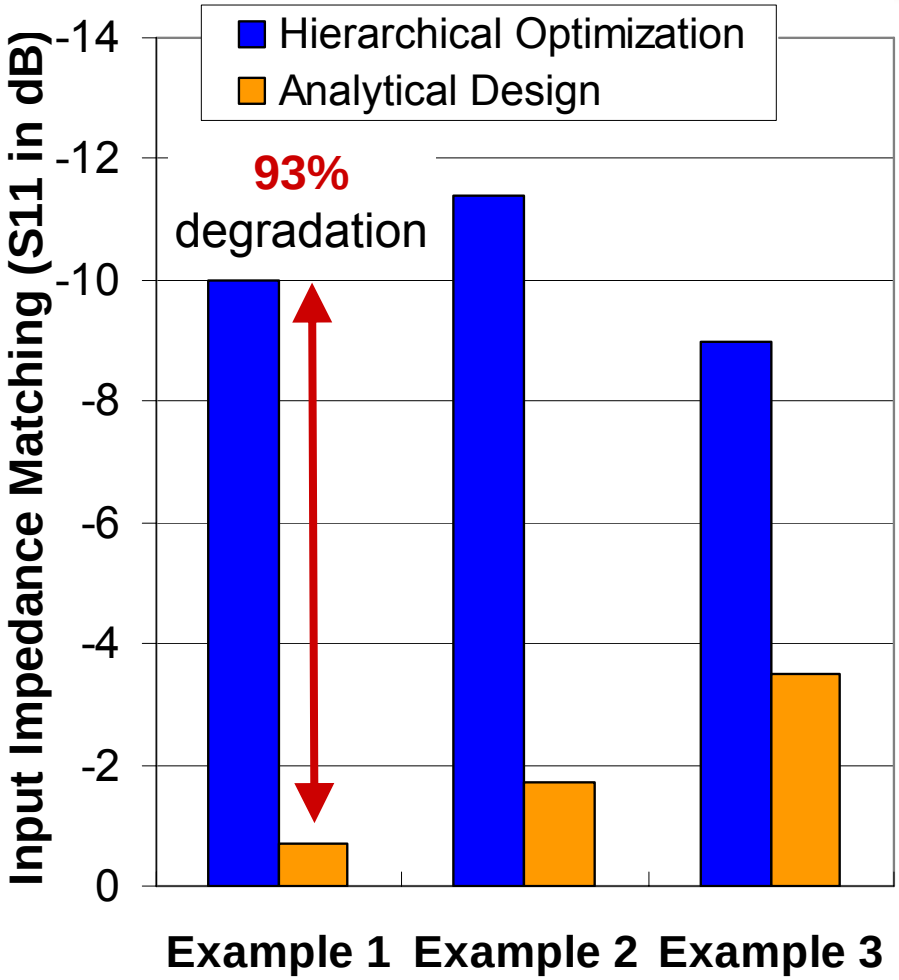


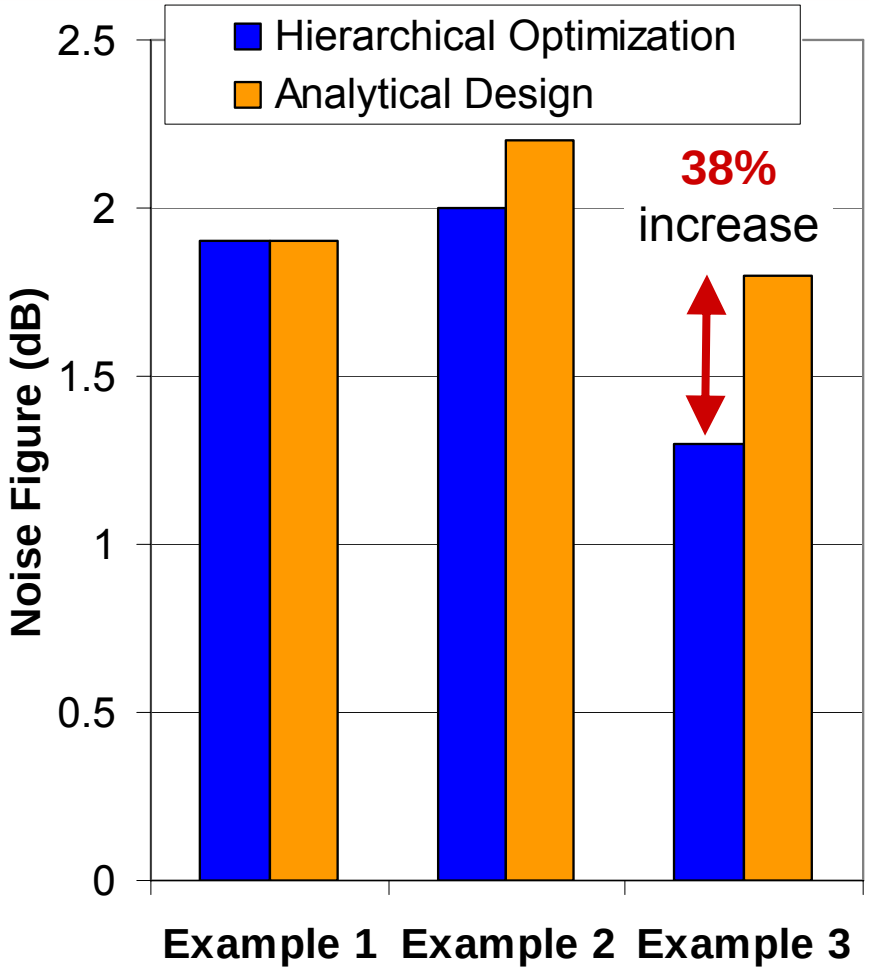


Design Example 2: Linearity



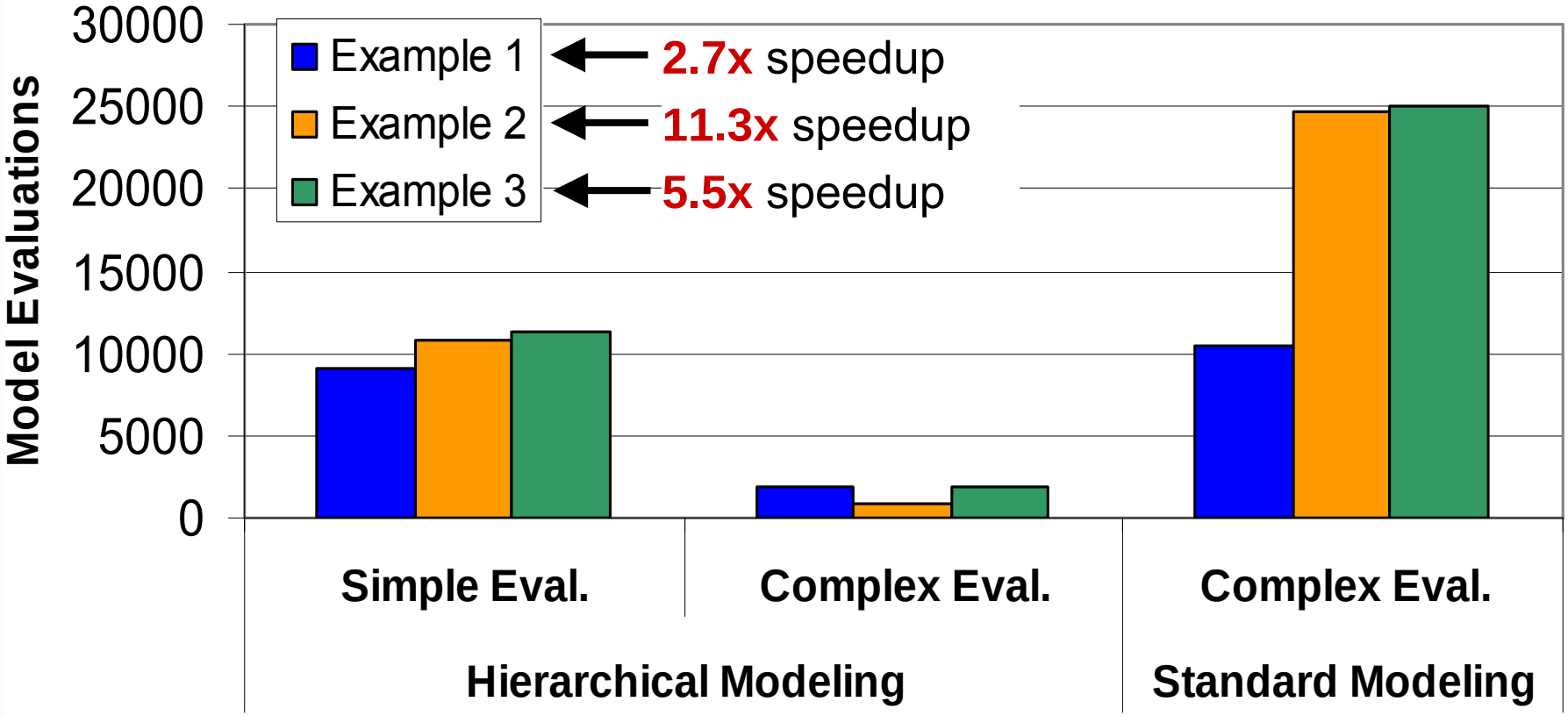
Comparison with Analytical Design





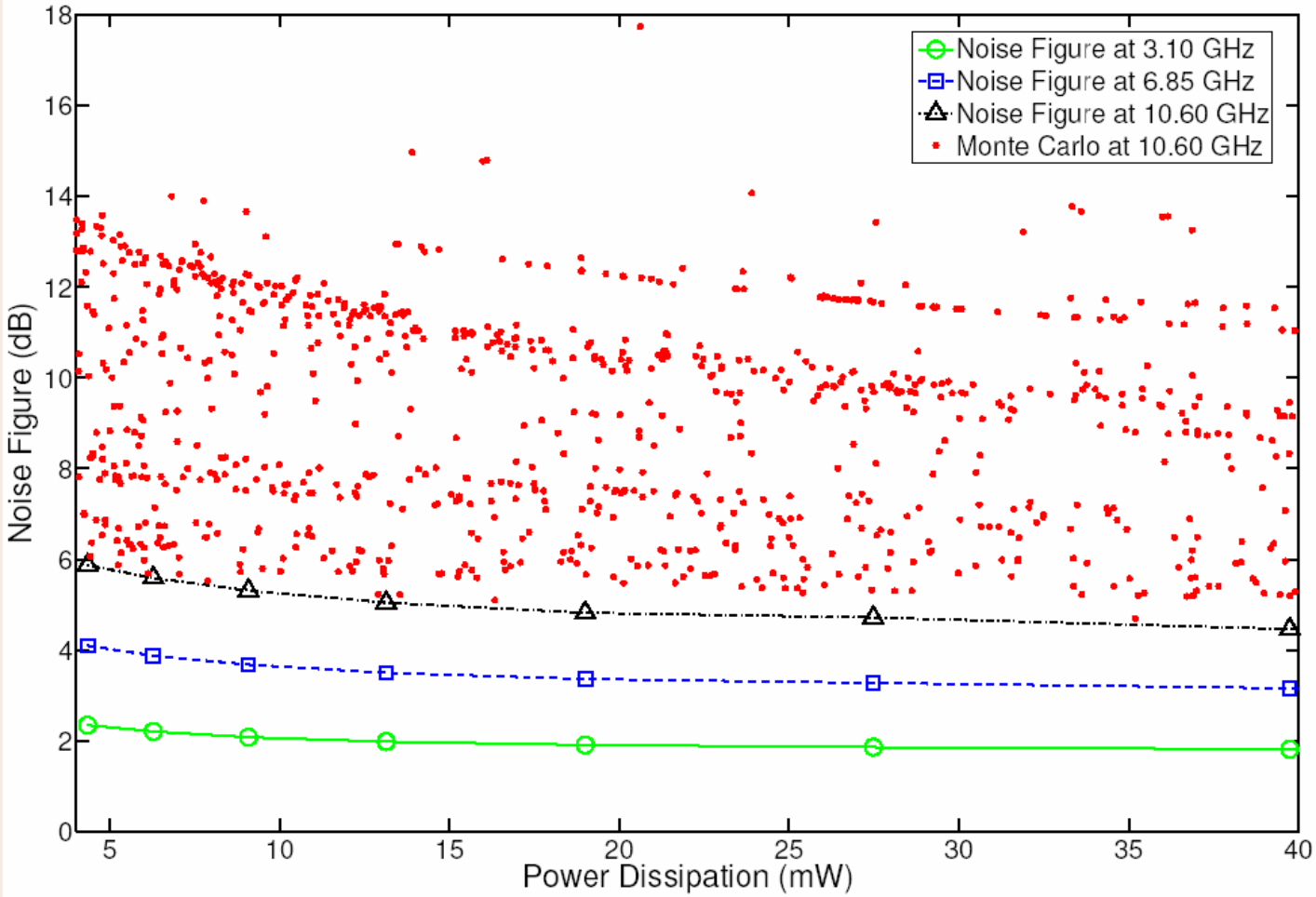
Analytical design technique:
A. Bevilacqua and A. Niknejad, IEEE JSSC, Dec. 2004.

Hierarchical Modeling Results



- Compared hierarchical modeling versus standard modeling for 3 examples
- 11.3x speedup for example 2 (438.1s for standard, 38.6s for hierarchical)
- Our analytical modeling and proposed optimization techniques provide several orders of magnitude decrease in computational complexity over a circuit-level simulation design approach

Pareto Optimization



- Little benefit in increasing power constraint beyond 20 mW
- Pareto optimization an important tool for evaluating design constraints
- Monte Carlo simulation demonstrates accuracy of method

Conclusions

- Developed a hierarchical automated design methodology for integrated wideband LNAs
  - Provides a systematic design method for wideband LNA circuits
  - Employ hierarchical Pareto optimization to efficiently capture passive component parasitics
  - Pareto optimization efficiently captures the trade-off between design constraints
- Method generates wideband LNAs designs with greater performance than those created using manual design techniques
- **Enables the efficient realization of fully integrated wideband LNAs in SoC technology**