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Ultralow-Power Reconfigurable Computing with Complementary Nano-Electromechanical Carbon Nanotube Switches

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Outline

- Motivation and Background
- Device and Technology
- Circuit Implementation
- Architectural Fabric
- Modeling and Results
- Conclusion

Motivation and Background

- CMOS devices have served us marvelously for past four decades
- Intrinsic physical limitations of CMOS devices have emerged as barrier to further scaling
  - Increasing process variations
  - Reduced transconductance
  - Higher leakage due to increasing short-channel effect

- Alternative devices need to be explored with matching circuit design style and architectural framework
  - CNTFET
  - Molecular and macro-molecular electronics
  - Single Electron Transistor (SET)
  - Quantum Cellular Automata (QCA)

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Motivation and Background

- Most of the emerging devices are prohibitive in terms of manufacturing cost or
- Does not allow a smooth transition from conventional CMOS

To overcome some of the limitations of emerging solutions:

We propose a novel device referred as - Complementary Nano Electro-Mechanical Switch (CNEMS)

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CNTs

- One-dimensional molecular-scale structures
- CNTS can be single or multi-walled
- High thermal conductivity and stability
- Adjustable and interesting electrical properties
  - Electrical conductivity: Metallic or semiconducting
  - Electrical transport: Ballistic, no scattering
- Large Young's Modulus
- Can be grown and integrated with CMOS and other electronics

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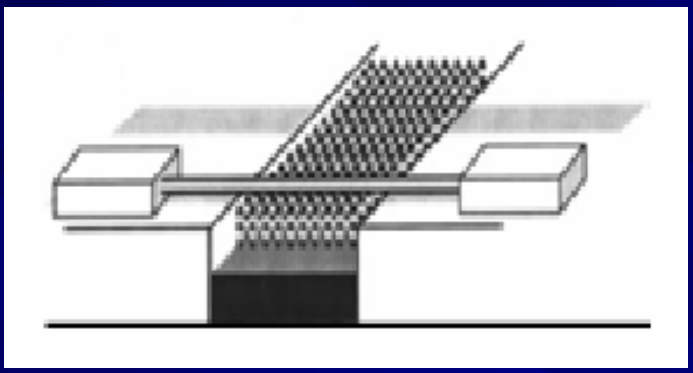
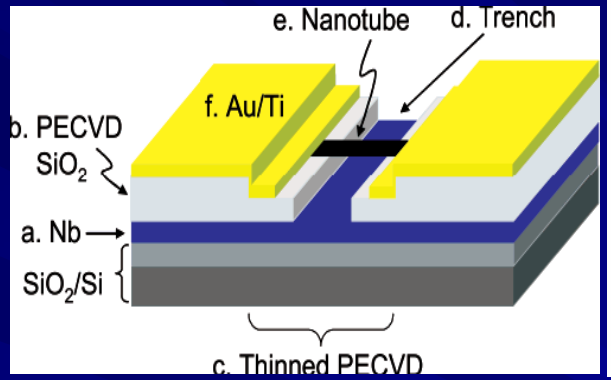
Prior Work: CNT-NEMS



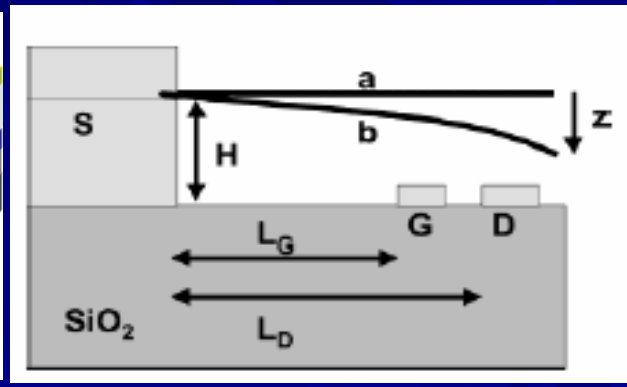
APL'05

(a)



Nano Letters'06

(b)



Nano Letters'04

(c)

(a) Self-assembled switches based on electroactuated multi-walled nanotubes; (b) Single-walled nanotubes (SWNTs) suspended over shallow trenches in SiO2, with a Nb pull electrode; (c) Three-terminal carbon nanorelay of a CNT cantilever beam switch.

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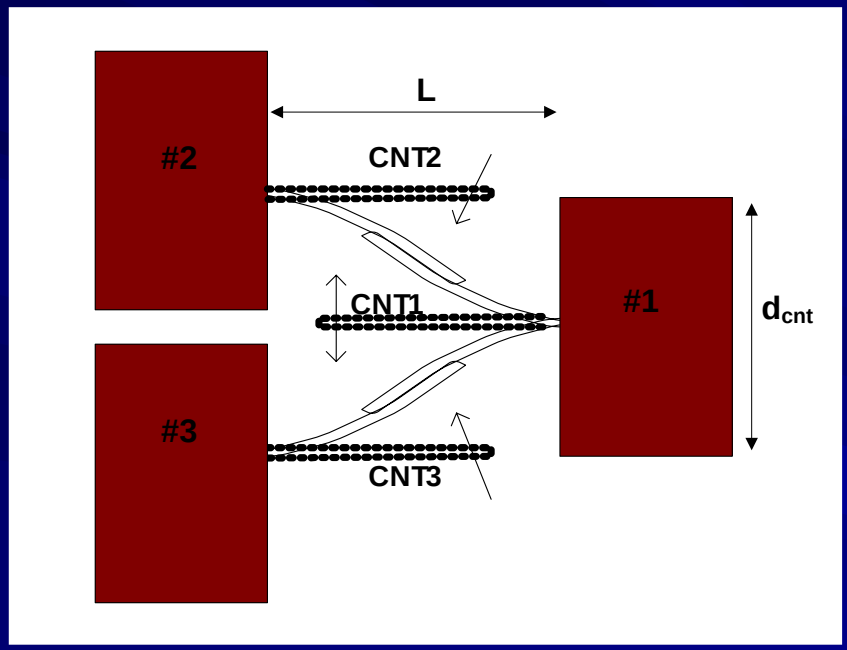
Proposed Device and Technology



The central CNT (CNT1) is either touching the top (CNT2) or bottom (CNT3) carbon nanotube. The latching is caused by the van der Waals force and the energy stored in CNT1 is recovered when it is transitioned.

Complementary nano electro-mechanical switch (CNEMS).

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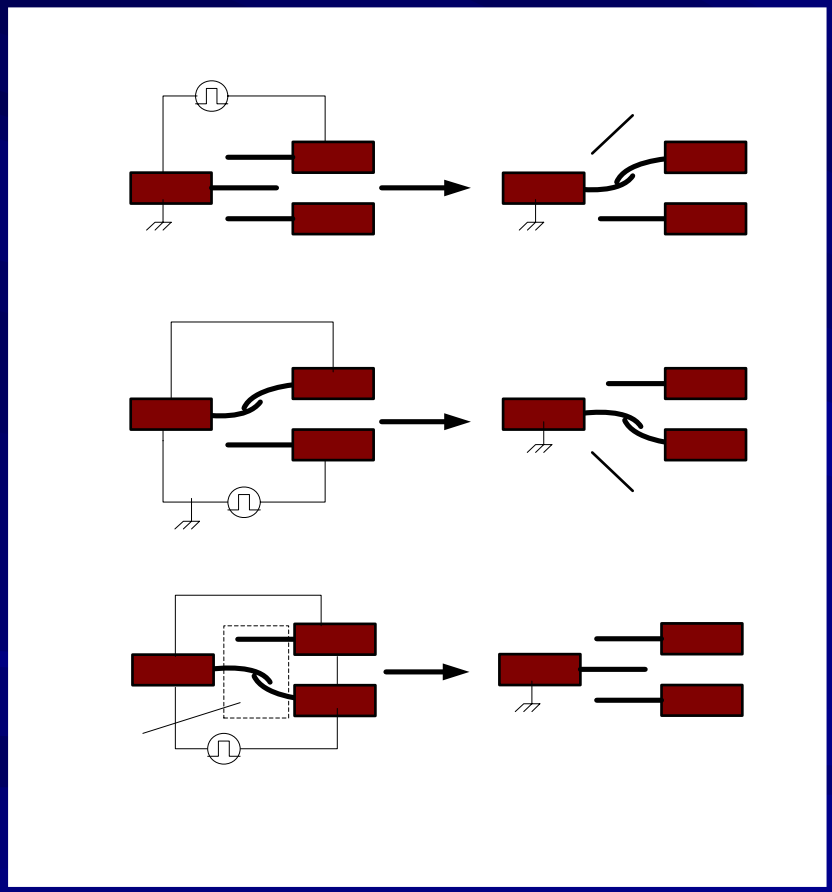
CNEMS

Schematic of CNEMS switching cycles



a) A voltage pulse (V1) causes CNT1 to be attracted to CNT2.

b) Upon touching, the van der Waals force latches CNT1 to CNT2.

c) To transition the switch, CNT1 and CNT2 are connected together and a voltage pulse (V2) is applied between CNT1 and CNT3.

d) Unlatching of CNT1 from CNT2 and latching CNT1 to CNT3. V2<<V1 because the energy stored in CNT1 in (b) is recovered in (d).

e) To reset, a bottom gate will be used to apply a voltage pulse to all CNTs

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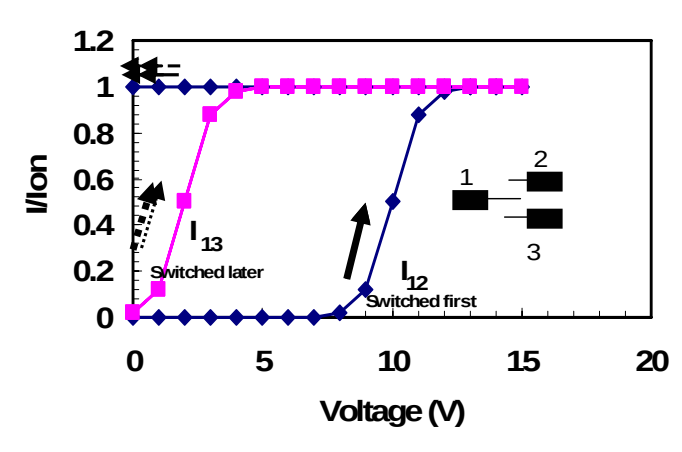
CNEMS

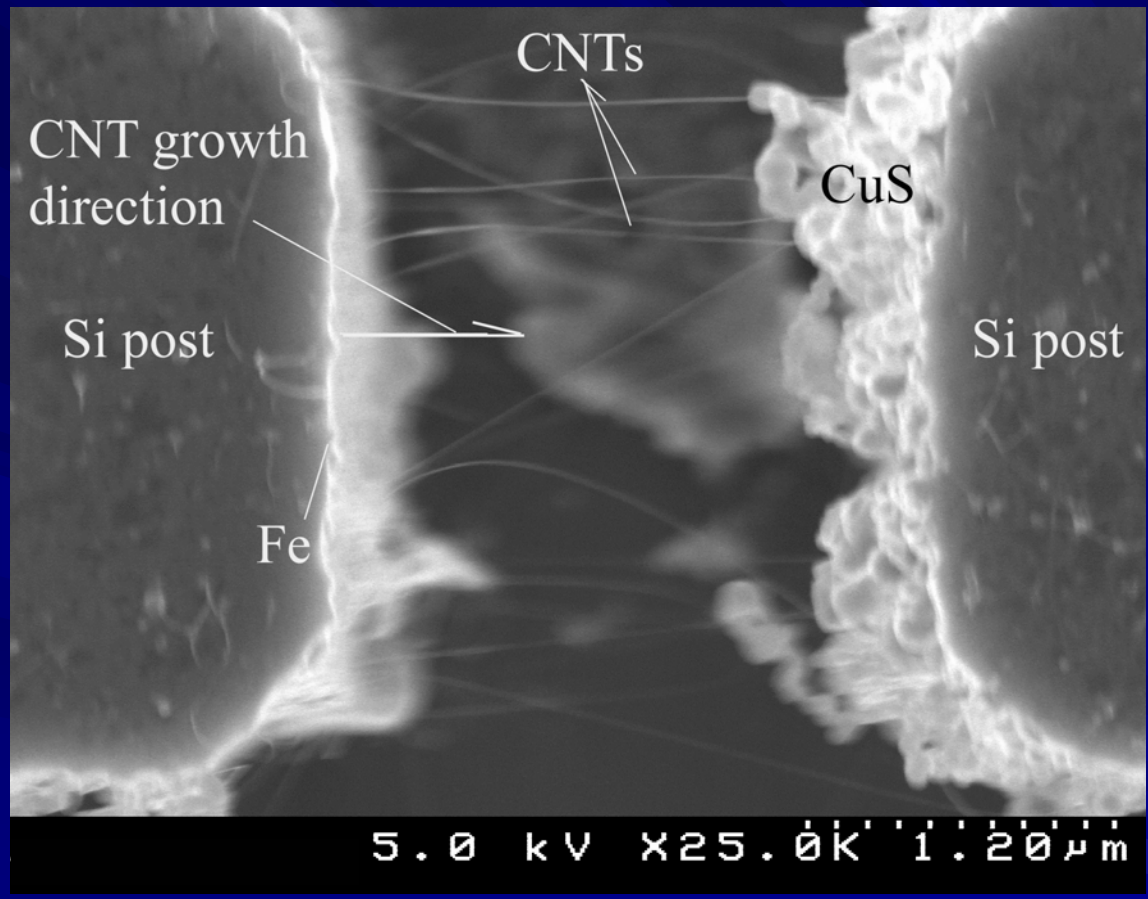


Switching characteristics of CNEMS (L~50nm, d1~3.5nm, d2~3nm, and dcnt~20nm, and d~10nm).

❑ **Scaling Issues:** **Clearly CNTs can be scaled down to 1nm diameter and sub-10nm lengths. The main constraints are:**

- **how large of an initial programming threshold voltages are allowed**
- **how precisely CNT length and CNT-CNT distances can be controlled in the fabrication process.**

Carbon Nanotube Growth Process: SEM image



Carbon nanotubes (CNTs) grown using a metal-catalyzed (iron) chemical vapor deposition technique using C2H2 between two raised silicon posts. The self-aligned and welded CNTs can be grown into any layer that can withstand the growth temperature of 500-800° C.

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CNEMS properties

- Ultra large scale integration
- Fabrication on the same substrate as CMOS
- Switching speed comparable to CMOS (~1 GHz)
- Virtually no leakage (negligible tunneling current)
- Ultra low transition power due to internal energy storage mechanism (Similar to Feynman'82 and Bennett'73 computation device)
- Latching mechanism allows every device to be used as a non-volatile memory cell

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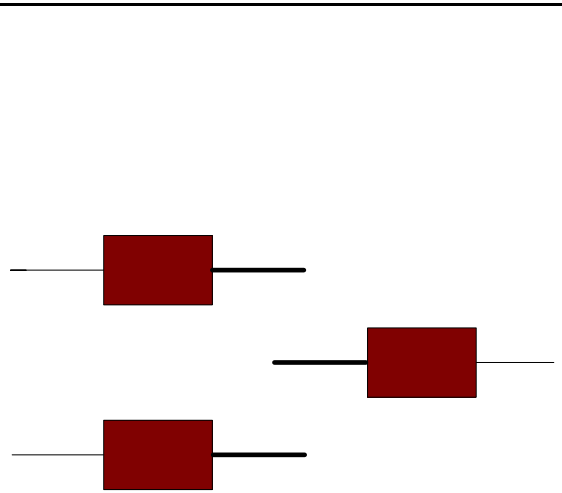
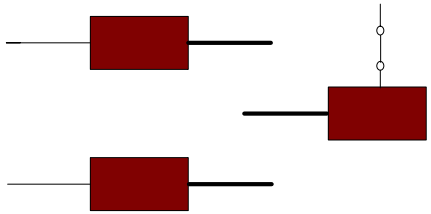
Circuit Design Style

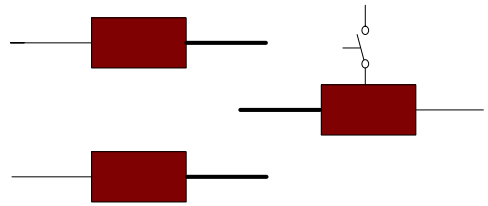


Schematic of the CNEMS



A	B	C	
0	0	0	Open
0	0	1	Indet
0	1	0	B-C
0	1	1	A-C
1	0	0	A-C
1	0	1	B-C
1	1	0	Indet
1	1	1	Open

Programming CNEMS



A	B	C	Out
0	0	0	Open
0	0	1	Illegal
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	Illegal
1	1	1	Open

Logical behavior of CNEMS

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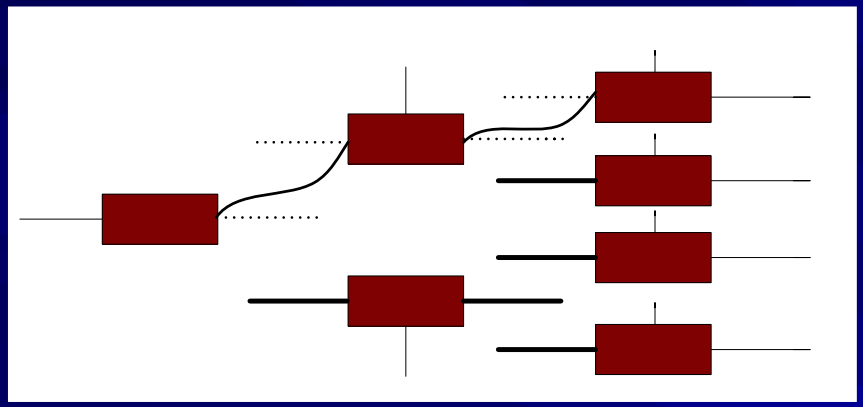
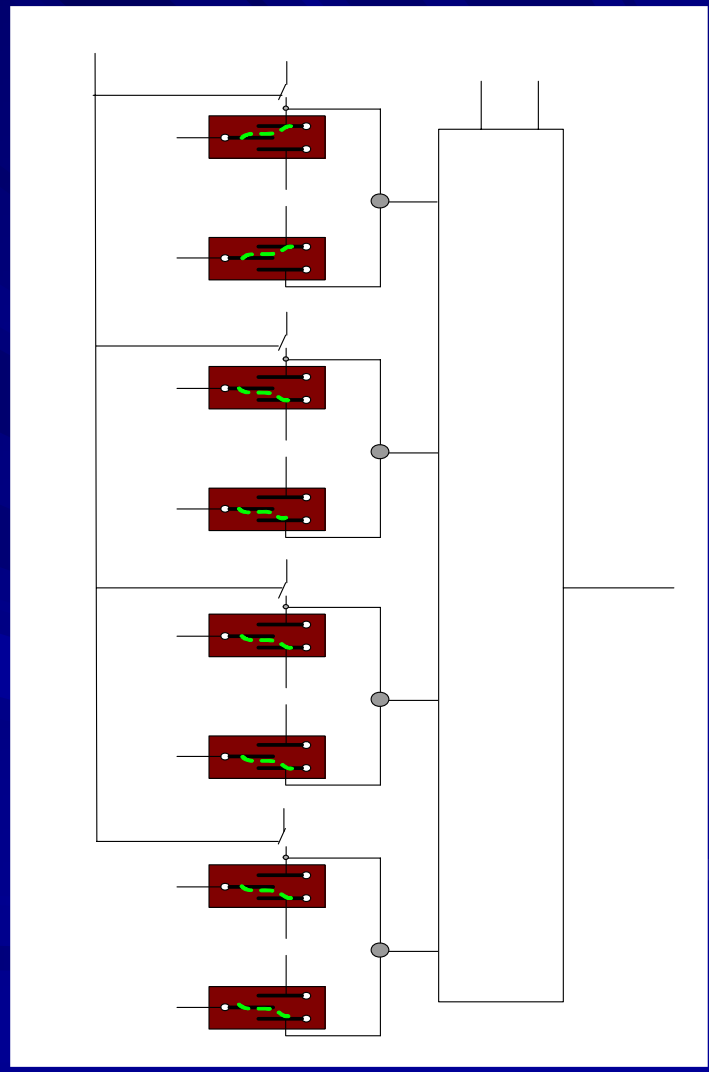
CNEMS Circuits



Configuration of a decoder (2X4) for A=1, B=1, implemented with CNEMS



Design of a Look Up Table using CNEMS

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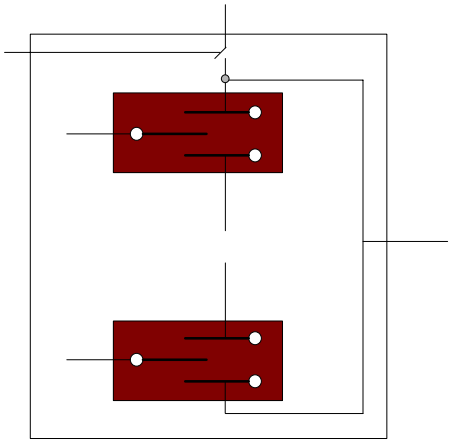
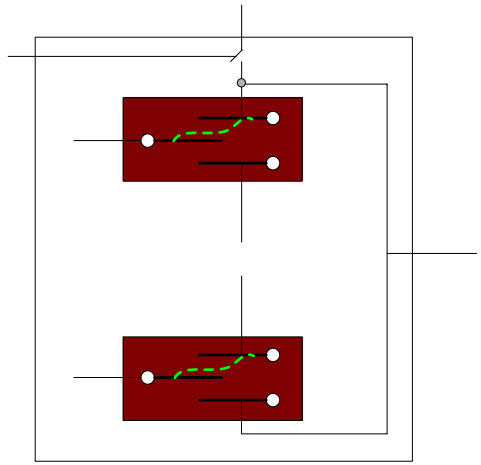
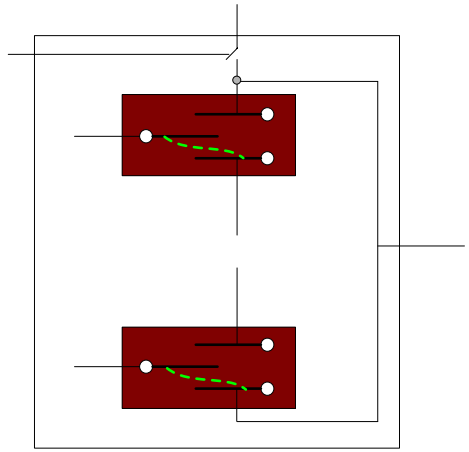
CNEMS Sequential Element



An inverting clocked latch design using the CNEMS device. The complement of the data input at D is latched by the clock.



Latch storing logic 1 in response to a data value 0. Note that it is an inverting latch.



Latch storing logic 0.

Clk

In

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Circuit Level Properties

- Conventional logic style using CNEMS is not feasible
- However, each CNEMS can be used as non-volatile memory
- Two CNEMS can make a sequential element (clocked latch)
- Radiation hard (no “soft error”)
- Negligible leakage in memory cell
- Read/write speed is comparable to CMOS
- Writing takes very little energy due to internal energy storage

- CNEMS is suitable for LUT-based architecture
  - Order of magnitude less “ON” resistance
  - No requirement of SRAM-cells for storing configuration
  - Instant-On Systems

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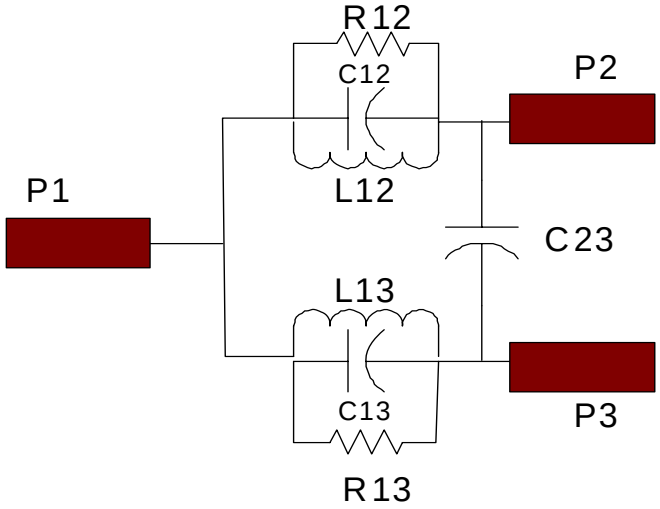
Modeling and Simulation



The simple model of the switch that is used in circuit simulation

Table 1. Comparison of delay and power results between CMOS and CNEMS implementation

Circuit	Delay (sec)		Power (watt)			
	CNEMS	CMOS (70nm, 1V, 100°C)	CNEMS	CMOS (70nm, 1V, 100°C)		
				Dynamic	Leakage	Total
Ripple Carry Adder (4-bit)	6.125e-11	1.392e-10	58.38e-08	6.570e-06	8.972e-06	1.542e-05
Magnitude Comparator (4-bit)	7.877e-11	3.481e-11	18.07e-08	1.859e-06	2.689e-06	4.548e-06
Priority encoder (8:3)	5.252e-11	7.143e-11	23.63e-08	2.470e-06	3.328e-06	5.798e-06
Even Parity (8-bit)	6.127e-11	2.205e-10	29.19e-08	3.701e-06	4.903e-06	8.604e-06

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Conclusion

- We have proposed a novel device: CNEMS, which shows promises as an alternative to CMOS at the end of its roadmap!
- Two important properties of CNEMS are:
  - Internal energy storage
  - Latching mechanism leading to non-volatile memory implementation
- Circuit design with CNEMS is proposed
  - Low power and robust logic and memory can be developed with CNEMS
  - CNEMS are also easily amenable for reconfigurable architectural fabric
- Accurate simulation models are being developed and fabrication of simple logic circuits are underway.