Single-Issue 1500MIPS Embedded DSP with Ultra Compact Codes

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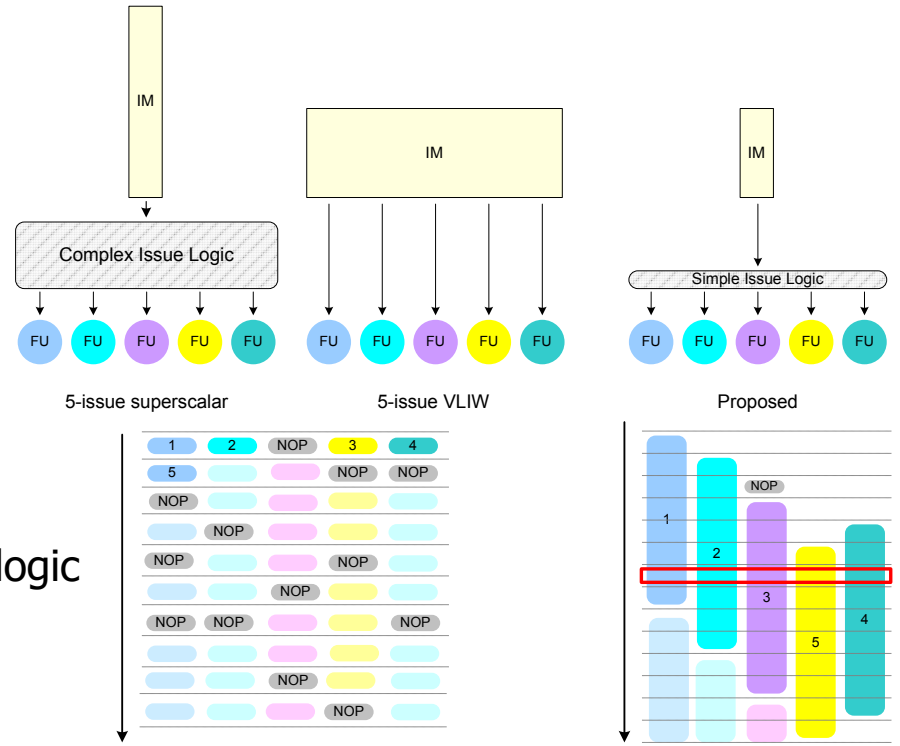
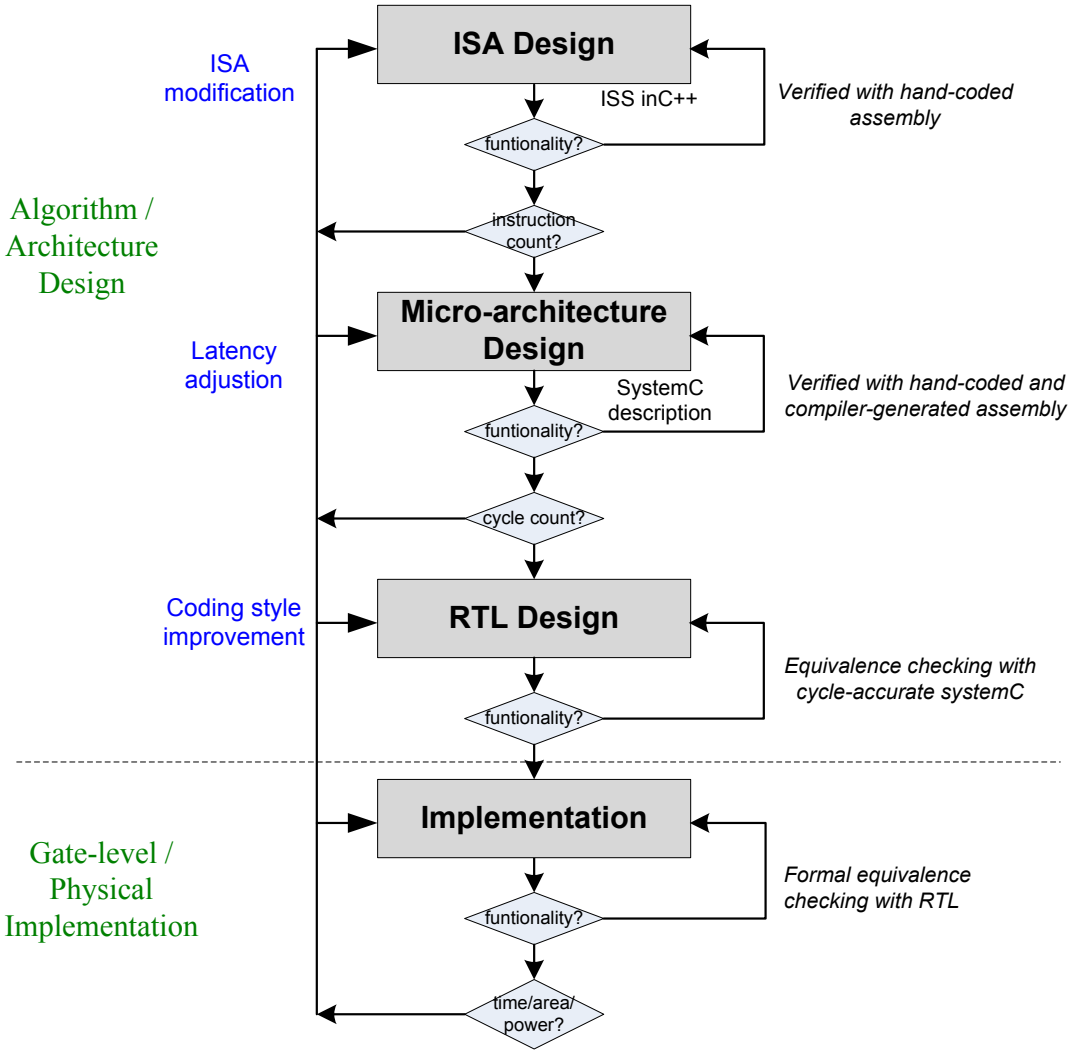
Architecture Issue

- Single-issue RISC cores
  - Only one FU is activated
    → low hardware utilization
- Multi-issue architecture
  - Pros
    - Better performance
    - Higher hardware utilization
  - Cons
    - Superscalar: complex issue logic
    - VLIW: poor code density
- Our proposed architecture
  - Simpler single-issue unit with vector processing
  - Peak performance as that of VLIW



Design Flow

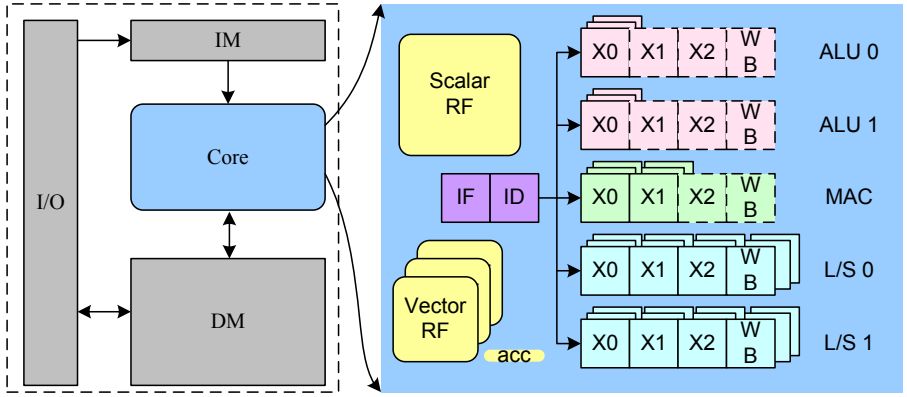

ISA Design
ISA modification
ISS inC++
Verified with hand-coded assembly
funtionality?
Algorithm / Architecture Design
instruction count?
Micro-architecture Design
Latency adjustion
SystemC description
Verified with hand-coded and compiler-generated assembly
funtionality?
cycle count?
RTL Design
Coding style improvement
Equivalence checking with cycle-accurate systemC
funtionality?
Implementation
Gate-level / Physical Implementation
Formal equivalence checking with RTL
funtionality?
time/area/ power?

Processor Design (1/2)

- Instruction set architecture design
  - Register file organization
    - Scalar RF
    - Vector RF
    - Accumulator
  - Instruction set
    - Three types
      - scalar instructions
      - vector-scalar instructions
      - vector instructions
    - Functionality
      - program flow control
      - memory reference
      - arithmetic
  - Instruction encoding
    - 16/32-bit encoding for instructions with/without immediate
  - Instruction-set simulator in cycle-accurate SystemC

Processor Design (2/2)

- Design space exploration
  - Functional unit configuration
  - Vector length
  - Number of vector registers
- Micro-architecture design
  - Single-issue logic modified from RISC
  - 6-state pipeline



Performance Evaluation

	TI C55x		Proposed DSP	
	Cycle counts	Code sizes	Cycle counts	Code sizes
FIR filtering	N*(T+2)/2+18	99	**N*(T+9)+6**	**54**
Vector add.	N+7	66	**3*N/2+5**	**40**
Vector max.	N/2+15	99	**N+15**	**56**
8-point 1D DCT	67	94	**82**	**50**

*code sizes in bytes

Silicon Implementation

Technology	TSMC 0.13um 1P8M CMOS
Core size	1.45 x 1.40 mm^2
On-chip memory	8KB DM & 4KB IM
Transistor/gate count	269,739
Max. frequency	305MHz
Power dissipation	38mW