A Multi-Drop Transmission-Line Interconnect in Si LSI

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1. Background and purpose

Global Interconnect

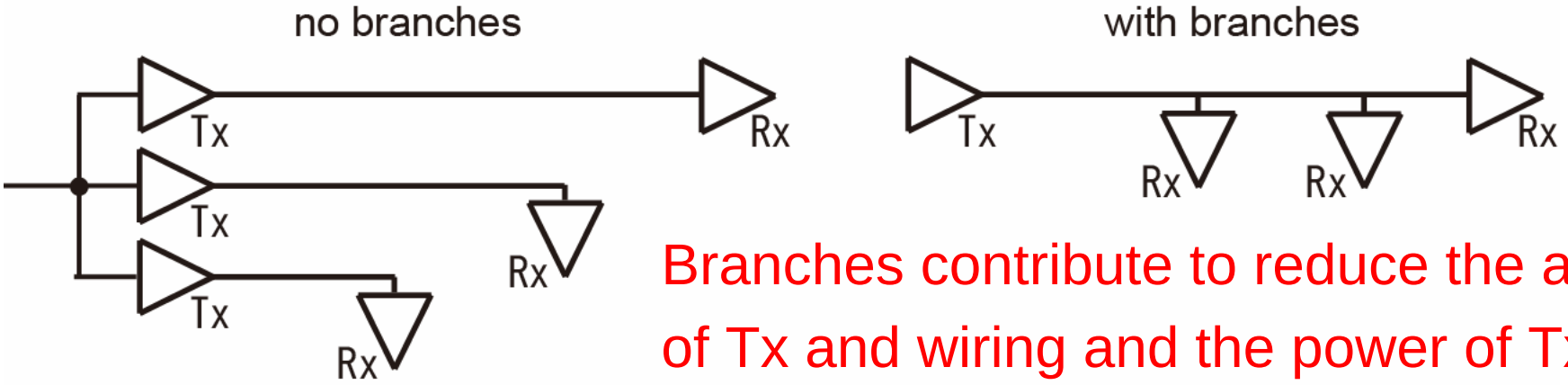
Delay & Power consumption:
The enduring obstacles

Transmission Line Interconnect

- Signals can propagate at near speed-of-light.
- The conventional on-chip TL interconnects are peer-to-peer ones.

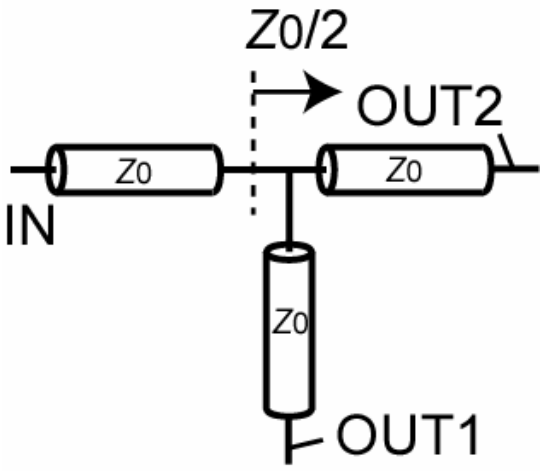
We propose the on-chip TL interconnect with branches.

2. Branching structure



Branches contribute to reduce the area of Tx and wiring and the power of Tx.

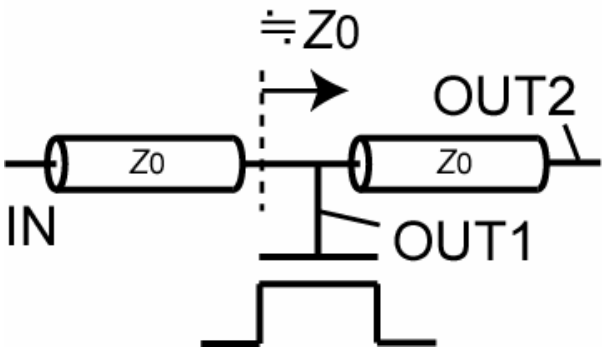
A brute-force branch



Impedance mismatch causes reflection.

Used branching structure

※Z0: Characteristic impedance



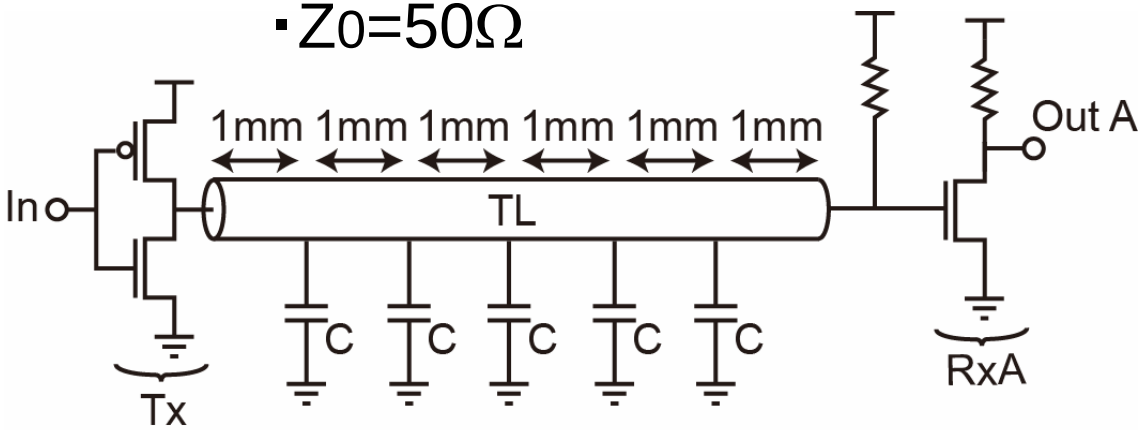
Z0 is hardly changed by branching.

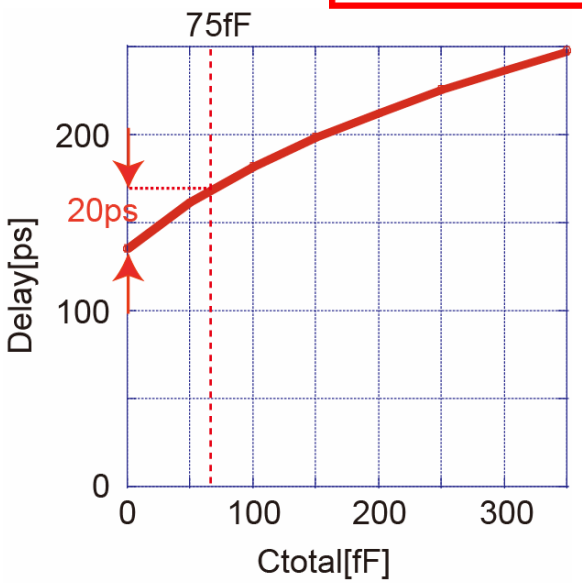
3. Test circuit for branches

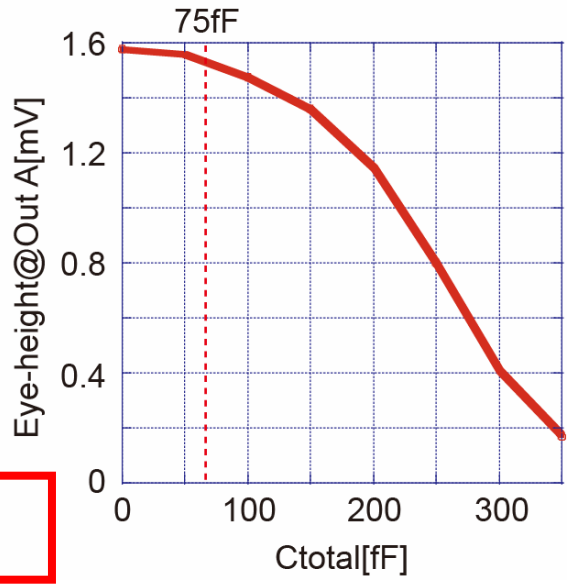
8Gbps

Transistors at branching nodes are modeled as capacitors.

- 0.18μm CMOS process
- Line width: 2.4μm
- Z_0=50Ω





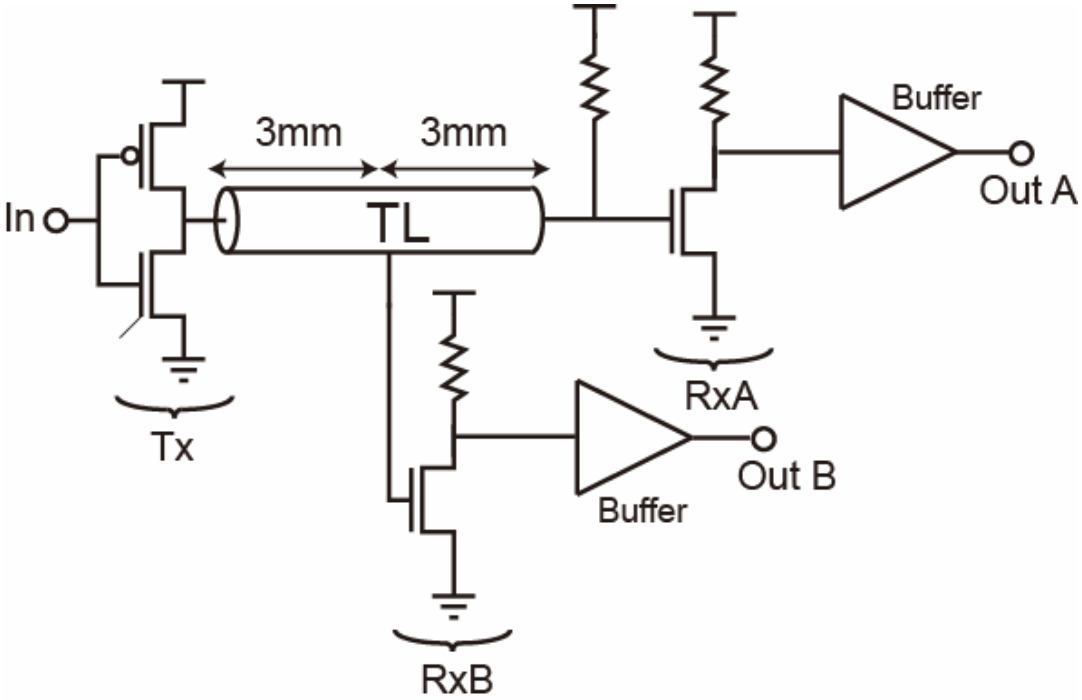


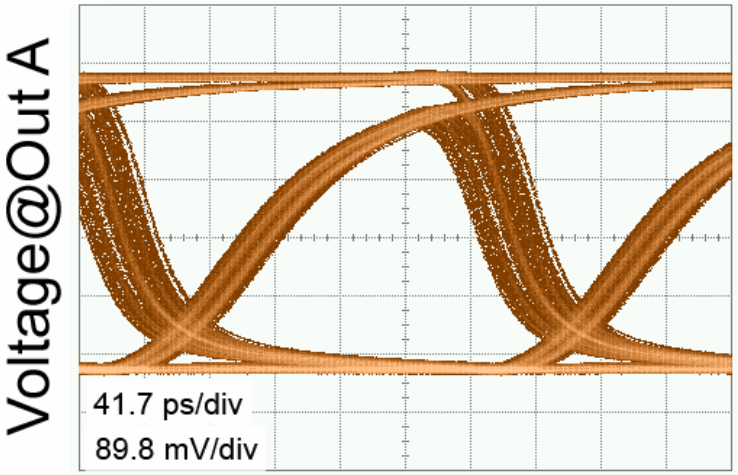
- Assumption ; Acceptable degradation of eye-height is 5%.

→75fF can be connected to the single-ended transmission line.

C_{total}=5C

4. Measurement results





Eye-pattern(4Gbps)

Simulated results

	Delay [ps/cm]	Power[mW] @4Gbps
The proposed (with a branch)	144	6.3
RC line[1] (no branches)	500	15

The proposed interconnect achieves the lowest power and delay although it has a branch.

[1] R. T. Chang , et al., Proc. IEEE JSSC, vol. 38, no. 5, pp. 834-838, 2003

5. Conclusion

- We have proposed an on-chip transmission-line interconnect with branches.
- In the measurement result, the proposed interconnect realizes 4Gbps signal transmission.
- Transmission line interconnects can improve delay and power of a branching global-interconnect as well as a peer-to-peer interconnect, which will contribute speeding-up and power saving of LSI.