A 90nm 8x16 FPGA Enhancing Speed and Yield Utilizing Within-Die Variations

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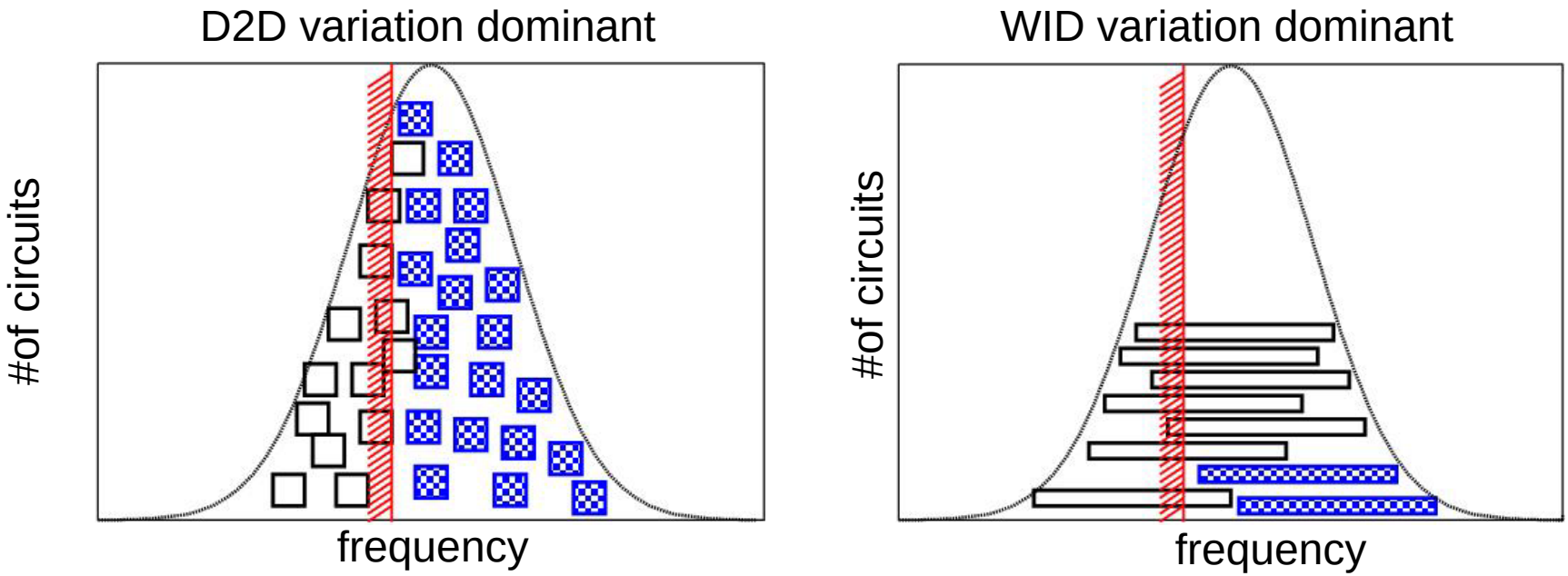
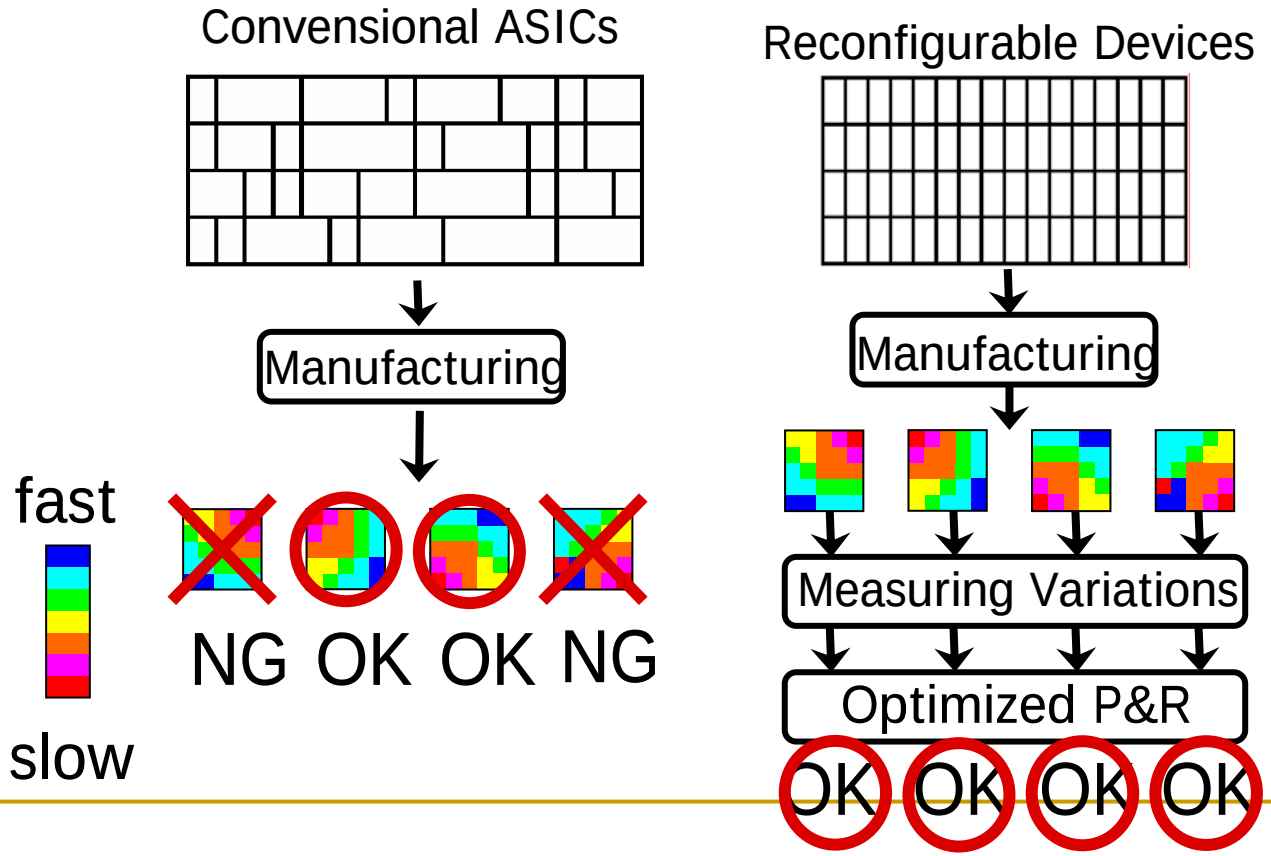
Research Background

- Within-Die (WID) Variations
  - Variations are getting more serious as process scaling.
  - WID variations are dominant in the sub-100nm regime.
  - WID variations causes the drastic yield losses.



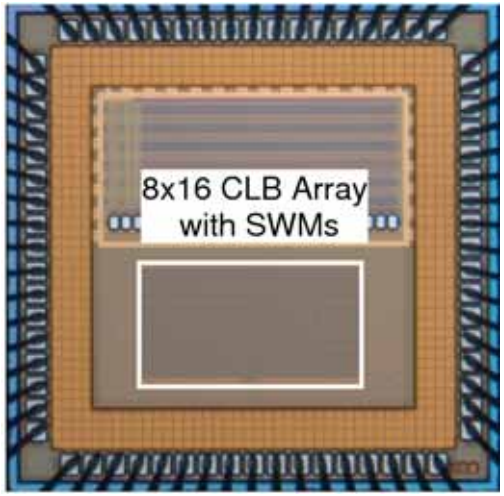
Proposed Method

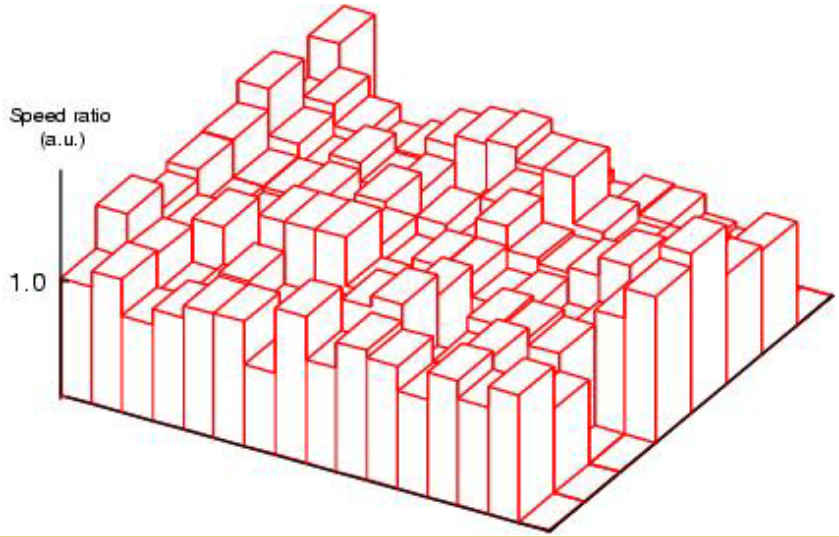
- Variation-Aware Reconfiguration
  - Reconfigurable devices can utilize the WID variations by reconfiguration



An FPGA Device For Variation-Aware Performance Optimization

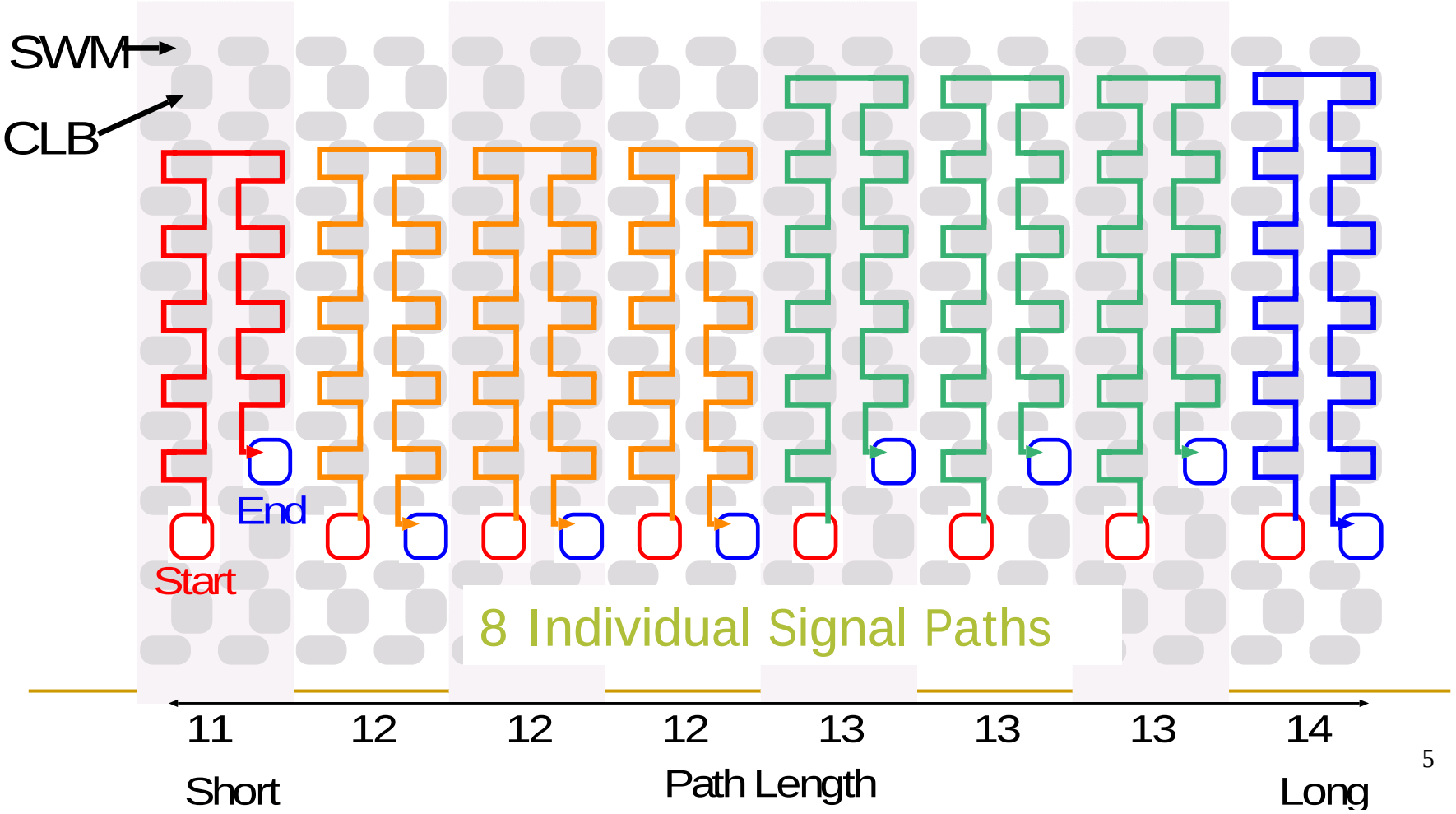
- We fabricate FPGA which can measeure WID variations in a 90nm process.
- WID variations are measured as # of oscillations by implementing a ring oscillator



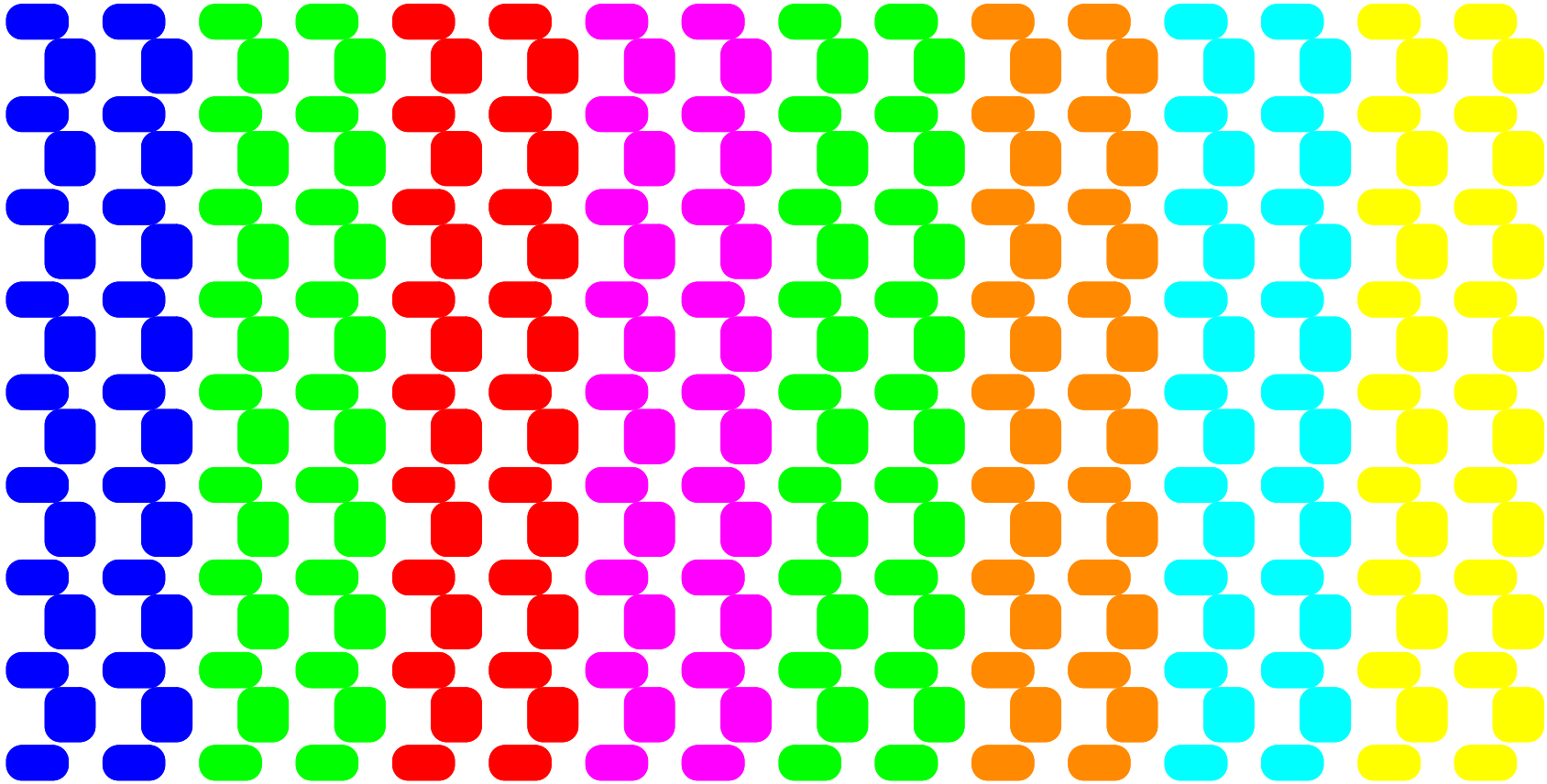


Variation-Aware Reconfiguration

- Implement a test circuit to evaluate the speed and yield enhancement
  - Paths are rearranged using the measured WID variations

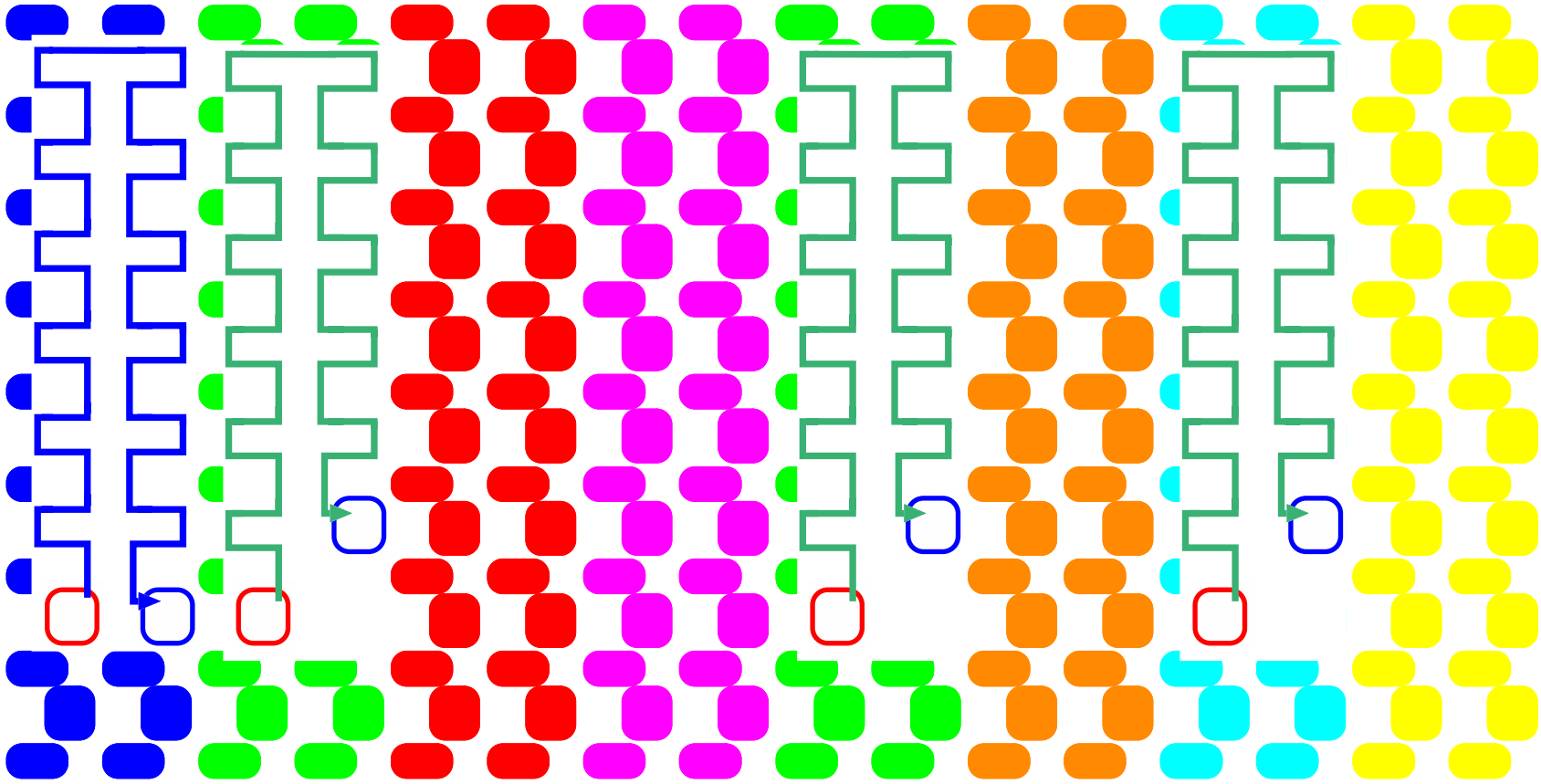


Variation-aware Reconfiguration(2)



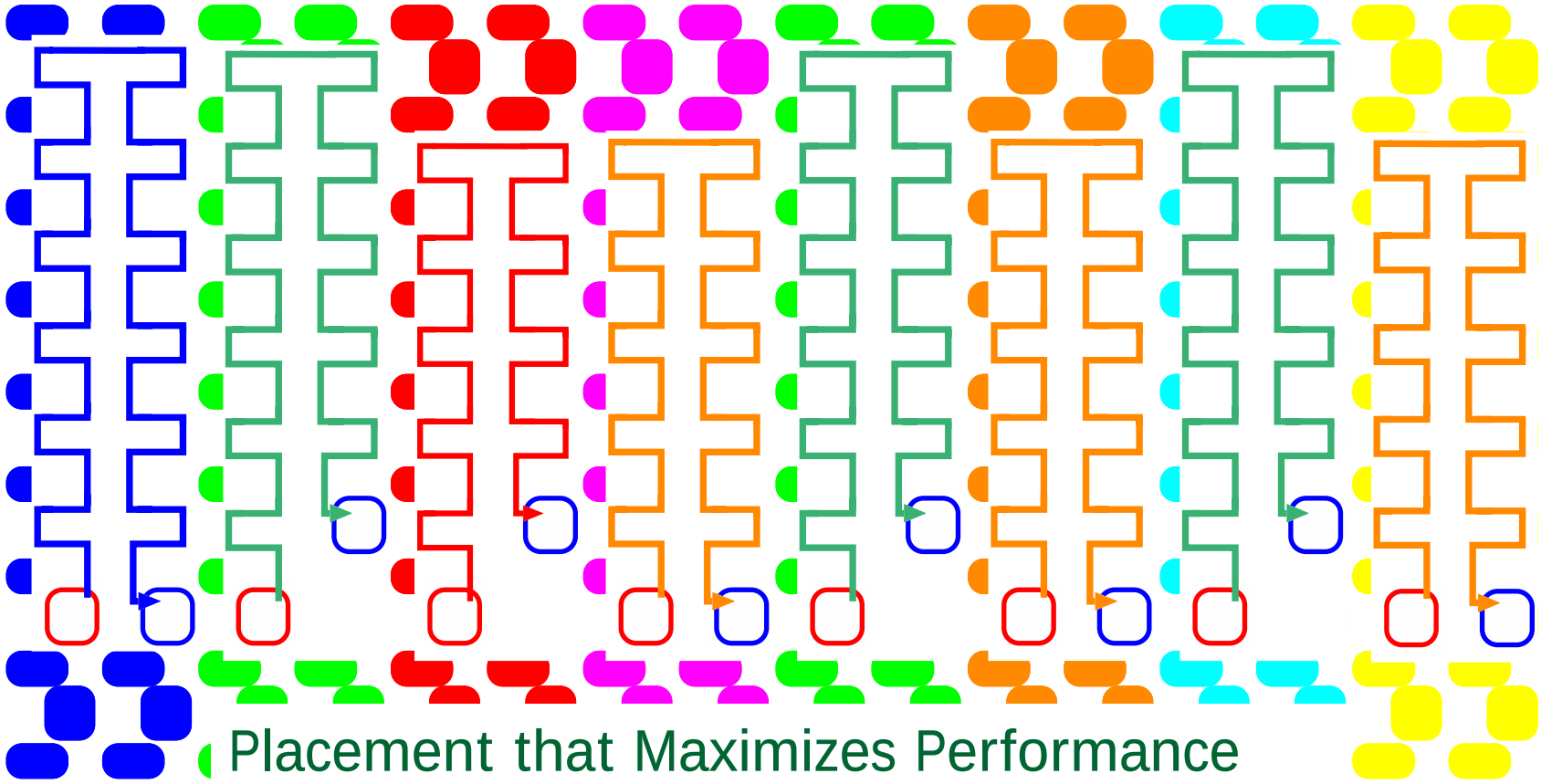
Measured Performance

Variation-aware Reconfiguration(2)



Measured Performance

Variation-aware Reconfiguration(2)



Placement that Maximizes Performance (Best-Case)

Measured Performance

Fast Slow

Results

- Speed enhancement (Fig (a))
  - Operating speed becomes faster in every chip
  - 4.1% speed enhancement in average
- Yield enhancement (Fig (b))
  - The best placement has the 32% better yield than the worst one at the performance ratio=0.98

Fig (a)

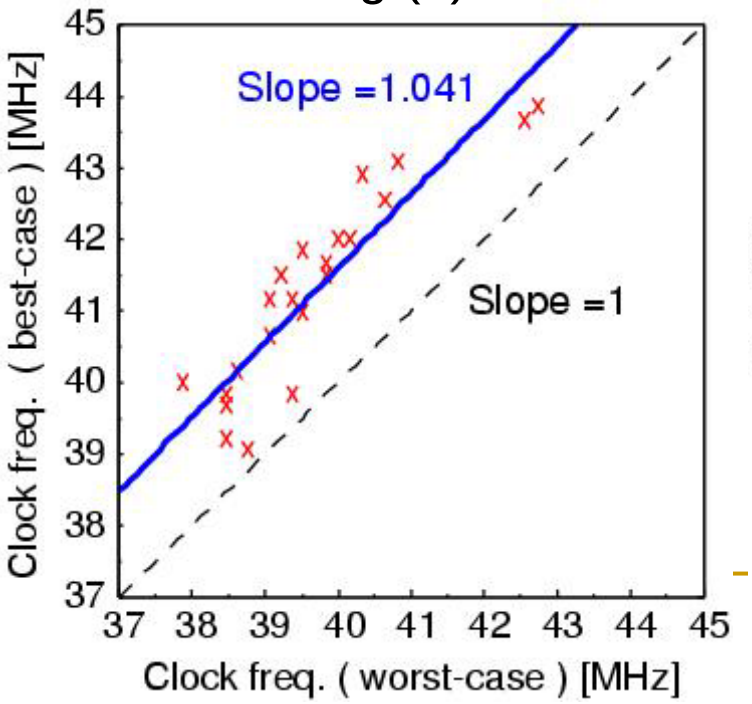


Fig (b)