A 0.35um CMOS 1,632-gate count Zero-Overhead Dynamic Optically Reconfigurable Gate Array VLSI

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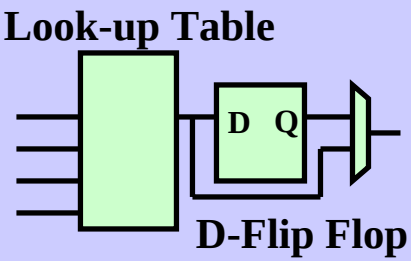
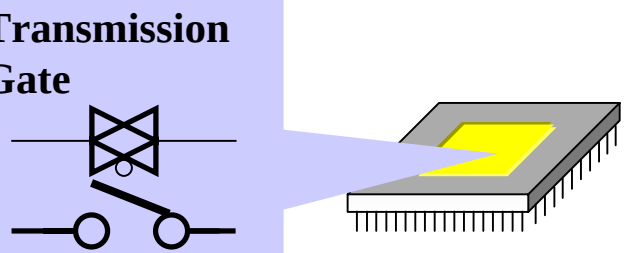
Dynamic Reconfiguration Advantage

Drawback of Conventional Programmable Devices

LUT structure

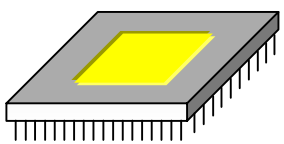


SM structure



Drawback is based on LUT and transmission gate structure

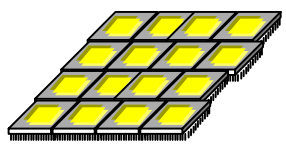
Conventional Implementation



Multi-Functions Unit
or General purpose Unit

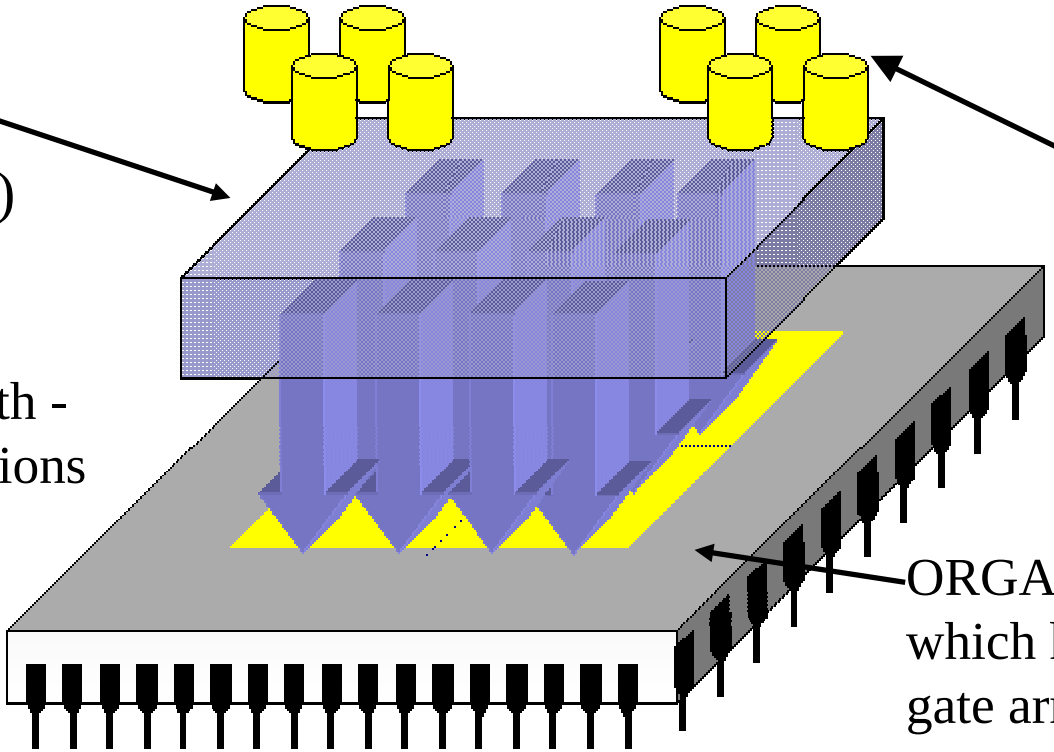
Dynamic reconfiguration Implementation

Single Function Unit



Parallel computation

Overview of optically reconfigurable gate array



Holographic Memory (virtual gates)

Laser Diodes Array

Large bandwidth - optical connections

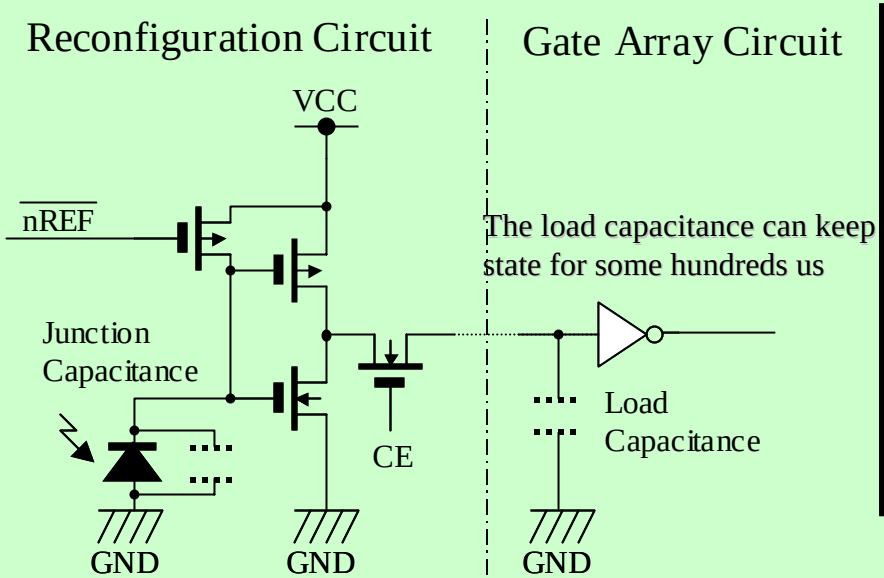
ORGA- VLSI (real gates) which has a programmable gate array with photodiodes

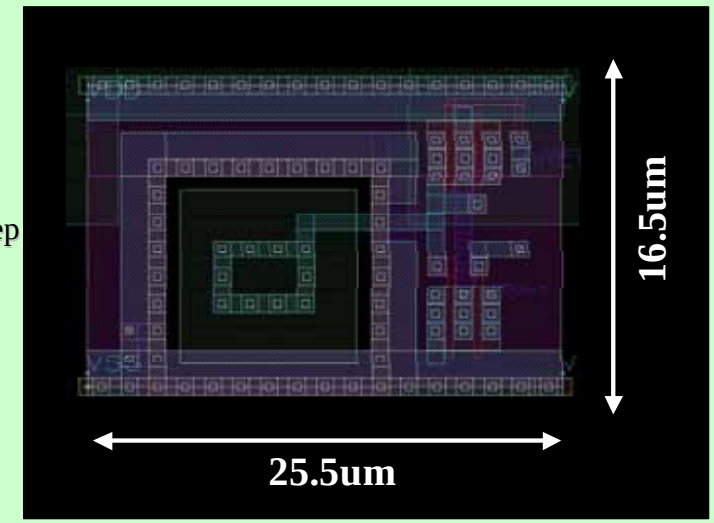
Holographic Memory

1) According to the latest paper, multi-layered wave-guide holographic memory can store 15.5Gbit in 0.23 cubic centimeter. (Appl. Opt., Vol. 42, No. 35, 7085 – 7092, 2003). The memory amount corresponds to 4G gate count program.

2) According to the prospect of a future holographic memory, one cubic centimeter holographic memory will store 1 terabit , corresponding to about 250 billion gate count.

Improved Dynamic Optical Reconfiguration Circuit



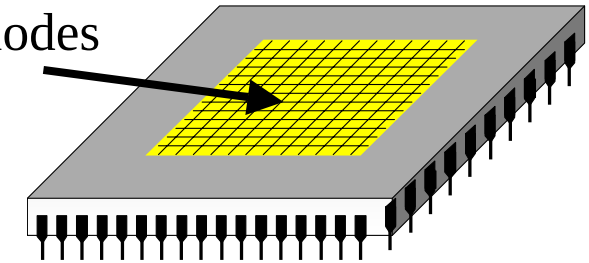


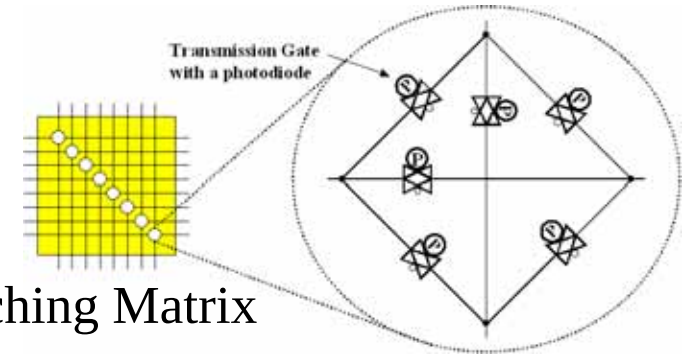
CAD Layout of PD Cell

- New circuit consists of a DORC and a pass transistor.
- The pass transistor is used for blocking off the connection between reconfiguration circuit and gate array circuit.
  The load capacitance is used for keeping the gate array state.
- The load capacitance is sufficient to maintain the state of gate array while reconfiguring.

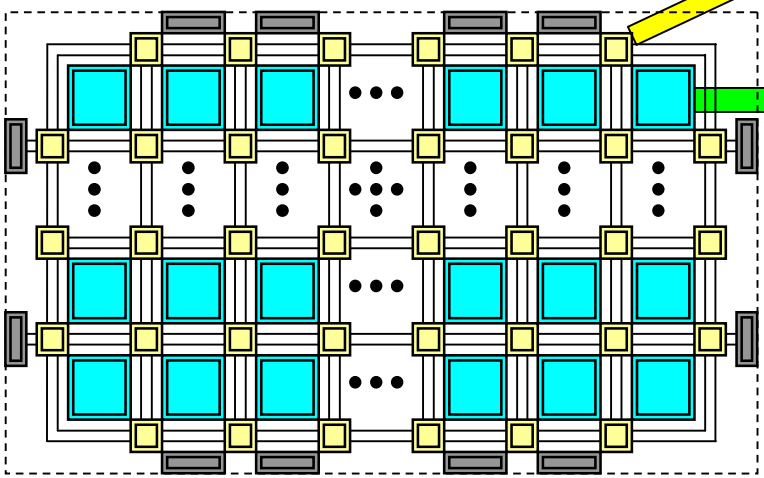
Gate Array Design

Photodiodes

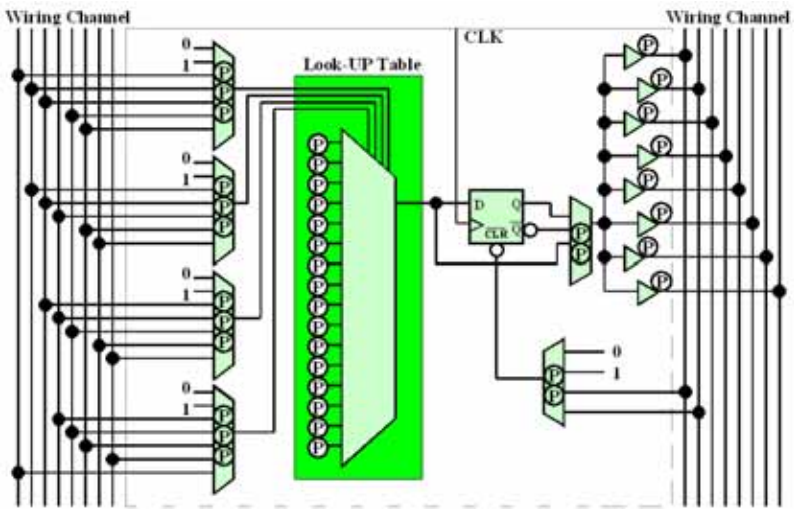




Switching Matrix



Island-Style Gate Array



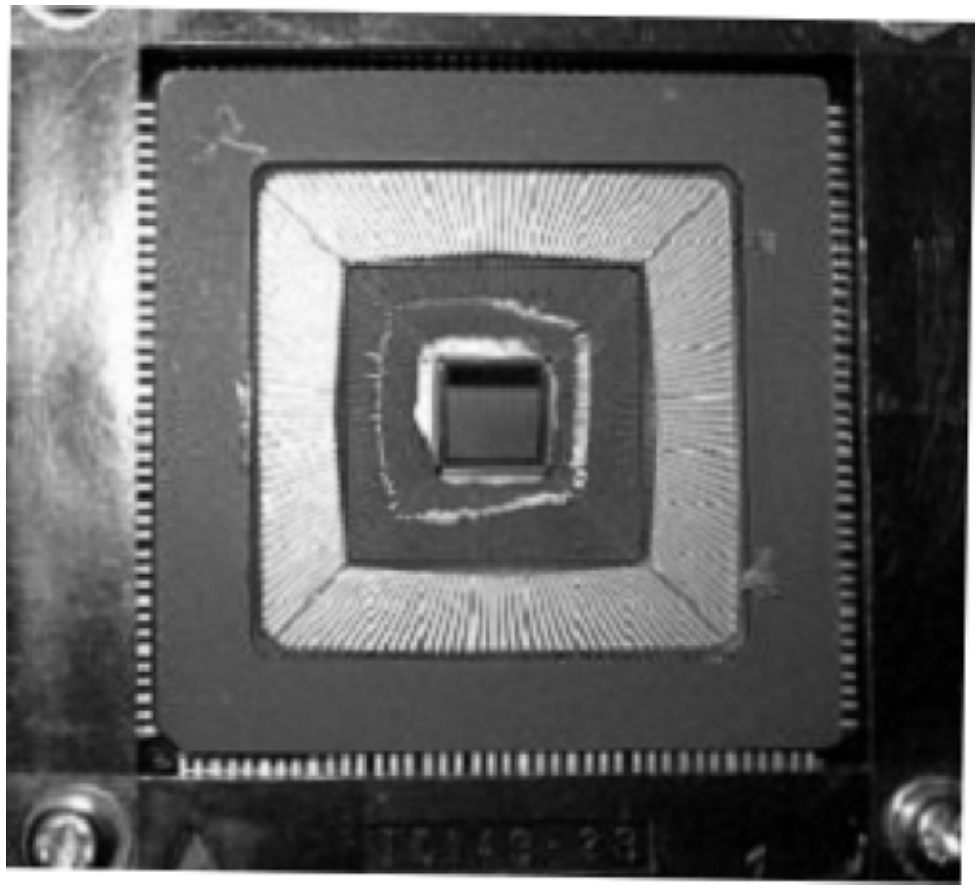
Logic Block

An ORGA takes Island-Style gate array. The basic structure is same as that of current FPGAs. However, each programming element of the gate array is connected to a photodiode. Thereby, all state of the gate array can be programmed in perfectly parallel.

1,632 gate count ZO-DORGA-VLSI

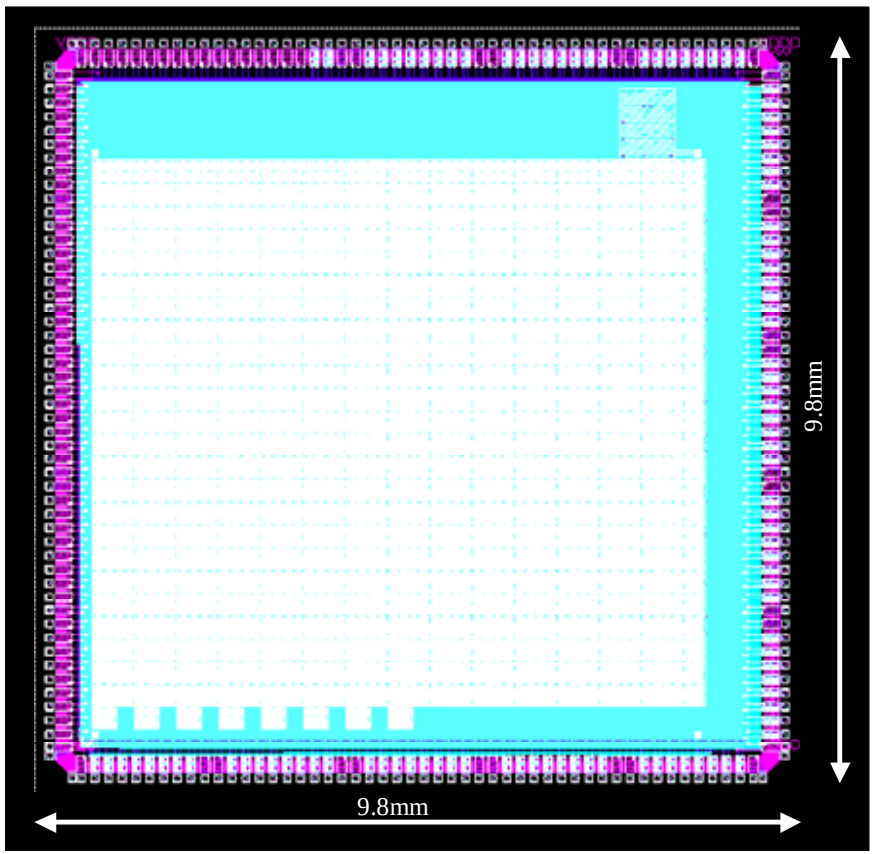
Specification of a DORGA-VLSI

Technology	0.35 μm double-poly triple-metal CMOS process
Chip size	4.9 $\times$ 4.9 [mm]
Supply Voltage	Core 3.3V, I/O 3.3V
Photodiode size	9.5 $\times$ 8.8 [μm]
Horizontal Distance between Photodiodes	34.5 [μm]
Vertical Distance betweenPhotodiodes	33.0 [μm]
Number of Photodiodes	6,213
Av. Aperture Ratio	4.24%
Number of Logic Blocks	48
Number of Switching Matrices	63
Number of Wires in a Routing Channel	8
Number of I/O bits	24
Gate Count	1,632



Photograph of a DORGA-VLSI

Design of a future high density DORGA



CAD Layout of a ZO-ORGA

Specifications of a ZO-ORGA

Technology	0.35 μm 3-metal CMOS process
Chip size	9.8×9.8 [mm²]
Photodiode size	9.5×8.8 [μm²]
Horizontal distance between photodiodes	34.5 [μm]
Vertical distance between photodiodes	33.0 [μm]
Number of Photodiodes	38,591
Number of Logic Blocks	336
Number of Switching Matrices	375
Number of I/O Blocks	8 (32bit)
Wiring channel	8
Gate Count	11,424 gates

Conclusion

・This presentation presents

(a) the design of a fabricated world's largest 1,632 gate count ZO-DORGA-VLSI,

(b) an over 10,000 gate count VLSI by using 9.8mm square CMOS process chip and same logic blocks and switching matrices.

Acknowledgments

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