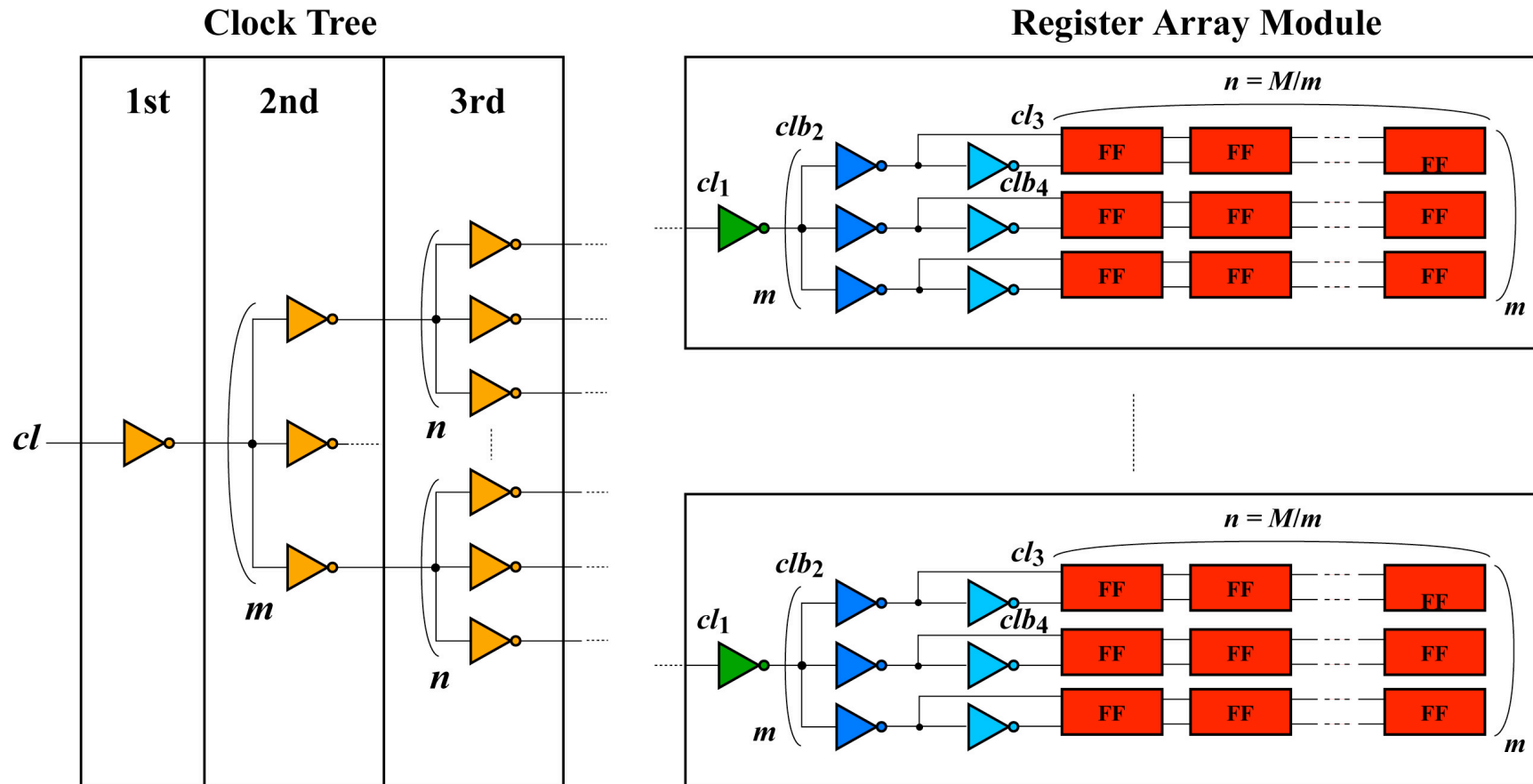# Low-Power High-Speed 90-nm CMOS Clock Drivers
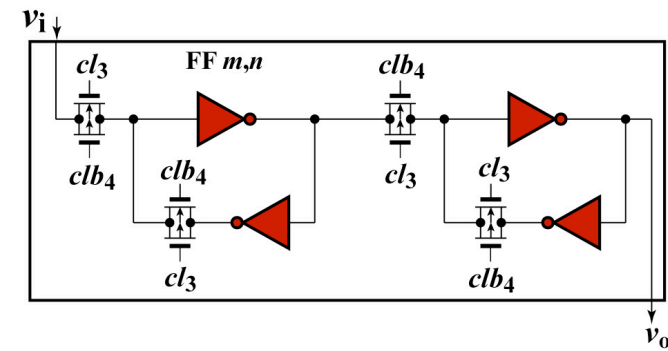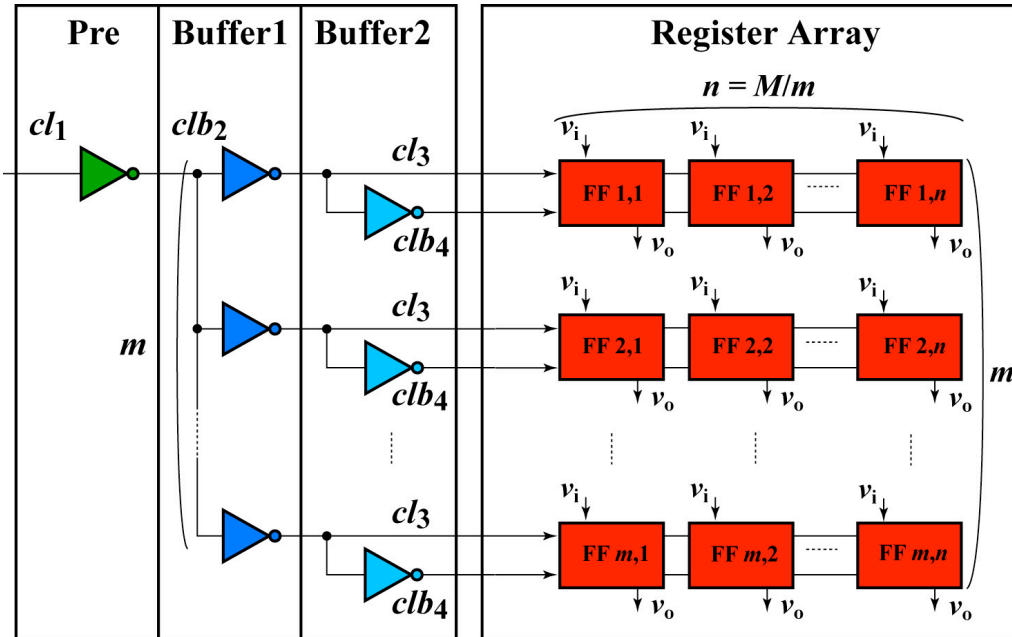
T. Enomoto, S. Nagayama and N. Kobayashi
Chuo University, Tokyo, Japan
ASP-DAC'2007, Yokohama, Japan, Jan. 24, 2007

Register Array Modules

Technology: 90-nm, Triple-Well, 6-Layer, Cu, CMOS

Gate Lengths: $L_n = L_p = 0.1$ mm

Channel Widths (Logic): $W_n = 1.08$ µW, $W_p = 1.64$ µW

Channel Widths (Swich): $W_n = 0.54$ µW, $W_p = 0.82$ µW

Threshold Voltages: $V_{tn} = 0.222$ V, $V_{tp} = -0.241$ V

No. of D-FF ($M = m \times n$) = 40

m	$n = M/m$
1	40
5	8
8	5
10	4
20	2
40	1

Power Dissipation and Signal Propagation Delay of a Single Logic Gate

Power due to dynamic current

$$p_D(n) = (An+B) \cdot V_D^2 \cdot f$$
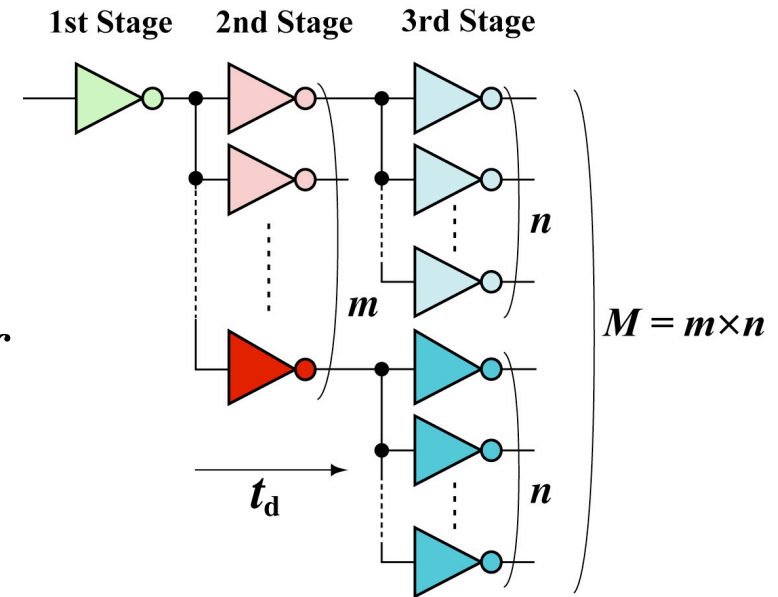
Power due to short-circuit current

$$p_S(m, n) = \frac{E(m+F)^G \cdot (V_D - 2V_T)^3 \cdot f}{(1+Hn)^J}$$

Signal Propagation Delay

$$t_d \approx \frac{(C_m + C_n)V_D^2}{\frac{\beta}{2}(V_D - V_{th})^2} \approx \frac{2(C_m + C_n)}{\beta(V_D - V_{th})}$$

$$\propto (Am + B) + (An + B) = A(m + n) + 2B$$

$$= A(m + \frac{M}{m}) + 2B$$

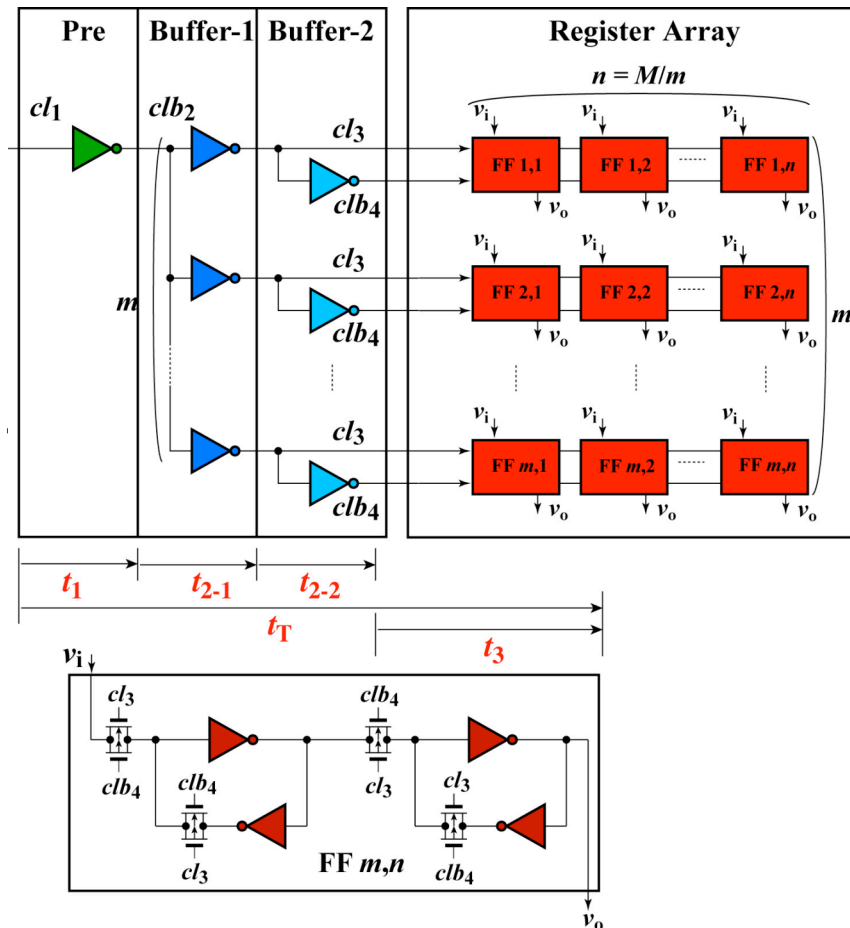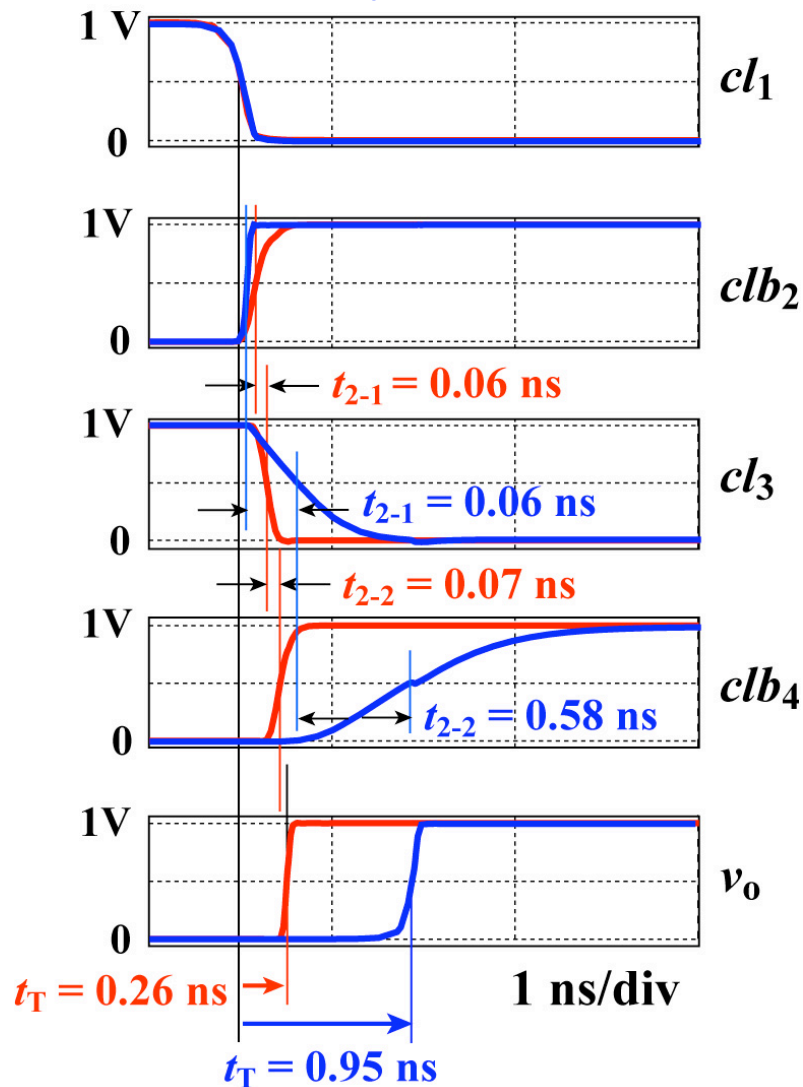$M = m \times n$

at $m = 1$ & $m = M$
$$t_d \propto A(M+1) + 2B$$

at $m = n$
$$t_d \propto 2AM^{0.5} + 2B$$

Signal Propagation Delay of 90-nm Register Array Modules (SPICE Simulation)
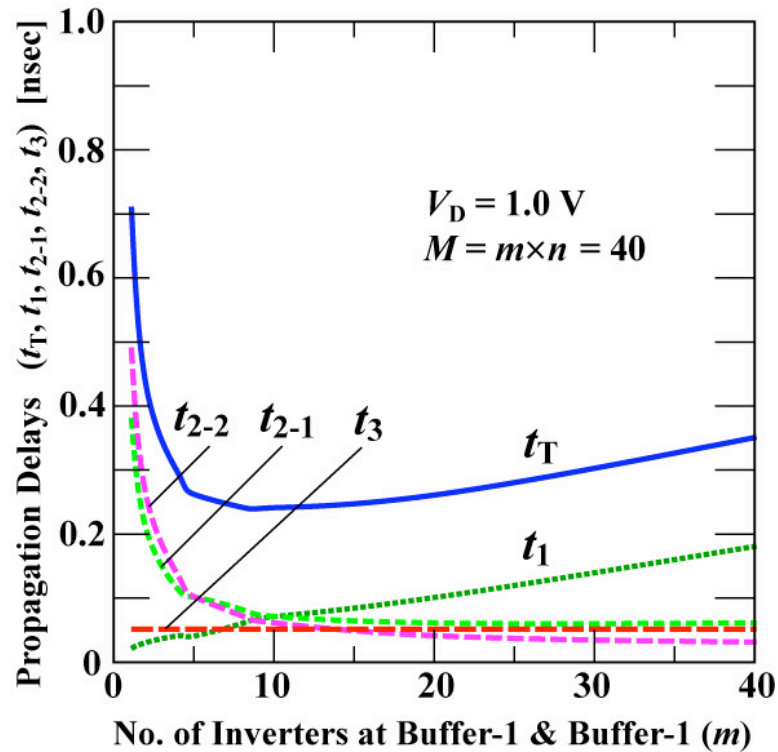
Signal Propagation Delay of 90-nm
Register Array Modules
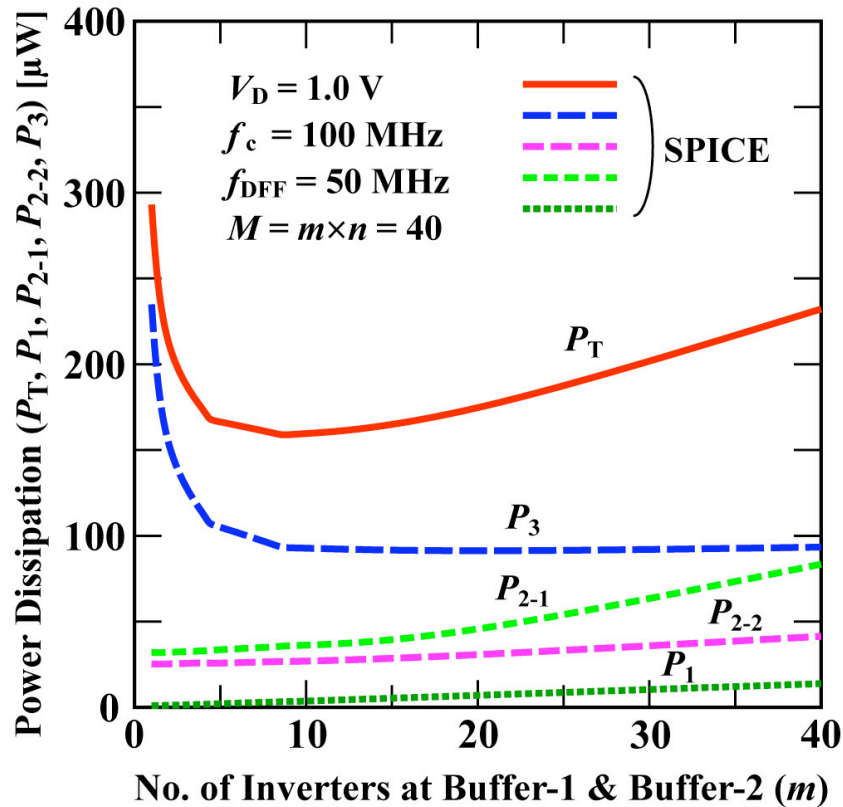## (SPICE Simulation)
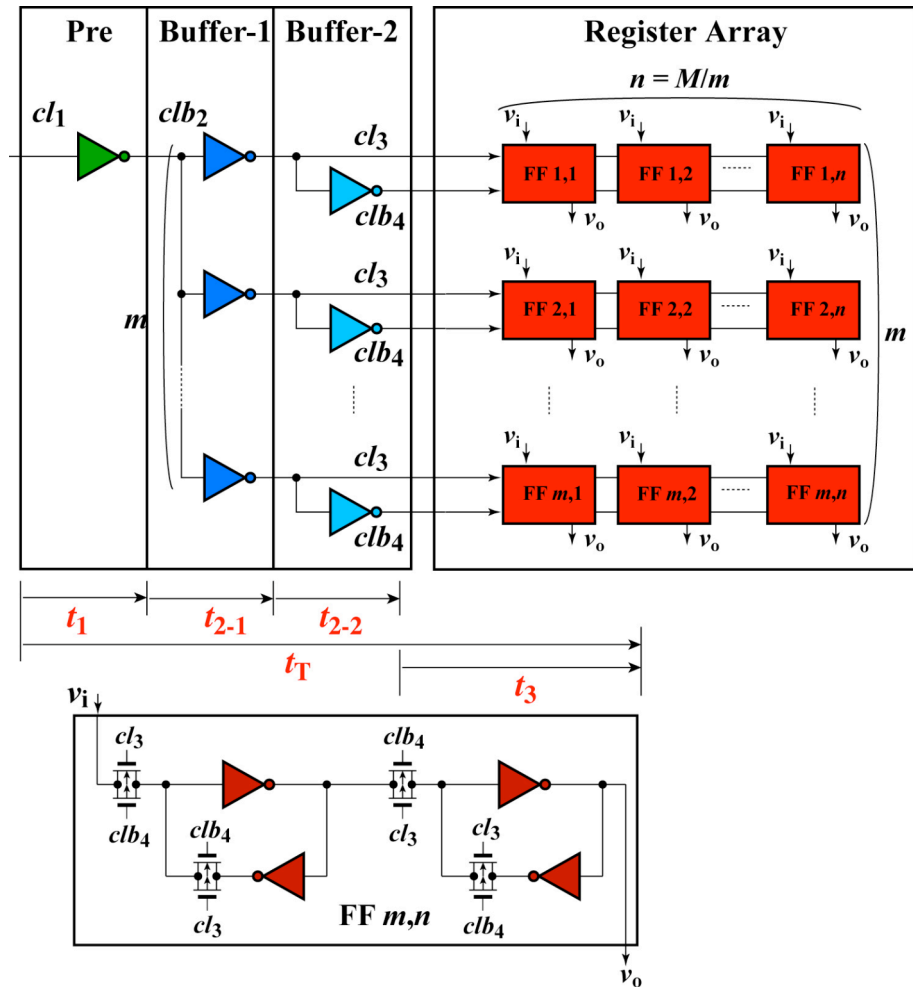
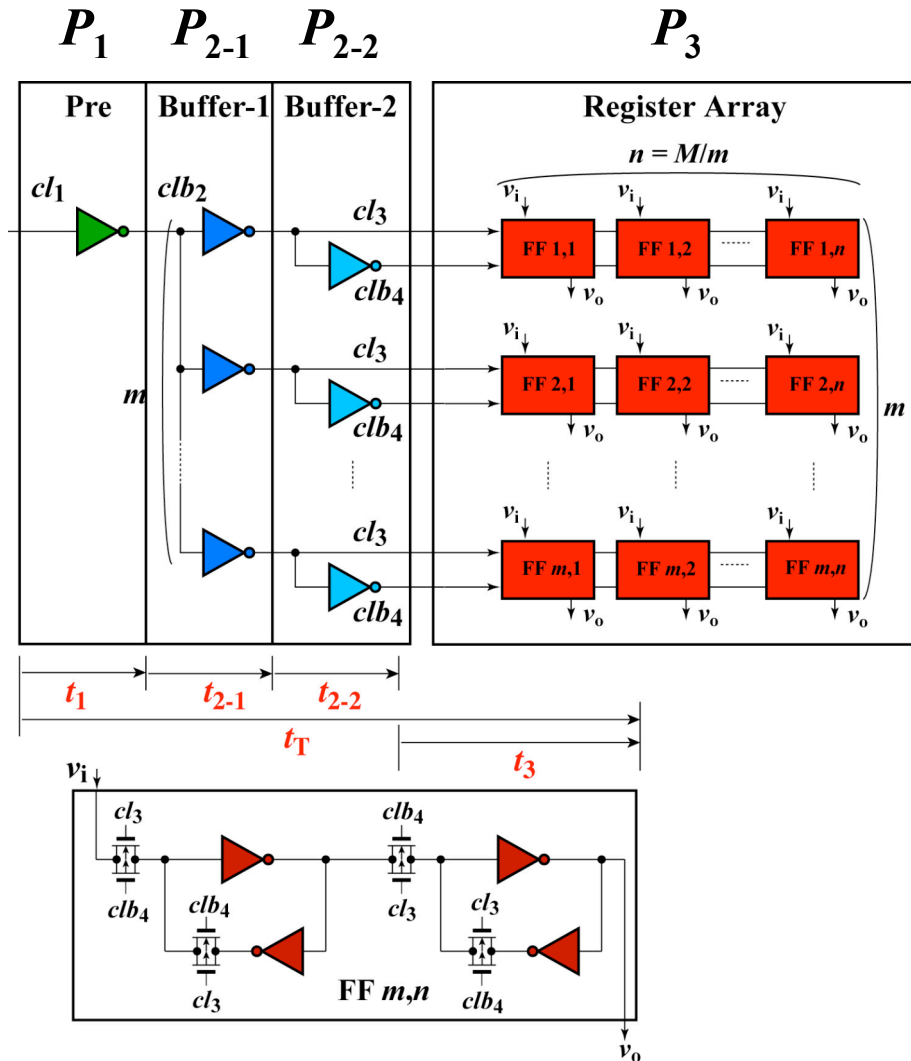# Signal Propagation Delay (t_T) & Optimized m for Minimum t_T of 90-nm Register Array Modules
(SPICE Simulation)
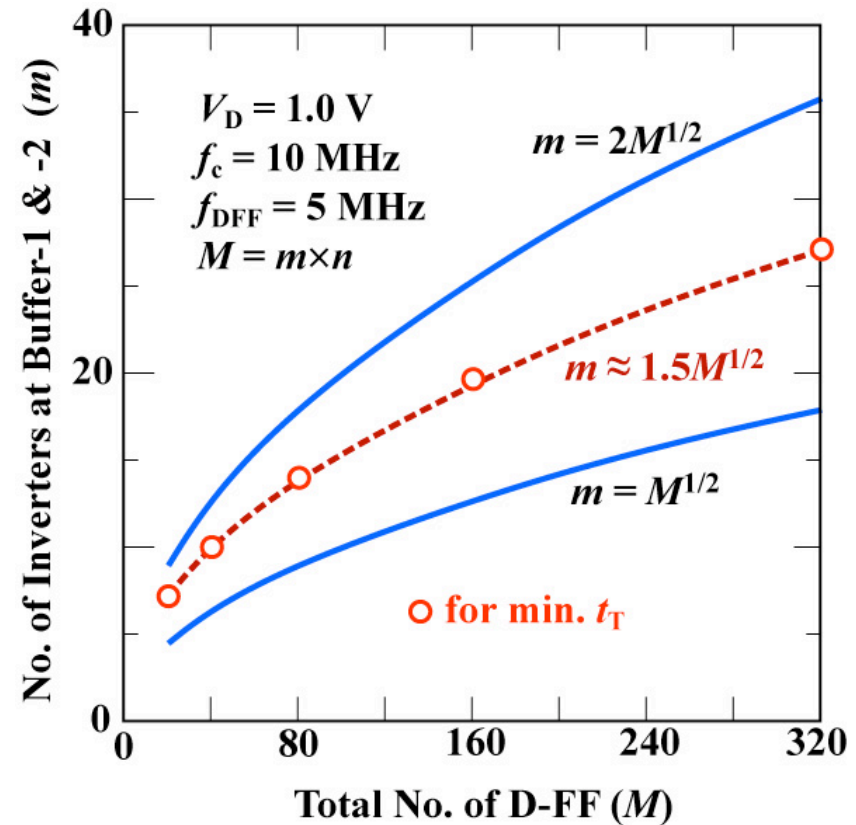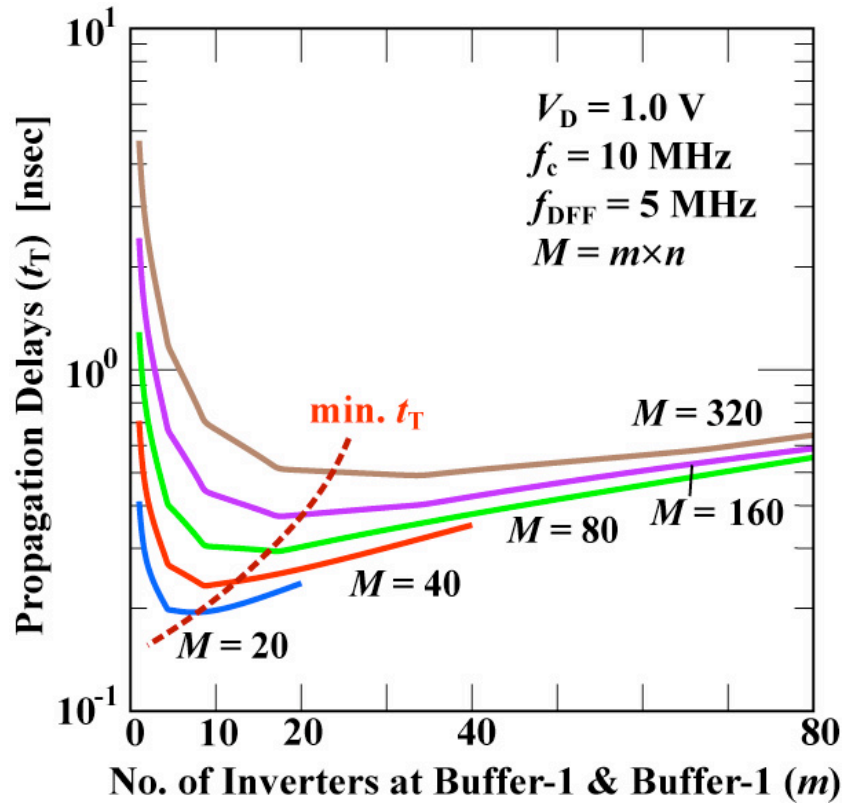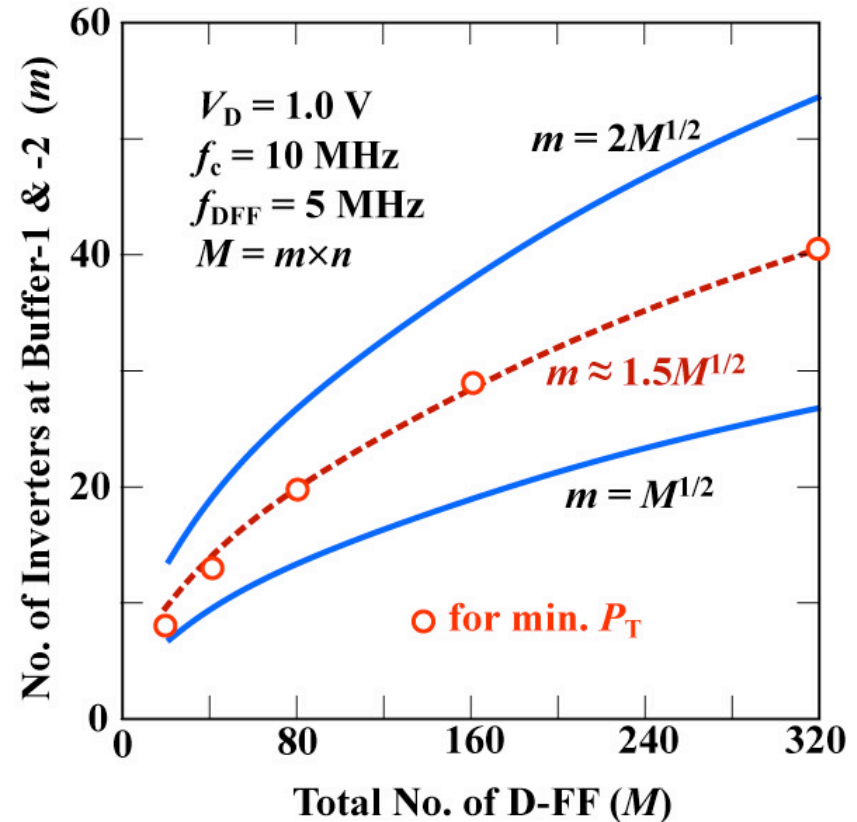

t_T is minimized at $m \approx 1.5M^{1/2}$
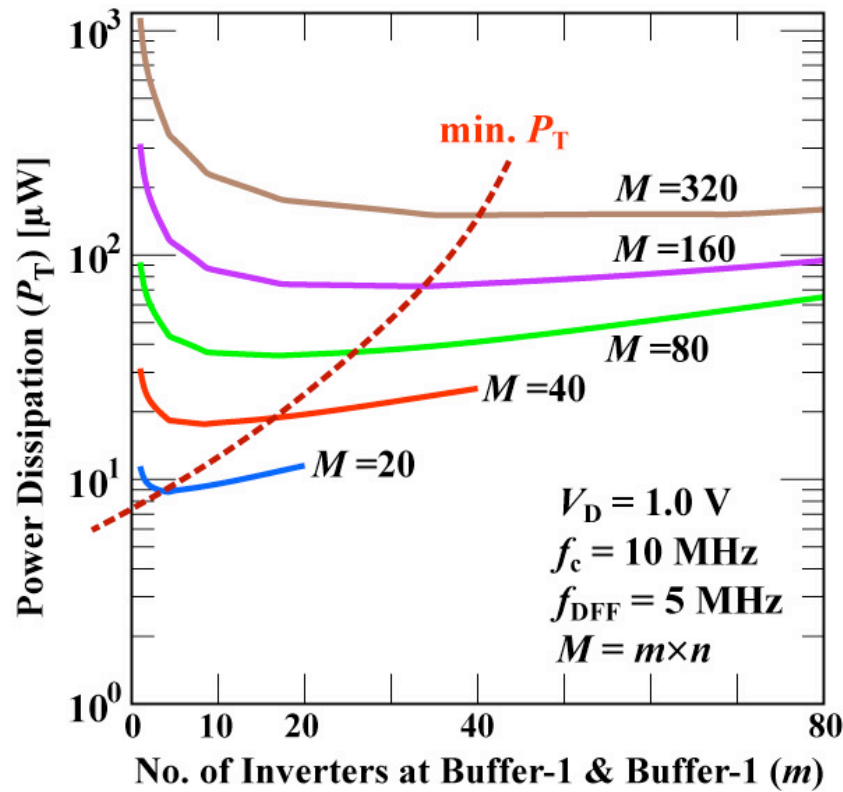
Power Dissipation of 90-nm Register Array Modules
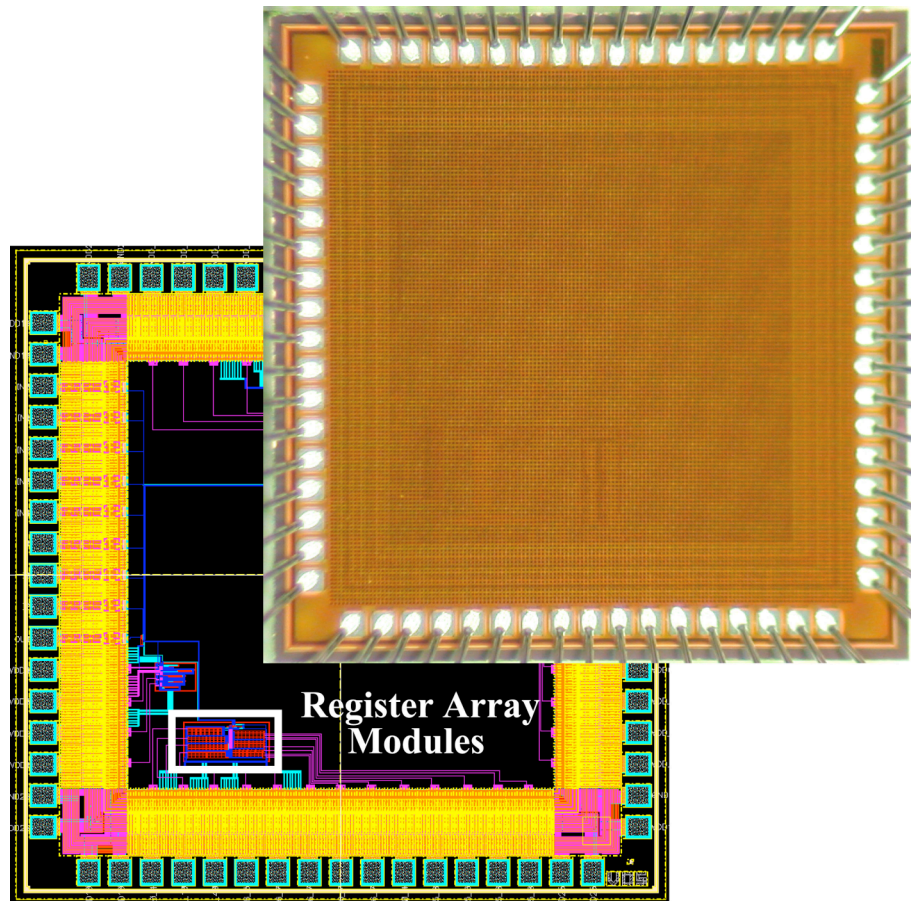## (SPICE Simulation)

Power Dissipation (P_T) & Optimized *m* for Minimum P_T of 90-nm Register Array Modules
(SPICE Simulation)

P_T **is minimized at**
$m \approx 1.5 M^{1/2}$

90-nm CMOS LSI Chip with 6 Register Array Modules

Technology:
  90-nm,Triple-Well,
  6-Layer, Cu, CMOS
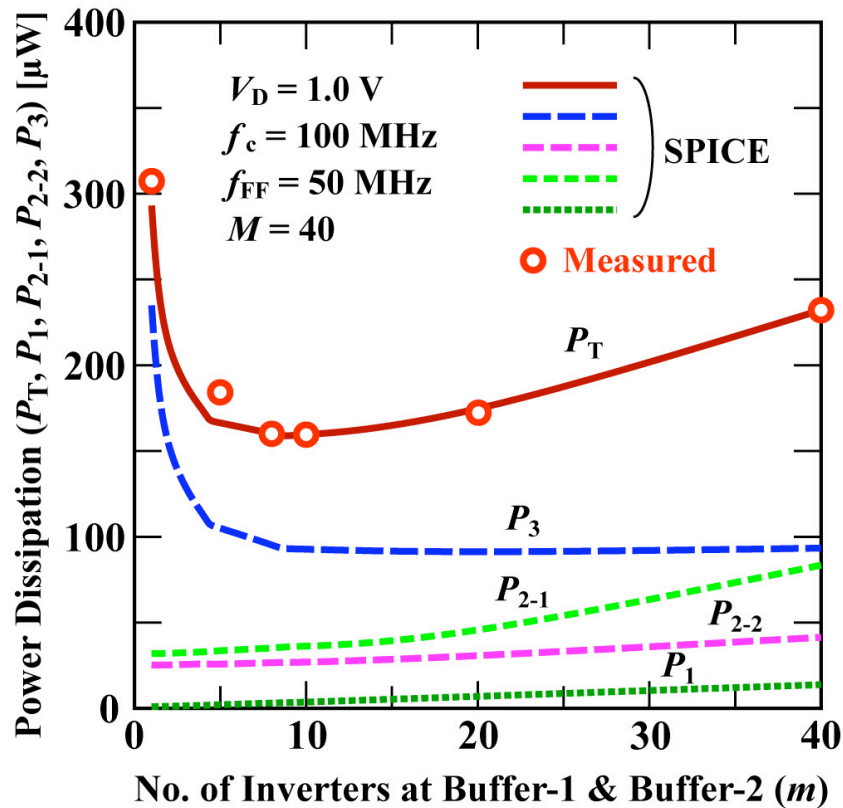Chip Size:
  2.5 mm × 2.5 mm

No. of D-FF ($M = m \times n$) = 40

m	$n = M/m$
1	40
5	8
8	5
10	4
20	2
40	1

Register Array Modules

Power Dissipation of 90-nm Register Array Modules
(Experimental Results)

No. of D-FF ($M = m \times n$) = 40

- **Signal Propagation Delay (t_T)**
  0.95 nsec ($m = 1$)

  0.26 nsec (27.4%) ($m = 10$)

- **Power Dissipation (P_T)**
  293.1 μW ($m = 1$)

  159.6 μW (54.5%) ($m = 10$)

t_T and P_T are minimized at
$m \approx 1.5M^{1/2}$