

Improving Execution Speed of FPGA using Dynamically Reconfigurable Technique

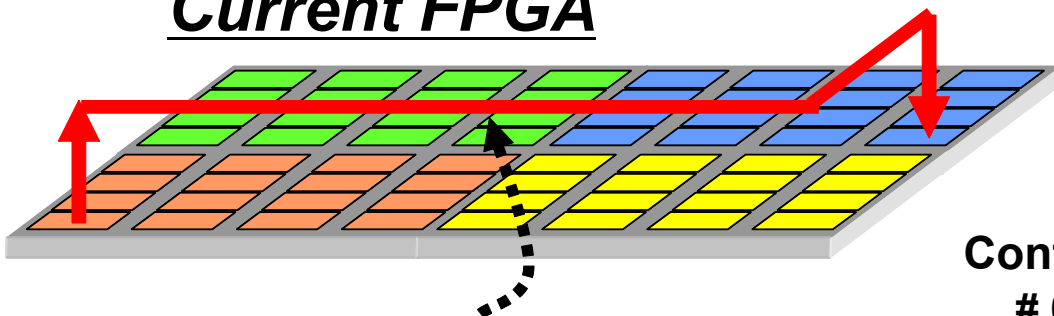
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Motivation of This Work

- To Reduce Interconnect Delay in FPGAs

Current FPGA



Longer Interconnection

*Shorter Interconnections +
Temporal Communication*

Dynamically Reconfigurable FPGA (DRFPGA)

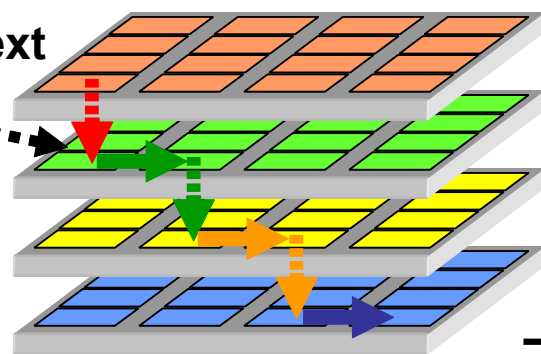
Context

0

1

2

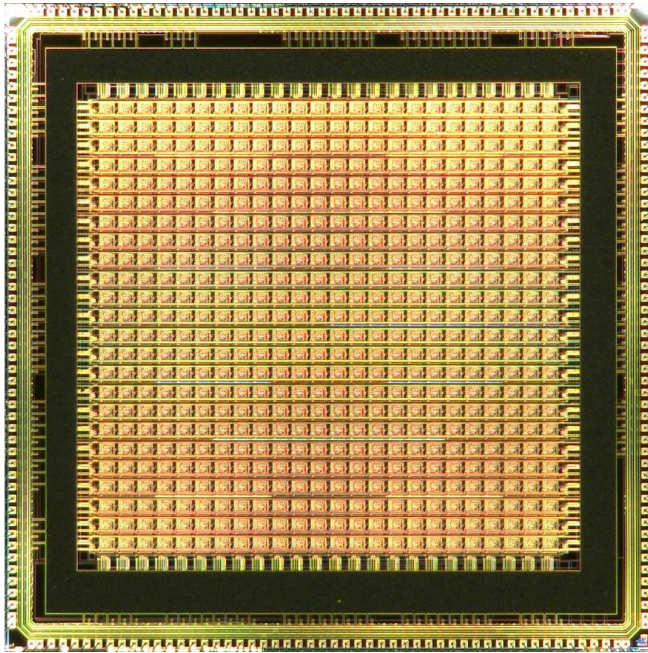
3



- In recent LSI manufacturing
Interconnect Delay \gg Gate Delay
- Long Interconnection \rightarrow Shorter Interconnections
via Temporal Communication

**Dynamic Reconfiguration can Reduce
Interconnect Delay in FPGAs!**

Dynamically Reconfigurable FPGA (FP-III) and its Design Automation Software (PELOC)



← 7.29mm →

FP-III chip die photo

0.35um CMOS 2P3M

4 Context Planes

24x24 Array of LE

Nearest Neighbor Architecture

Die Size: 9.86mm \square

A screenshot of the PELOC software interface. The main window displays a circuit diagram with various components and connections. Below the diagram is a configuration panel with several sections: 'Target circuit data' (Load target circuit, bcount4 circuit, 14 instances), 'EDA options' (Temporal partitioning options: Automatic, Fixed 1 (1-4), Number of LE based; Placing options: Simple, Maintain timeslot, Maintain timeslot spiral; Options: Enable Concurrent PR), and 'Progress' (Generate Configuration data, View log, Clear all logs, Close, Start EDA). A yellow box is overlaid on the interface with the text: Temporal Partitioning and Temporal Cost Reduction are supported.

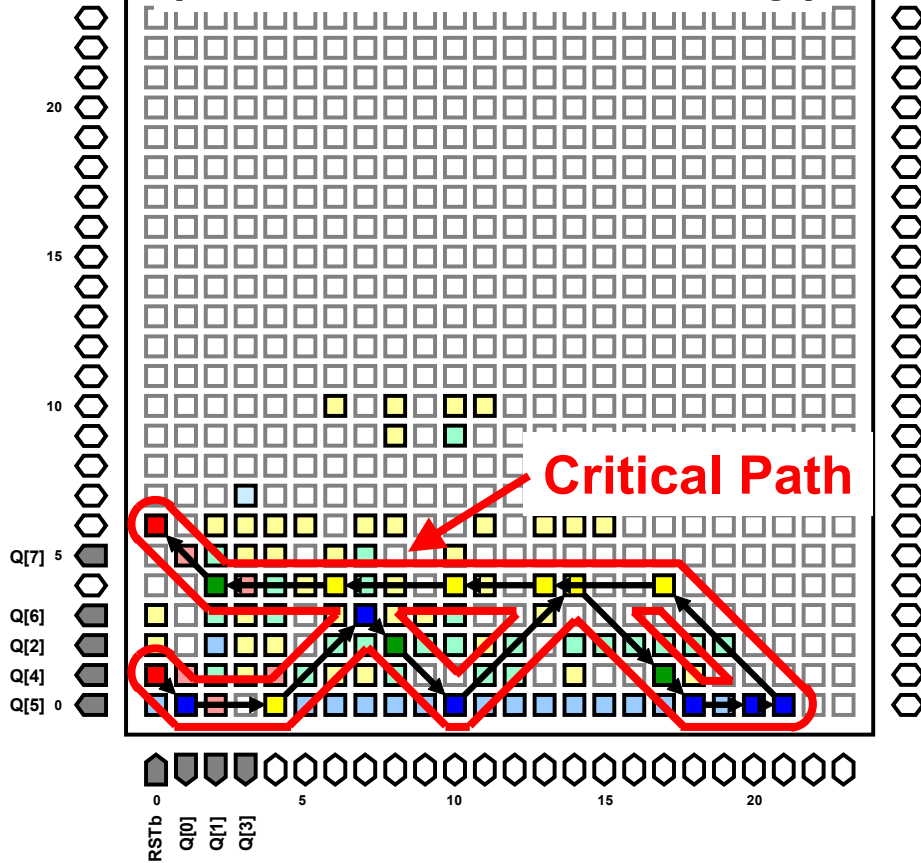
PELOC view

(Processor Element LOCator)

Placing & Routing Results

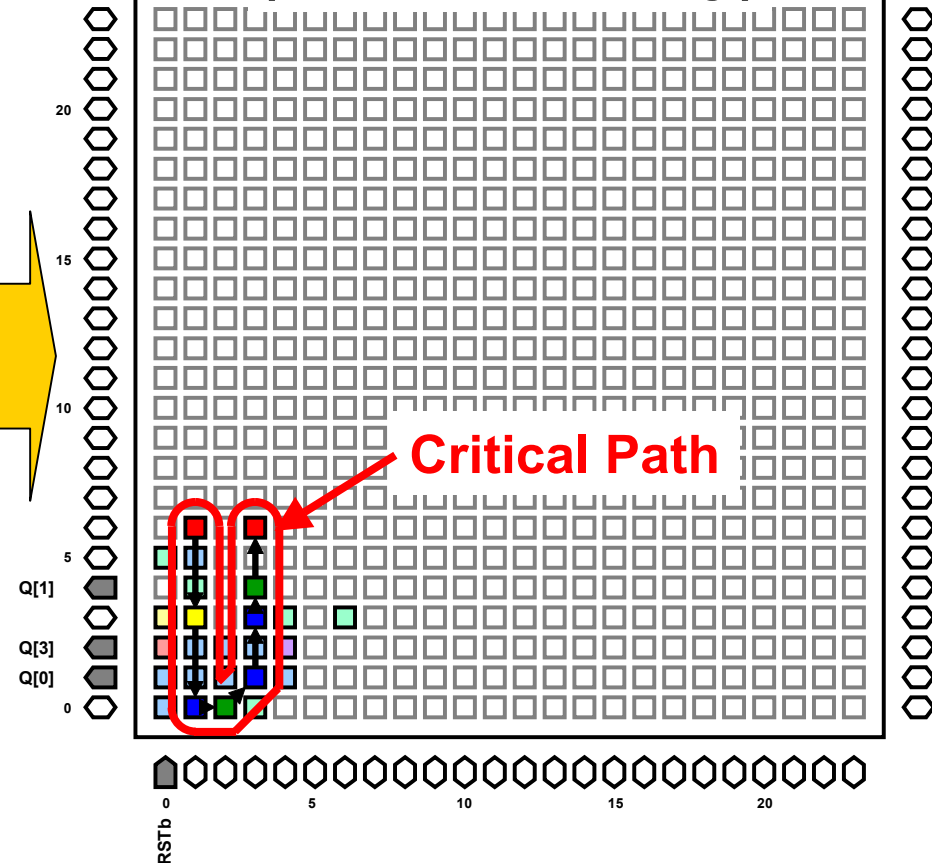
1 Context Used

(Current FPGA's way)



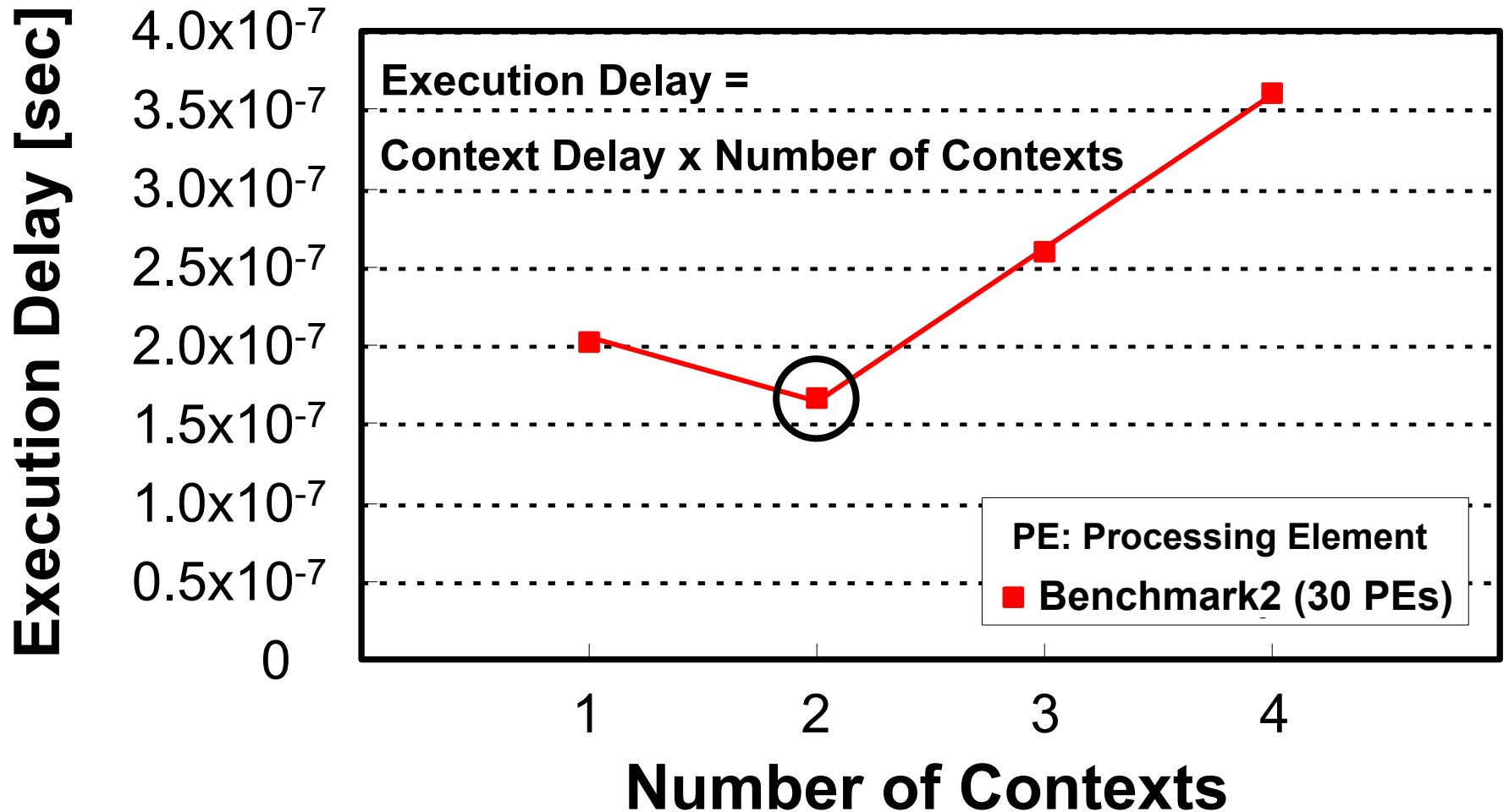
2 Contexts Used

(DRFPGA's way)



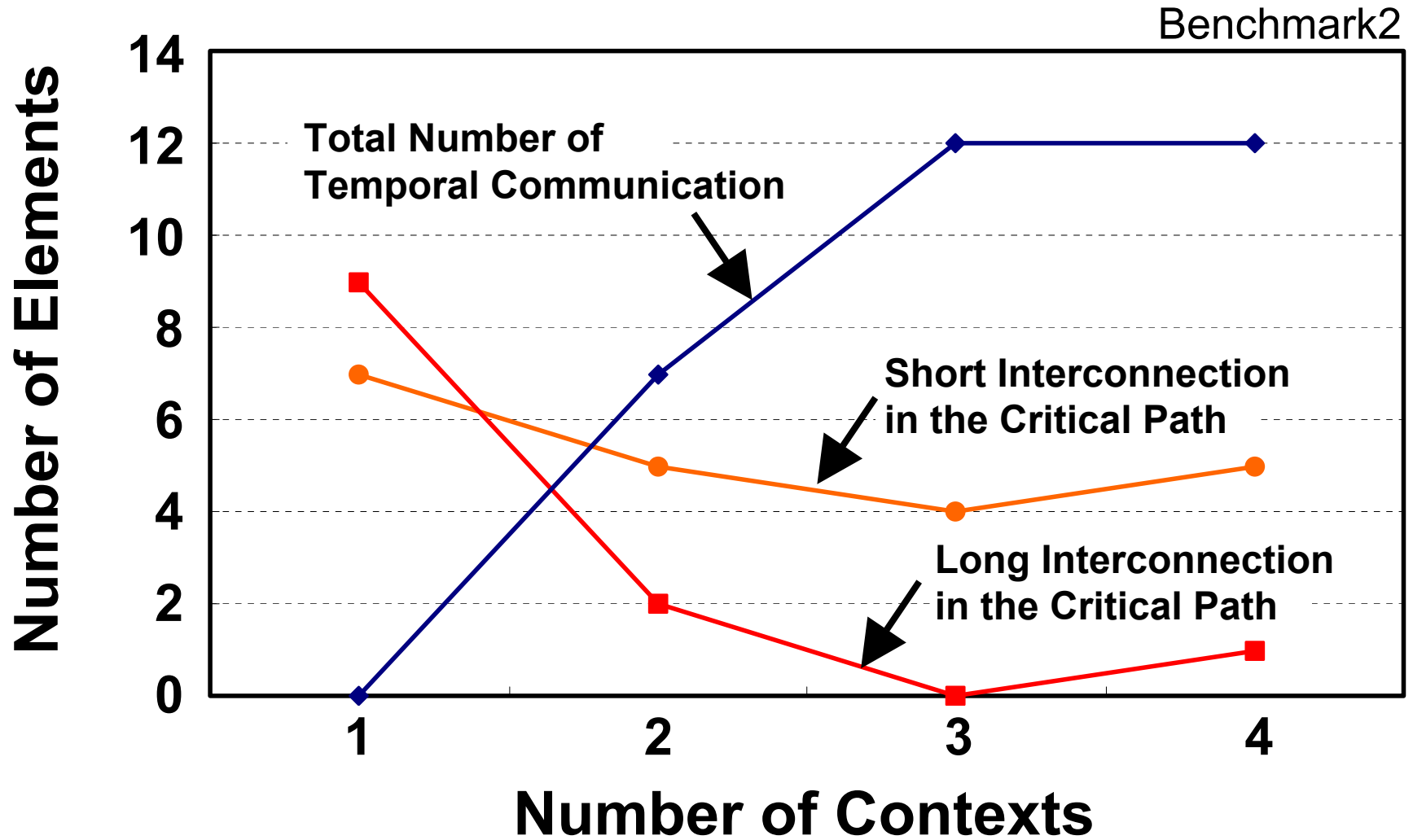
Number of Interconnections and Necessary Resources were Dramatically Decreased

Measurement Results



We found, for the first time, that the best exec. speed was obtained when multi contexts are used

Relation between Temporal Communication and Interconnections



As the Number of Contexts Increases, Interconnections are Converted to Temporal Communication

Conclusion

- A new DRFPGA has been proposed, by which long interconnection can be converted to much shorter interconnections
- Generally FPGA is said to be faster than DRFPGA, but we discovered cases where multi-context implementation works faster than FPGA

**Dynamic Reconfiguration Deserves
Fresh Attention!**