1D-9

Improving Execution Speed of FPGA using Dynamically Reconfigurable Technique

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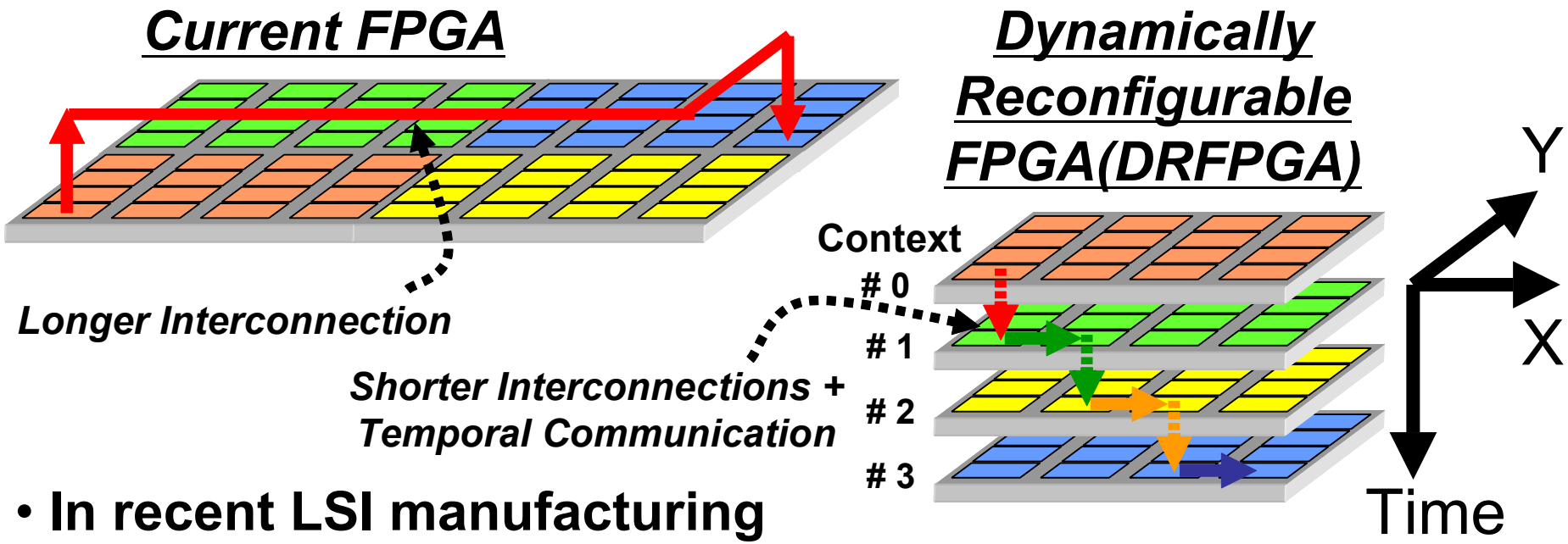
Motivation of This Work

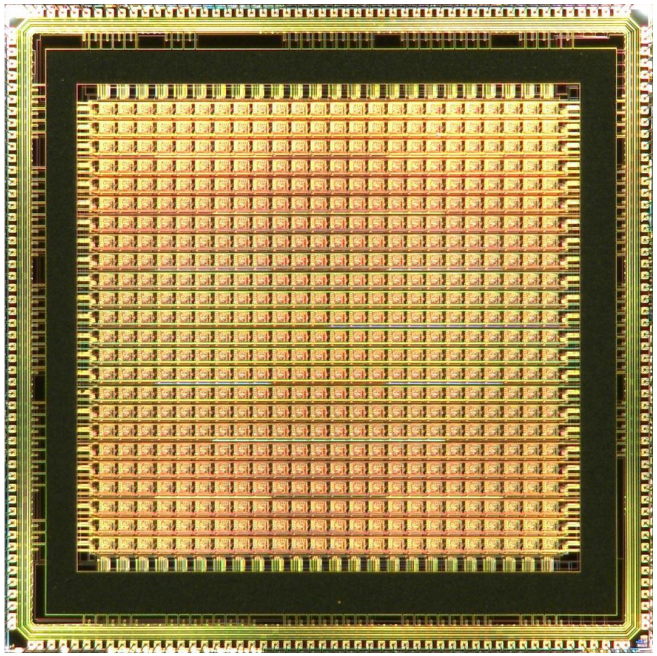
- **To Reduce Interconnect Delay in FPGAs**



- **In recent LSI manufacturing**
  Interconnect Delay >> Gate Delay
- **Long Interconnection → Shorter Interconnections via Temporal Communication**

Dynamic Reconfiguration can Reduce Interconnect Delay in FPGAs!

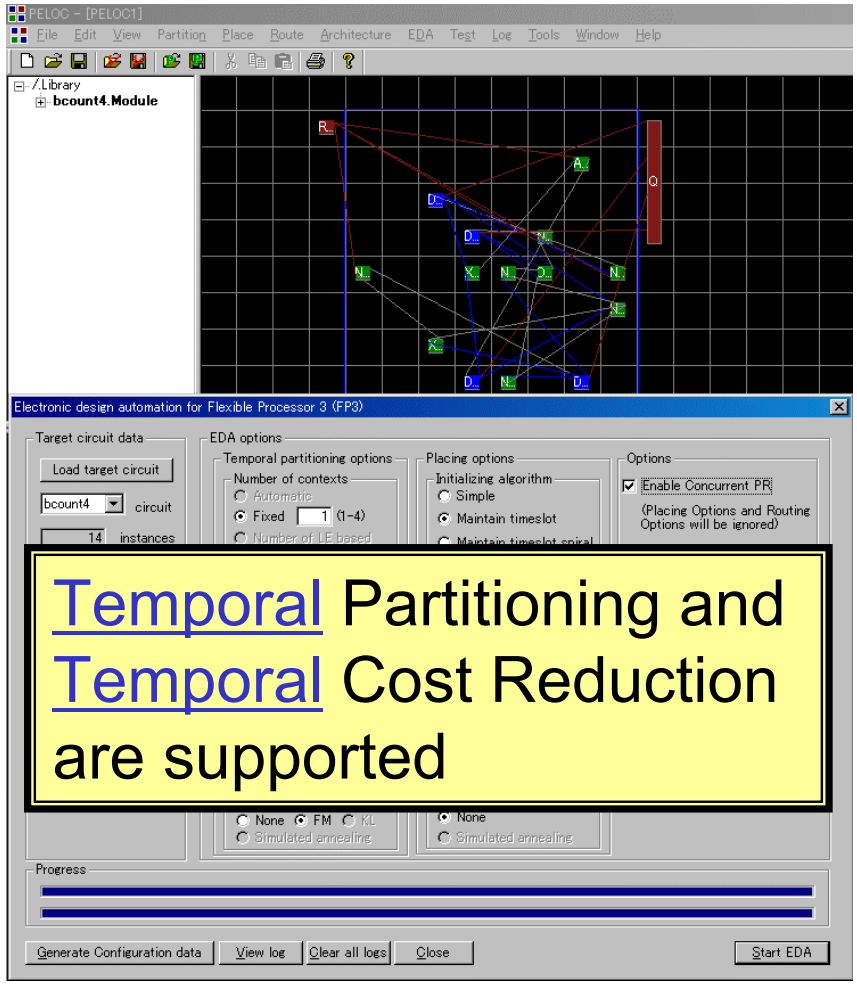
Dynamically Reconfigurable FPGA (FP-III) and its Design Automation Software (PELOC)



7.29mm

FP-III chip die photo

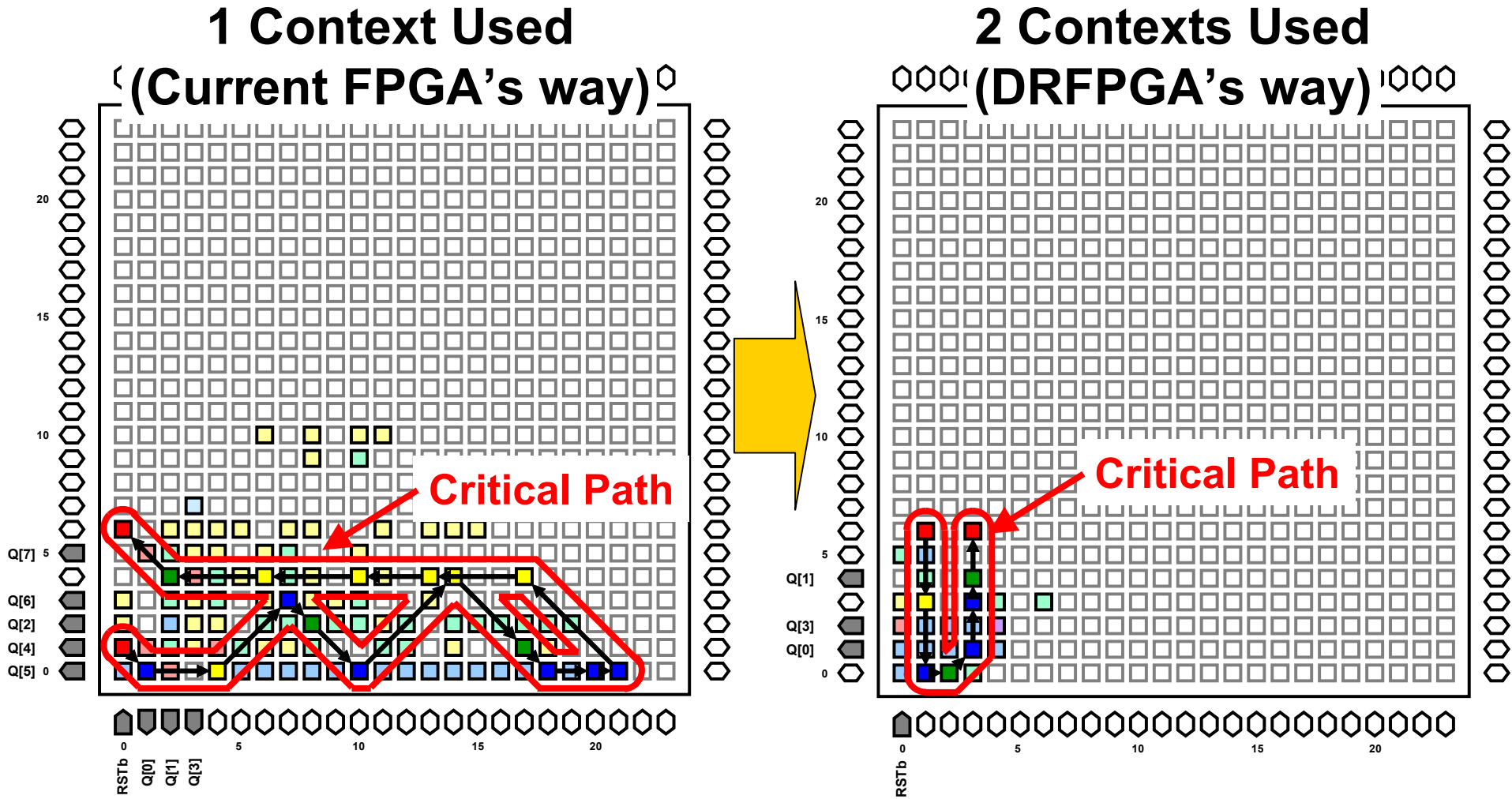
0.35um CMOS 2P3M
4 Context Planes
24x24 Array of LE
Nearest Neighbor Architecture
Die Size: 9.86mm□



Temporal Partitioning and Temporal Cost Reduction are supported

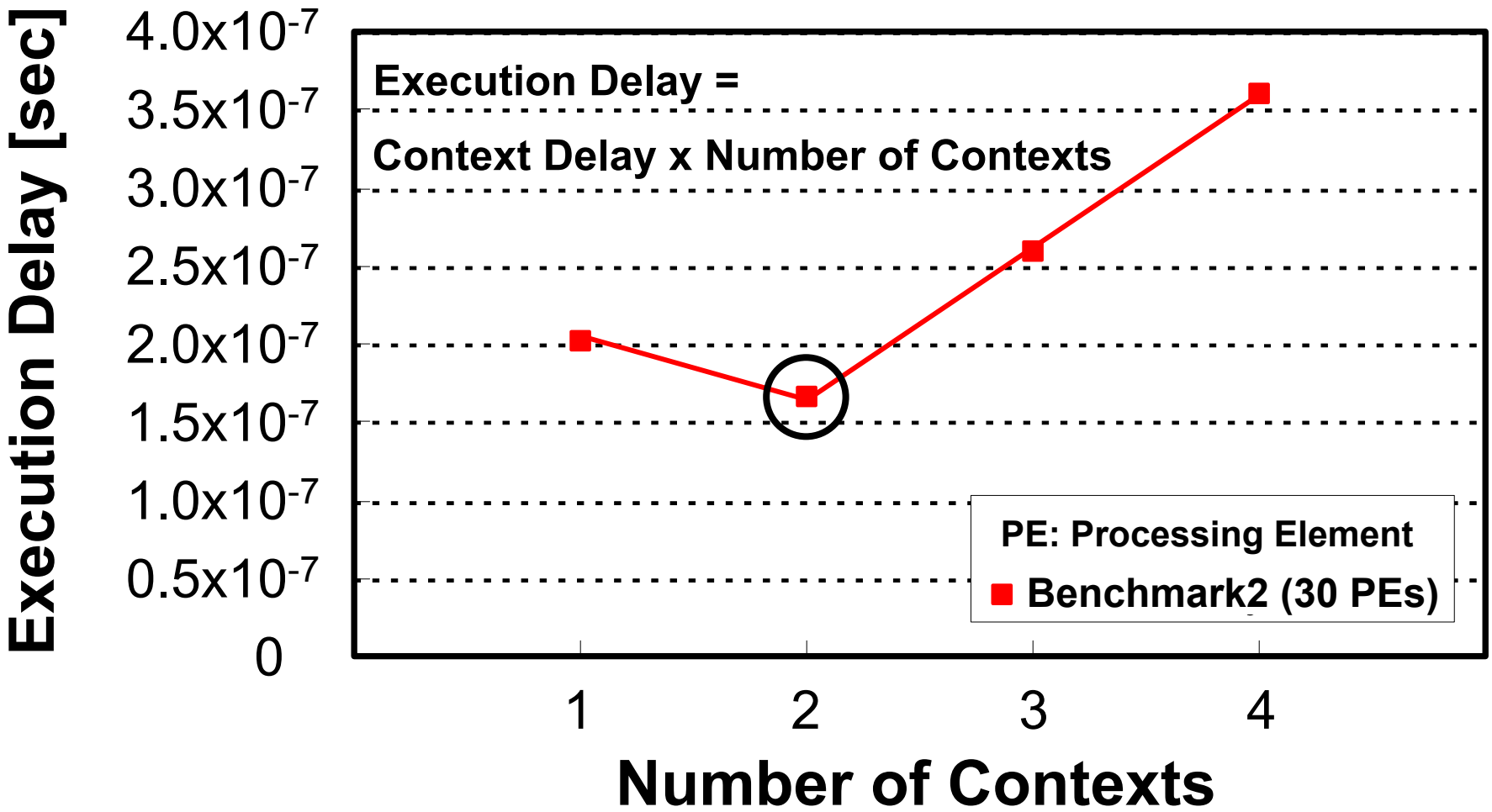
PELOC view
(Processor ELement LOCator)

Placing & Routing Results



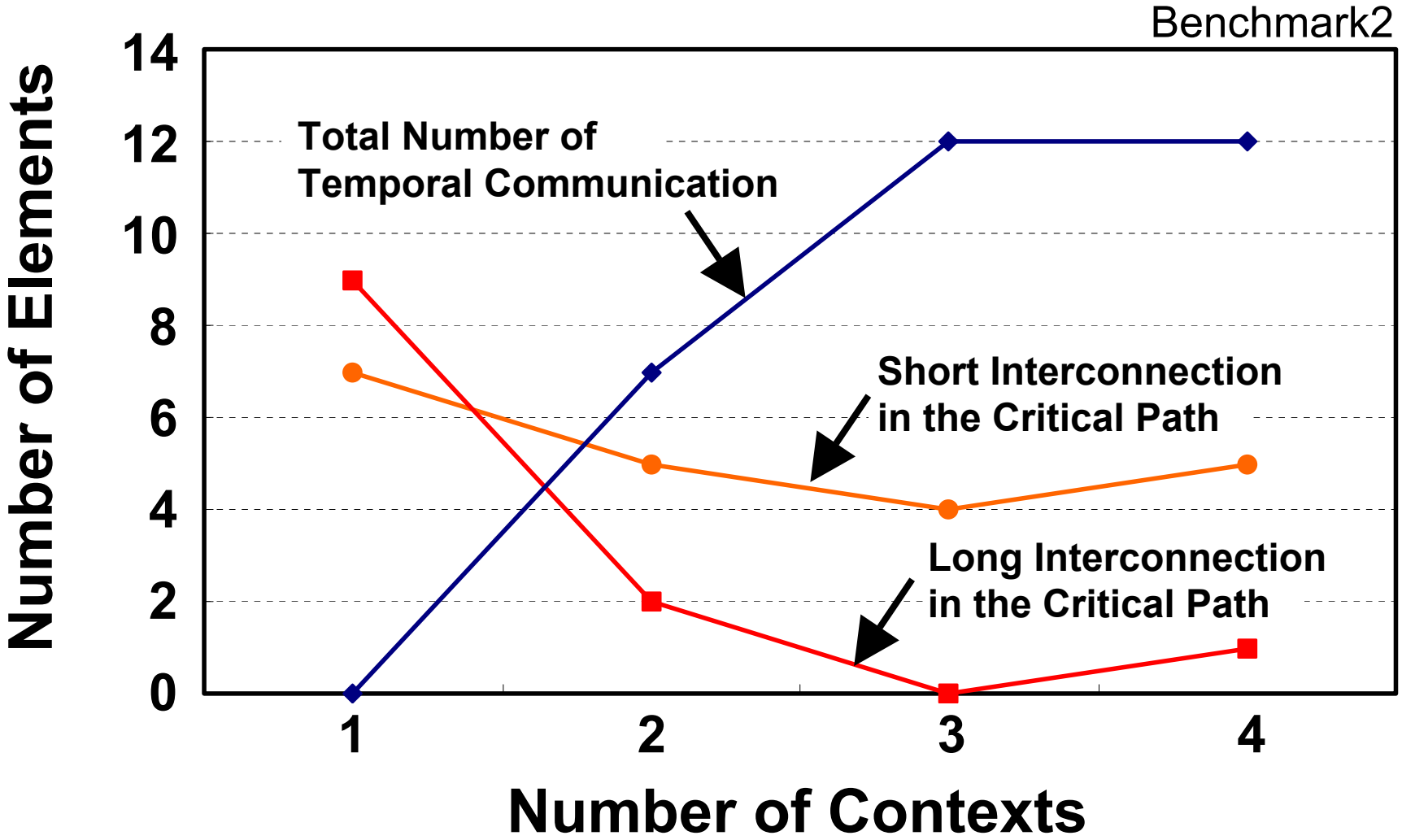
Number of Interconnections and Necessary Resources were Dramatically Decreased

Measurement Results



We found, for the first time, that the best exec. speed was obtained when multi contexts are used

Relation between Temporal Communication and Interconnections



As the Number of Contexts Increases, Interconnections are Converted to Temporal Communication

Conclusion

- A new DRFPGA has been proposed, by which long interconnection can be converted to much shorter interconnections

- Generally FPGA is said to be faster than DRFPGA, **but we discovered cases where multi-context implementation works faster than FPGA**

Dynamic Reconfiguration Deserves Fresh Attention!