Electronic Design Automation

Hippocrates: First-Do-No-Harm Detailed Placement

Haoxing Ren, David Pan*,
Charles J. Alpert, Gi-Joon Nam,
Paul Villarrubia

* University of Texas, Austin, USA

Building Blocks of Physical Synthesis

Placement
(find non-overlapping locations to minimize wirelength)

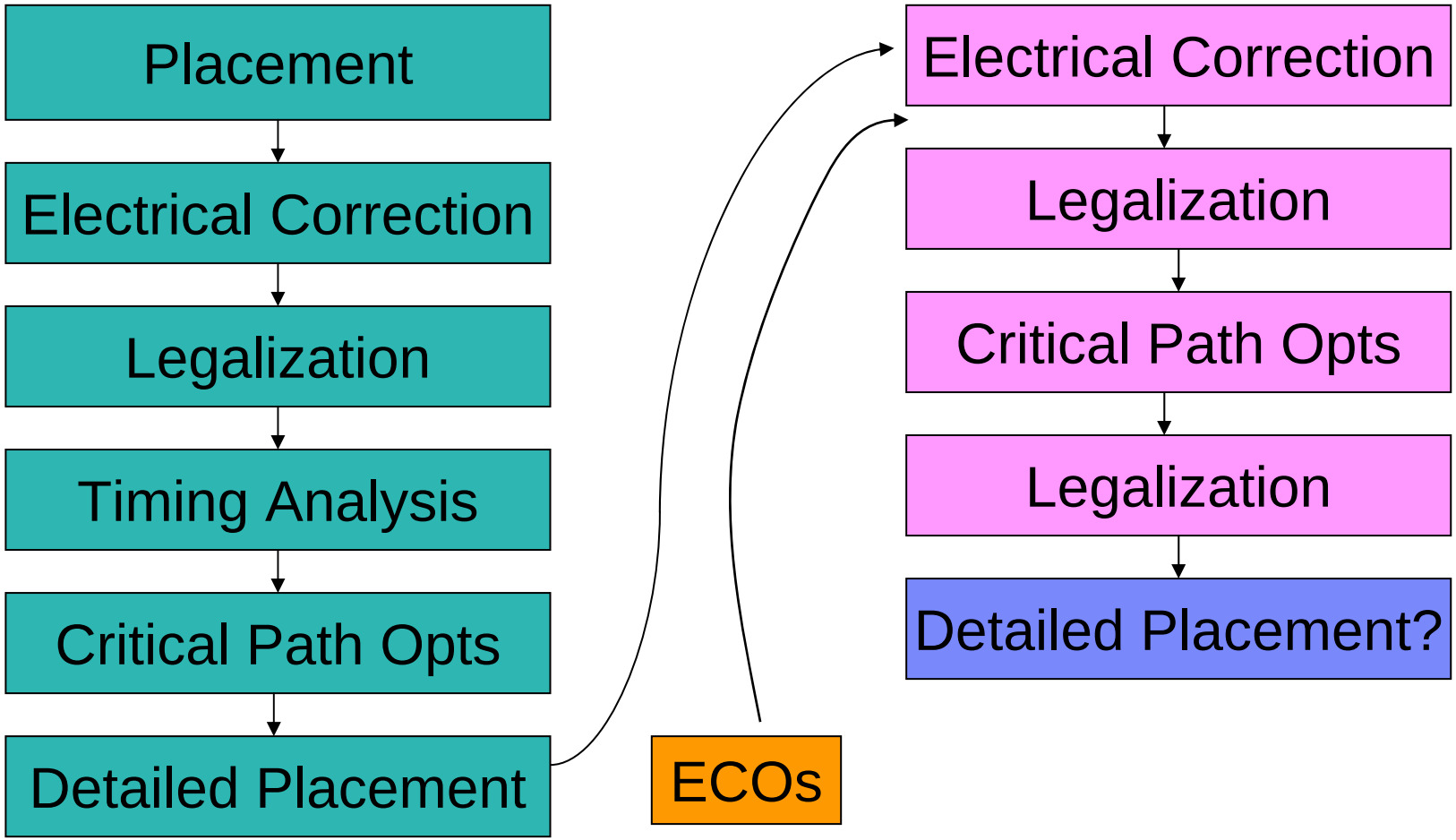
Critical Path Opts
(incremental synthesis to optimize most critical regions)

Electrical Correction
(buffer and repower to fix slew and cap constraints)

Detailed placement
(Locally improve wirelength)

Legalization
(place those buffers and logic in legal locations)

Example Physical Synthesis Flow



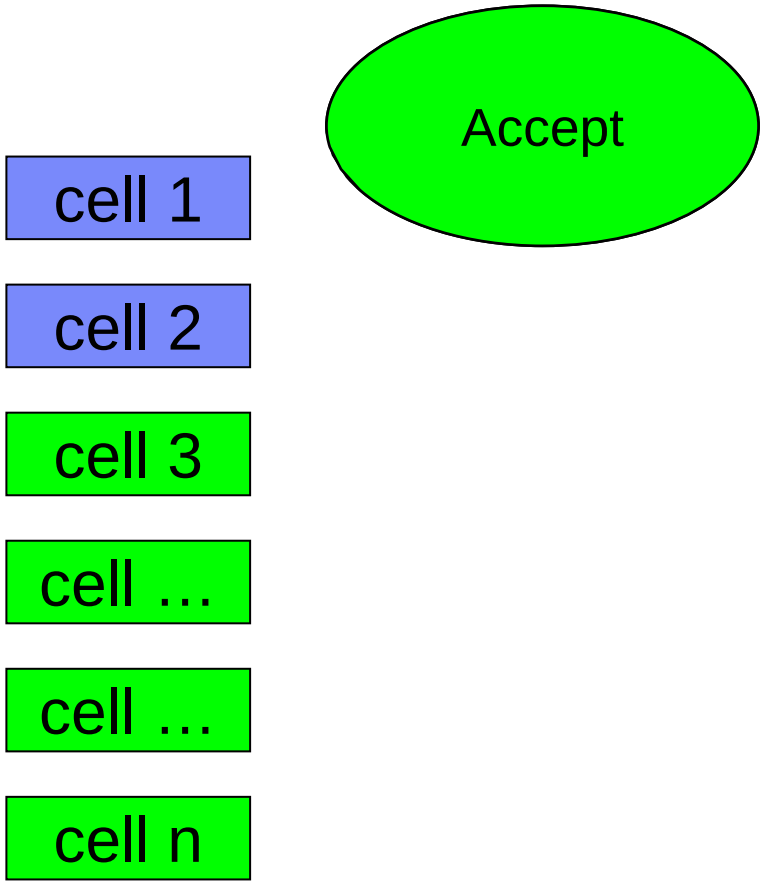
Essence of Detailed Placement

- **Can move lots of things around**
- **Can disrupt / degrade well-timed design**
- **Today: unsuitable for being run late in the flow**
- **But: there may be a need for it**
  - Improve wirelength
  - Improve routability
- **We need a “gentle detailed placer”**
  - Does not disrupt timing
  - Still makes the obvious improvements

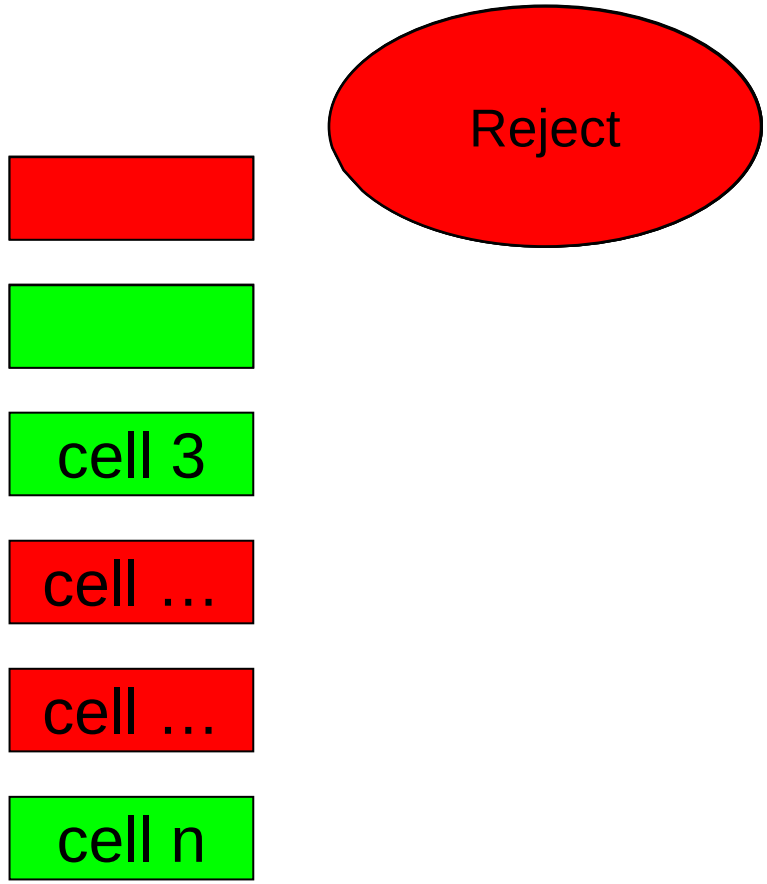
This Work

- **Two choices**
  - Consider a DP move
  - Accept or reject it
- **Today:**
  - Detailed placement accepts all moves that improve wirelength
- **Hippocrates:**
  - Accepts moves that improve wirelength and do not degrade timing
  - Moves are a **subset** of traditional DP

Conventional DP



Hippocrates



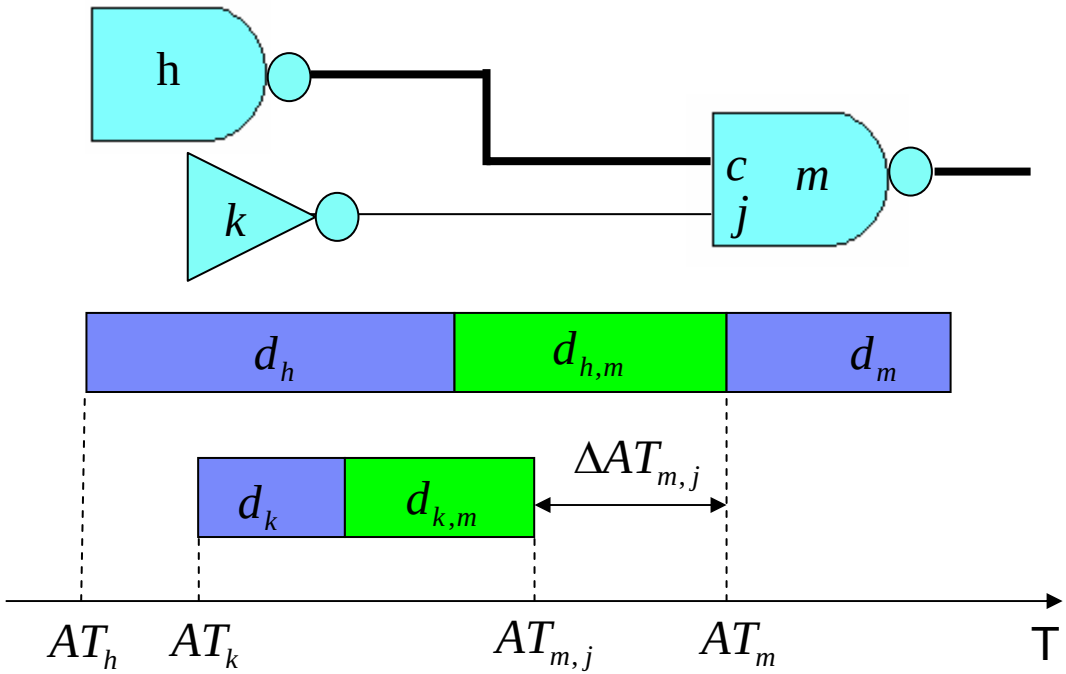
Outline: Key Concepts within Hippocrates

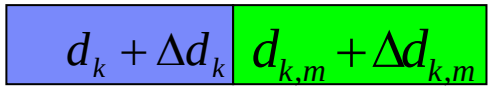
- **DP Constraints**
  - Delay Constraints: Delta Arrival Time
  - Electrical Constraints
- **Constraint Formulation**
  - Delay and slew computation for gates and wires
- **Combined Delay and Electrical Constraints**
- **DP Objective**
- **DP Transforms**
- **Hippocrates Flow**
- **Experimental Results**

Timing Constraints Within Placement

- **Need to repeatedly evaluate timing during placement**
- **Cannot use static timers in an iterative manner**
  - There are exponential number of paths
  - Slow
- **Divide and Conquer: transform path based delay constraints to pin based delay constraints.**
- **Propose: Delta Arrival Time**
  - Reduces the computation complexity
  - Bypasses the accuracy problems of estimating timing in placement

Delay Constraints : Delta Arrival Time

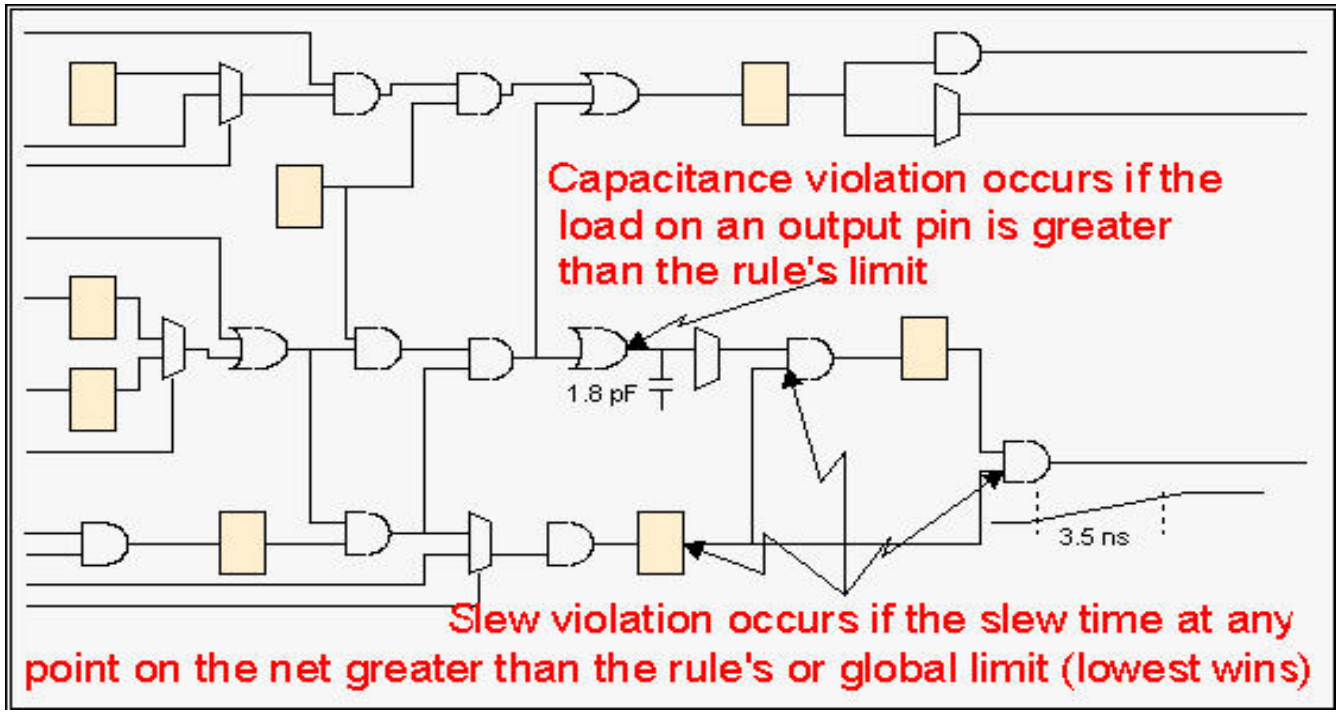




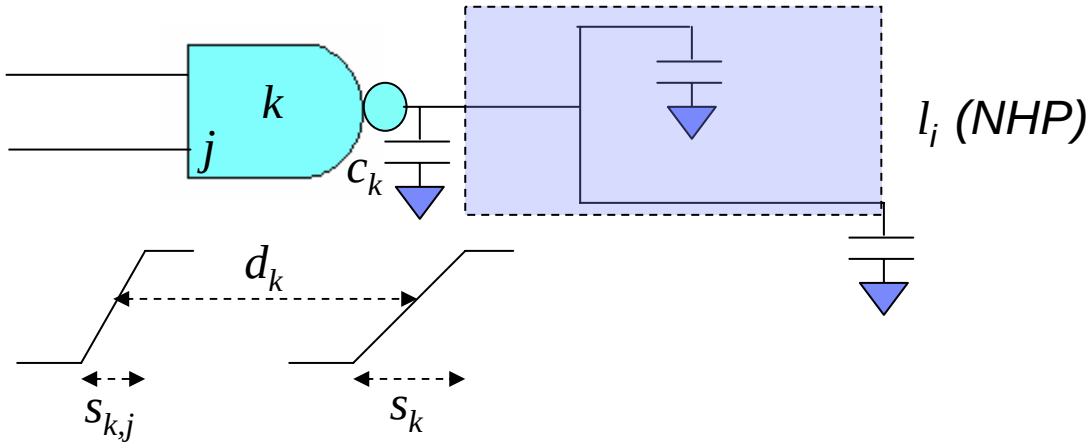
$$\Delta d_k + \Delta d_{k,m} \leq \Delta AT_{m,j}$$

Electrical Constraints

- **Maximum input slew** $\Delta s_{m,j} \leq s_{m,j}^{\max} - old\_s_{m,j}$
- **Maximum output load** $\Delta c_k \leq c_k^{\max} - old\_c_k$



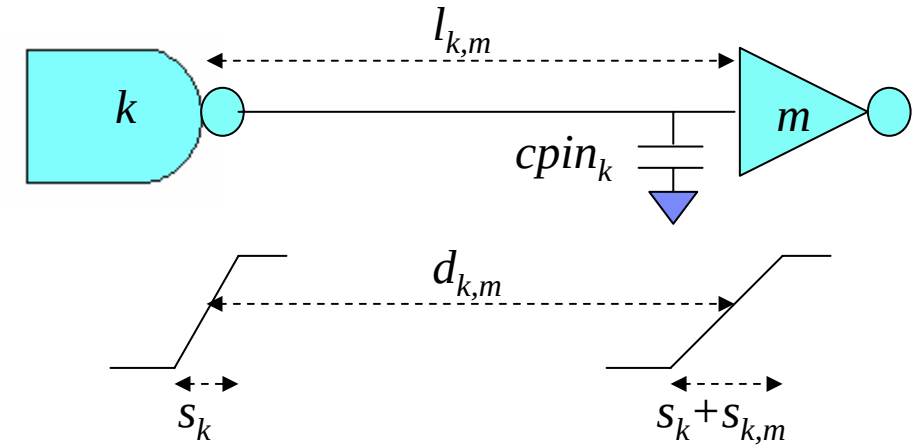
Incremental Gate Delay and Slew



- **Assuming critical input slew is constant**
- **Load incremental is only depend on net bound box**

$$\Delta d_k = A_k \Delta c_k$$
$$\Delta s_k = B_k \Delta c_k$$
$$\Delta c_k = c \Delta l_i$$

Incremental Wire Delay and Slew



- **Wires are modeled as driver to sink star model**
- **Wire delay are model by PI model**
- **Assuming all the sink pins input capacitances at the end of the wire**

$$\Delta d_{k,m} = K_D \left[r\,(c \cdot old\_l_{k,m} + cpin_k) \cdot \Delta l_{k,m} + \frac{rc\,(\Delta l_{k,m})^2}{2} \right]$$

$$\Delta s_{k,m} = K_S \left[r\,(c \cdot old\_l_{k,m} + cpin_k) \cdot \Delta l_{k,m} + \frac{rc\,(\Delta l_{k,m})^2}{2} \right]$$

Combined Incremental Delay & Slew

$$\Delta d_k + \Delta d_{k,m} = \alpha \Delta l_i + \beta \Delta l_{k,m} + \gamma \Delta l_{k,m}^2$$
$$\Delta s_k + \Delta s_{k,m} = \zeta \Delta l_i + \eta \Delta l_{k,m} + \theta \Delta l_{k,m}^2$$

where

$$\alpha = A_k c$$
$$\beta = K_D r (c \cdot old\_l_{k,m} + cpin_k)$$
$$\gamma = K_D rc/2$$
$$\zeta = B_k c$$
$$\eta = K_S r (c \cdot old\_l_{k,m} + cpin_k)$$
$$\theta = K_S rc/2$$

DP Constraints

- **DP can easily measure net half perimeter (NHP) and source-to-sink wirelength.**
- **Express the delay and electrical constraints in terms of wirelength**

Delay constraint $\alpha\Delta l_i + \beta\Delta l_{k,m} + \gamma\Delta l_{k,m}^2 \leq \Delta AT_{m,j}$

Slew constraint $\zeta\Delta l_i + \eta\Delta l_{k,m} + \theta\Delta l_{k,m}^2 \leq s_{m,j}^{\max} - old\_s_j$

Cap constraint $c\Delta l_i \leq c_k^{\max} - old\_c_k$

DP Objective

- **Use weighted total wirelength (WTWL) as the DP optimization objective.**

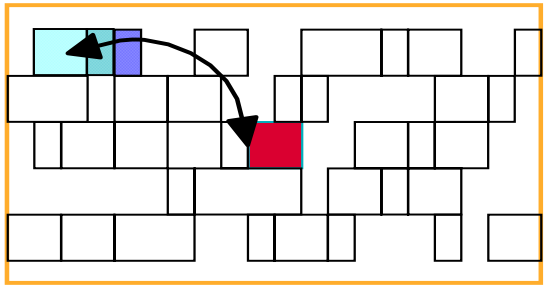
$$WTWL = \sum w_i l_i$$

- **Weights reflect timing criticality.**

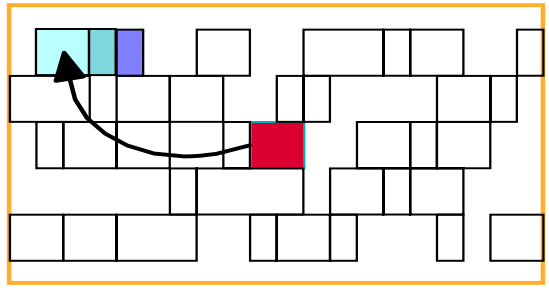
$$w_i = \begin{cases} W_0 - W_1 slk_i & slk_i < 0 \\ W_0 & slk_i \geq 0 \end{cases}$$

- **This objective drives DP to reduce wirelength on critical nets, which helps improve timing as well**

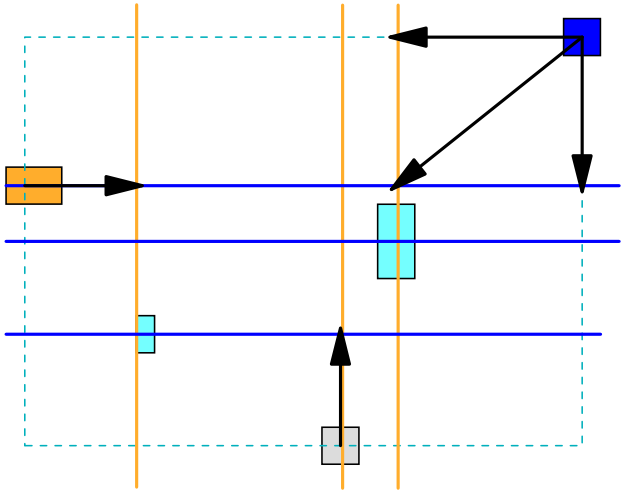
DP Transforms



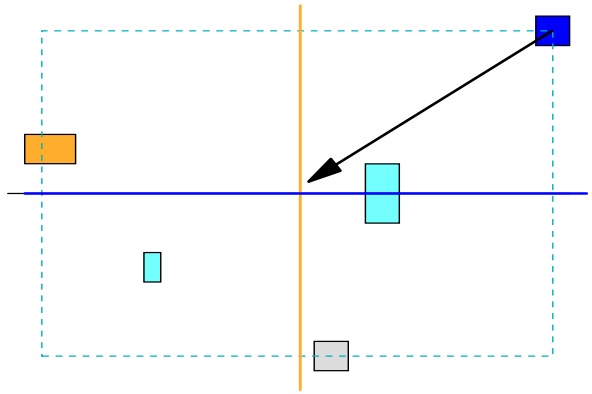
SWAP



MOVE

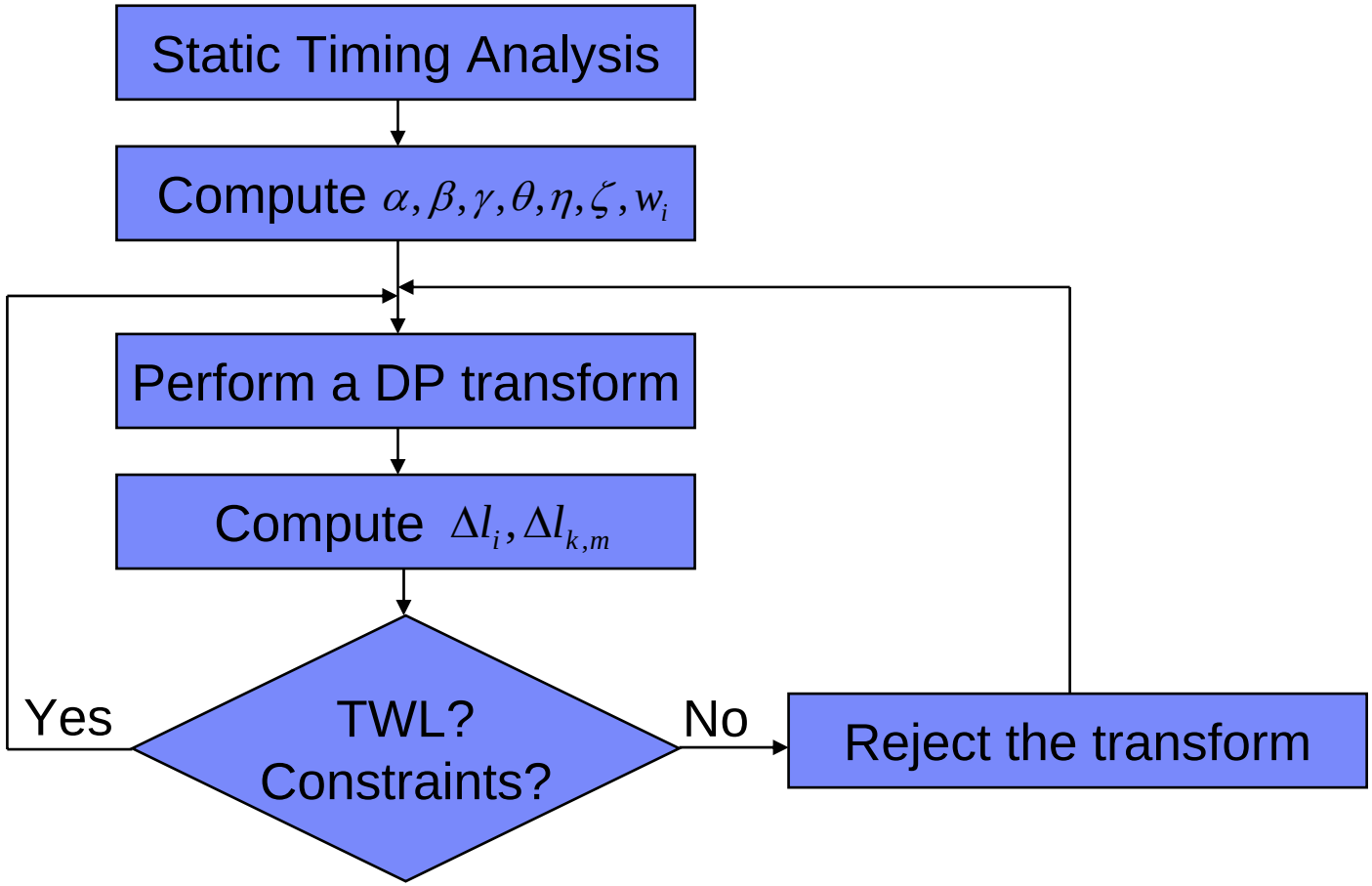


COMPACT



CENTER

Hippocrates DP Algorithm

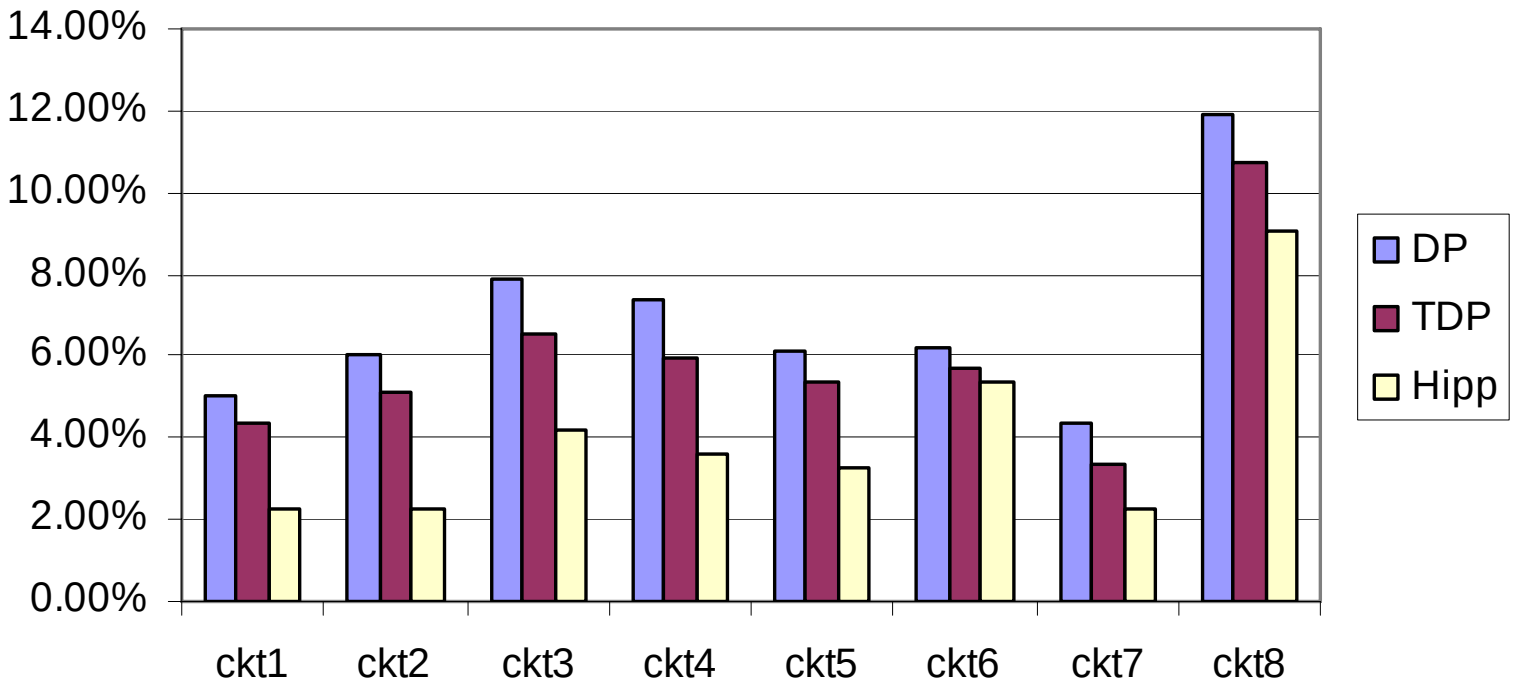


Experiments

- **Take the netlists from physical synthesis output**
- **Compare Hippocrates (Hipp) to weighted wirelength DP (TDP) and regular wirelength driven DP (DP)**

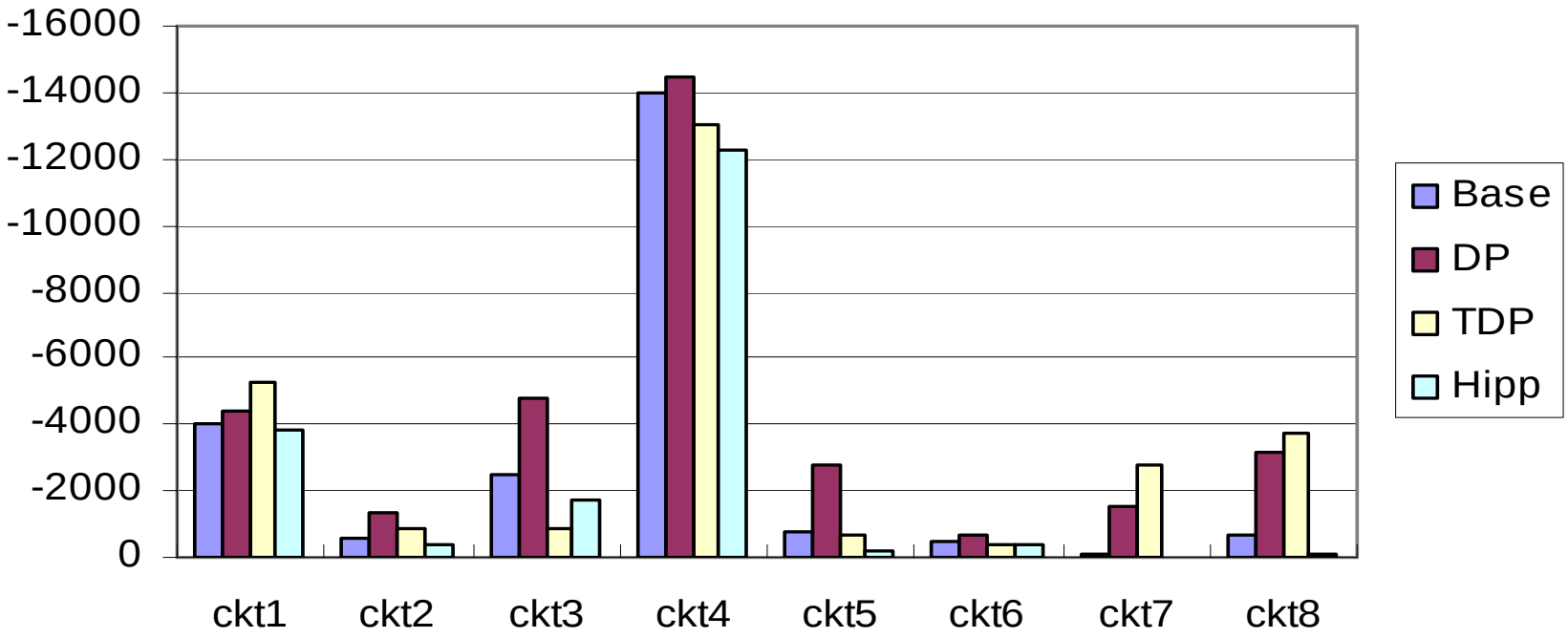
Designs	Cells	Tech (nm)	TNS (ns)	WNS (ps)
ckt1	3.9K	65	-4.048	-42
ckt2	3.9K	65	-0.575	-20
ckt3	4.4K	65	-2.447	-50
ckt4	6.0K	65	-14.011	-64
ckt5	7.5K	65	-0.753	-1
ckt6	64K	130	-452	-409
ckt7	295K	90	-83	-97
ckt8	445K	90	-631	-915

TWL



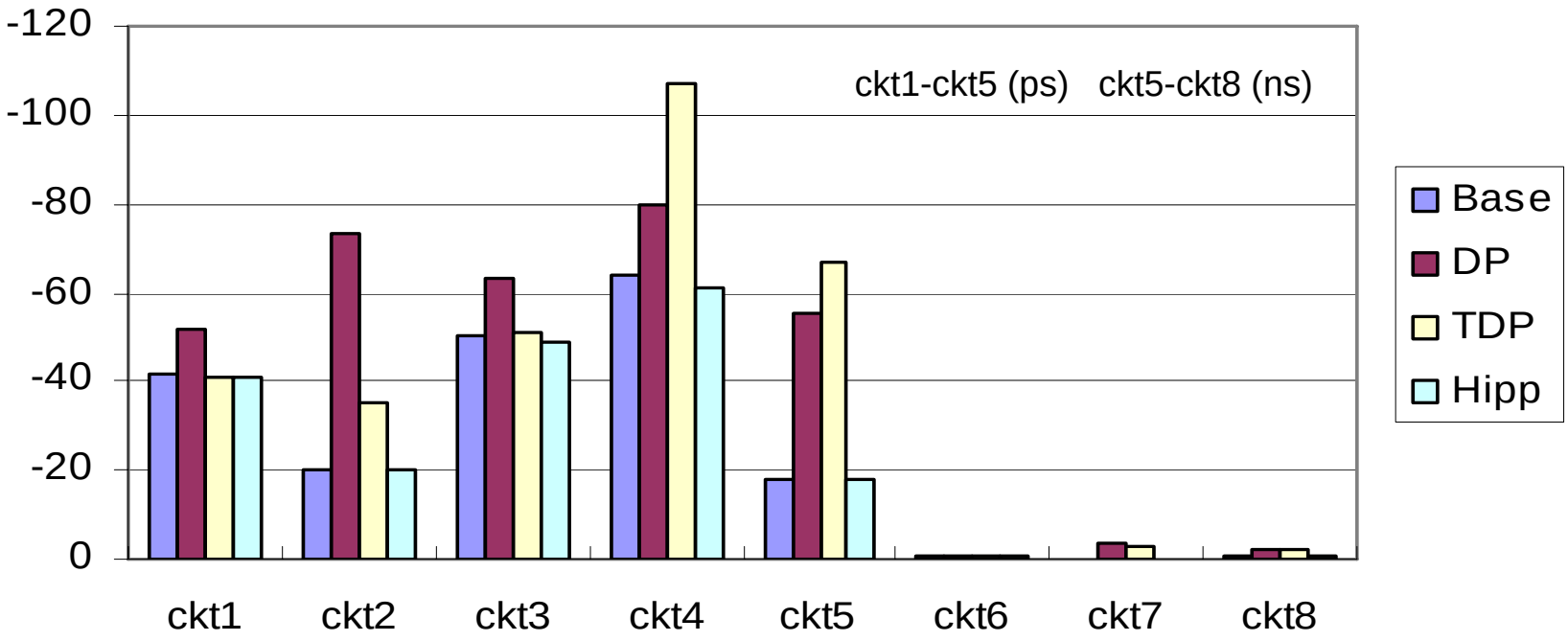
Average TWL improvement 4%

Timing (TNS)



	TNS %	Worse #
DP	-332	8
TDP	-469	4
Hipp	37	0

Timing (WNS)



	WNS %	Worse #
DP	-513	8
TDP	-418	7
Hipp	4	0

Runtime (sec)

Designs	DP	TDP	Hipp
ckt1	4	4	10
ckt2	5	5	12
ckt3	5	5	13
ckt4	6	6	16
ckt5	7	7	20
ckt6	76	81	366
ckt7	330	350	1230
ckt8	792	870	1788

Conclusions

- **Novel Idea - Timing/Electrical Constrained DP**
  - Reduce wirelength while keep original timing/electrical behavior
- **Novel Idea - Delta Arrival Time**
  - Reduces the computation complexity
  - Bypasses the accuracy problems of estimating timing in placement
- **Applications**
  - Incremental wirelength/timing improvement
  - Latch clustering for low power