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Thermal-driven Symmetry Constraint for Analog Layout with CBL Representation

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Outline

- Thermal effect on SOI technology
  - Self-heating effect of SOI
  - Device-level thermal behaviors
- Geometric symmetry with CBL
  - Topological relation in CBL
  - Symmetry feasible CBL
  - Solution Generator for symmetry-feasible CBL
- Experiment Design
- Experimental Results
- Conclusions

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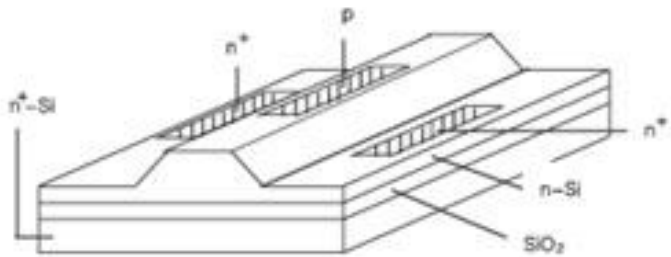
Introduction of SOI

- As the increase in frequency of the circuits, thermal constraint is becoming more and more important because of the poor thermal conductivity of the relatively thick buried oxide layer of SOI (silicon on insulator).
- For symmetrical devices, the thermal constraint is more serious, because temperature gradient on symmetrical devices may cause error even failure on the performance.

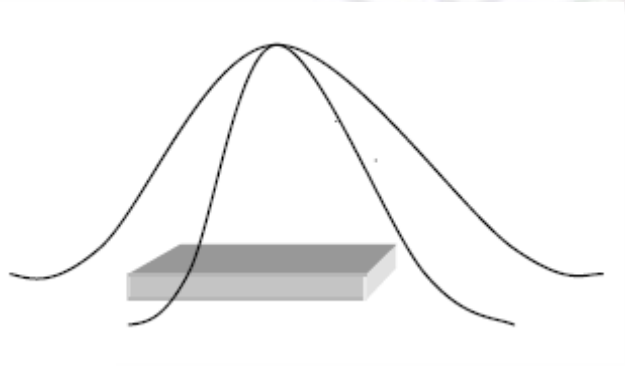


Related Works

- The traditional works on symmetry constraint such as symmetry with Binary Tree (F.Balasa, etc. ICCAD2000), with SP (F.Balasa, etc. TCAD2000) and with TCG-S (Jai-Ming Lin, etc. ASPDAC2005) assume that the circuit is isothermal, since the substrate material has good thermal conductivity.
- But this assumption must be questioned in the context of thermal-sensitive symmetrical analog devices and the use of SOI technology, because the isolating buried oxide layer has a lower thermal conductivity, often over 100 times worse than silicon.

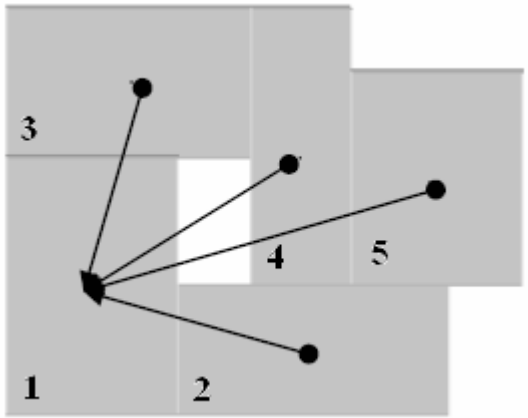
Self-heating effect of SOI

- As a result, increases in the channel temperature of tens of degrees due to self-heating effect can be observed.
- And some of the heat generated by the distinct devices will flow laterally before reaching the substrate.



Self-heating effect of SOI

- Thus the devices around them will be also affected, and the temperatures of these neighboring transistors will rise, too.



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Device-level thermal behaviors

- The risen temperature will affect the channel current through the carrier mobility, threshold voltage and velocity saturation mechanisms.
- The following three equations show the relations between them.
- The combination of these effects results in a reduction in drawn current with the increasing temperature.

Device-level thermal behaviors

- Relation between the carrier mobility and temperature:

$$\mu_{eff} = \mu_{eff,0}(T/T_0)^{-k}$$

- Relation between threshold voltage and temperature:

$$V_T = V_{T0} - \lambda(T - T_0)$$

- Relation between velocity saturation and temperature:

$$v_{SAT} = 2.4\times10^7 /(1+0.8\exp(T/600))$$

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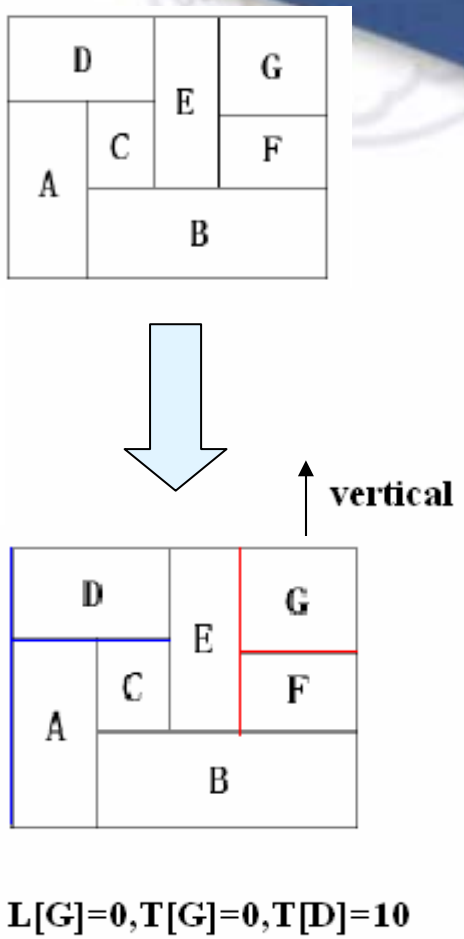
Introduction of CBL

- CBL which stands for Corner Block List is composed of three sequences: S, L and T.
- The figure on the right hand denotes a floorplan and its sequence S is (*ABCDEFG*), L is (*100110*) and T is (*0,0,10,10,0,0*).
- In CBL, sequence L and sequence T describe the T-junctions' information covered by every module. Thus, it is difficult to use L and T to recognize the topological relations between modules.

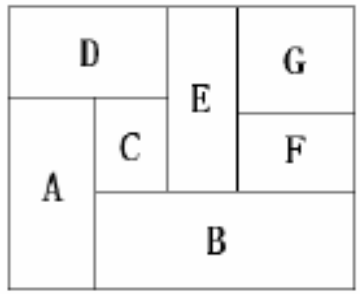


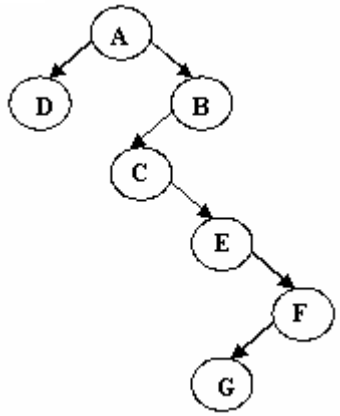
Symbolic Determinations

- First, some symbolic determinations are introduced:
  - S[A]<S[B], if A is before B in Sequence S.
  - S[A]>S[B], if A is after B in Sequence S.
  - A LT B, if A is to the left of B.
  - A RT B, if A is to the right of B.
  - A BW B, if A is below B.
  - A AE B, if A is above B.

Topological relation in CBL

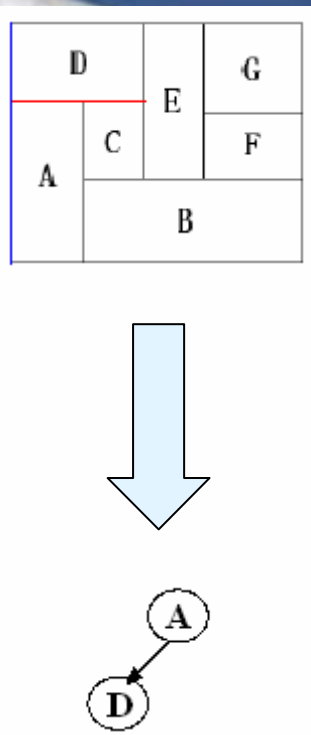
- As a result of the difficulty of recognizing topological relations, a tree structure called *T-bl* which is show in the figure is created in order to handle this problem.





Construction Rules for T-bl

- *Lemma 1: Construction rules for T-bl*
  - *R(1) If two modules M and N are separated by a horizontal cutline, which share a common left boundary, and M is above N, M is N's left subtree.*
  - *R(2) If two modules M and N are separated by a vertical cutline, which share a common bottom boundary, and M is to the right of N, M is N's right subtree.*
- In *T-bl*, every module has its number labeled as *Treenum.* All the nodes' *Treenum* can be got by an inorder traversal of *T-bl.*



Topological relation Recognition

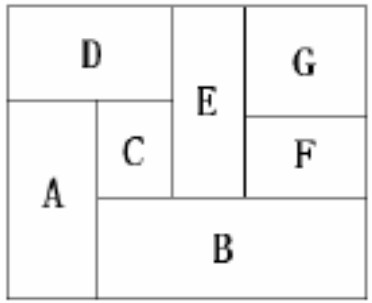
- *Theorem 1: Recognition of topological relations*
  - *If S[M]>S[N] and M' s Treenum<N's Treenum, M AE N.*
  - *If S[M]>S[N] and M' s Treenum>N's Treenum, M RT N.*

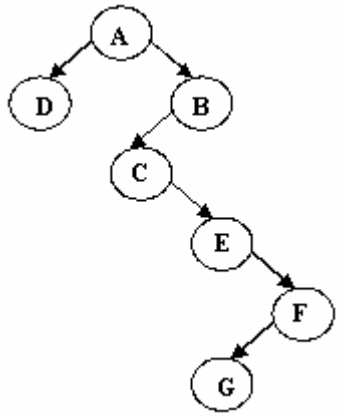
An example:

S[A]<S[D] and

A's Treenum=2, D's Treenum=1

Therefore, D is above A.





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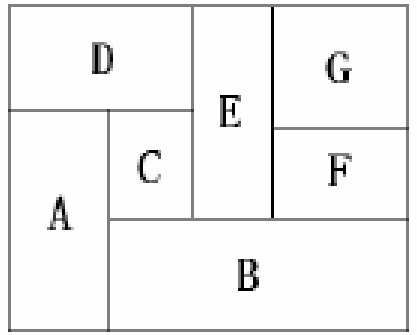
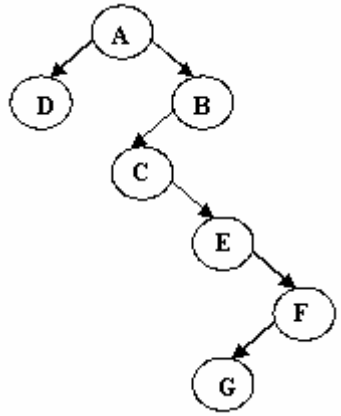
Conditions for Feasible-CBL

- *Theorem 2: Conditions for Feasible-CBL*
- *If all the k symmetry groups comply with the following two conditions, this CBL is a Feasible-CBL for symmetry.*
  - *C(1): For i=1 to k, Mi LT Mi.sym or Mi RT Mi.sym.*
  - *C(2): For i and j in [1,k] and i<>j,*
    - ✓ *If S[Mi]<S[Mj], S[Mi.sym]<S[Mj.sym] and Mi BW Mj, Mi.sym BW Mj.sym.*
    - ✓ *If S[Mi]<S[Mj], S[Mi.sym]>S[Mj.sym] and Mi LT Mj, Mi.sym RT Mj.sym.*

Symmetry feasible CBL

- For example, (D, G) and (C, F) are symmetry groups.
- According to Theorem 1, D LT G, C LT F complying with C(1).
- And S[D]<S[F], D's Treenum=1, F's Treenum=6, so D LT F. It is the same for C and G.
- Therefore, this floorplan is a symmetry feasible CBL.





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Solution Generator for symmetry-feasible CBL

- According to *Theorem 2*, whether a CBL can be converted to placement with symmetry constraint can be examined.
- But it can't be used directly in simulated annealing to search for an optimal placement, because it has been proved by F.Balasa that symmetry constraint would cause a great reduction to the feasible solution space.
- That means most of the random new solutions are not feasible-CBL.

Solution Generator for symmetry-feasible CBL

- *Solution generator for symmetry-feasible:*
  - *(1) Exchange two modules in Sequence S. If the two modules belong to distinct symmetry groups, their symmetrical modules should also exchange their positions in T-bl;*
  - *(2) Exchange two modules' TreeNums. And similarly, if they belong to different symmetry groups, their symmetrical modules should also exchange their positions in Sequence S;*
  - *P.S. for (1) and (2), the swapping of a symmetrical module and a free module is invalid.*
  - *(3) Rotate modules. If the module belongs to a symmetry group, its symmetrical module should also be rotated.*
  - *(4) Change the shape of modules. If the module belongs to a symmetry group, its symmetrical module should also be changed.*

Multi-symmetry Axes

- And the requirement of multi-symmetry axes with the same orientation which is more general to analog circuit can be modeled in a similar way.
- First all the symmetry groups belonging to distinct axes should comply with *C(1)* and *C(2)* respectively.
- Then the new solution generation process should also comply with the solution generator for symmetry feasible.

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Experiment Design

- The objective of thermal-driven symmetry constraint is composed of three parts: (1) high density of placement with symmetry, (2) decreasing temperature gradient on symmetrical devices, (3) avoiding hot-spot effect.
- The following equation denotes the objective function for decreasing temperature gradient. And this equation reflects the average temperature difference of all the symmetry groups.
- $$F_1 = \frac{1}{m}\sum_{i=1}^{m} | T_i - T_{i.sym} |$$
- *m* stands for the number of symmetry groups, *Ti* and *Ti.sym* are the temperatures of the two devices in the same symmetry groups

Experiment Design

- The next equation is the objective function for avoiding hot-spot. It is achieved by decreasing the difference of Tj and Tavg.

$$F_2 = \sum_{j=1}^{n} (|1 - \frac{T_j}{T_{avg}}|)$$

- At last, the objective function can be formed in the equation below:

$$F = w_1 \times Area + w_2 \times F_1 + w_3 \times F_2$$

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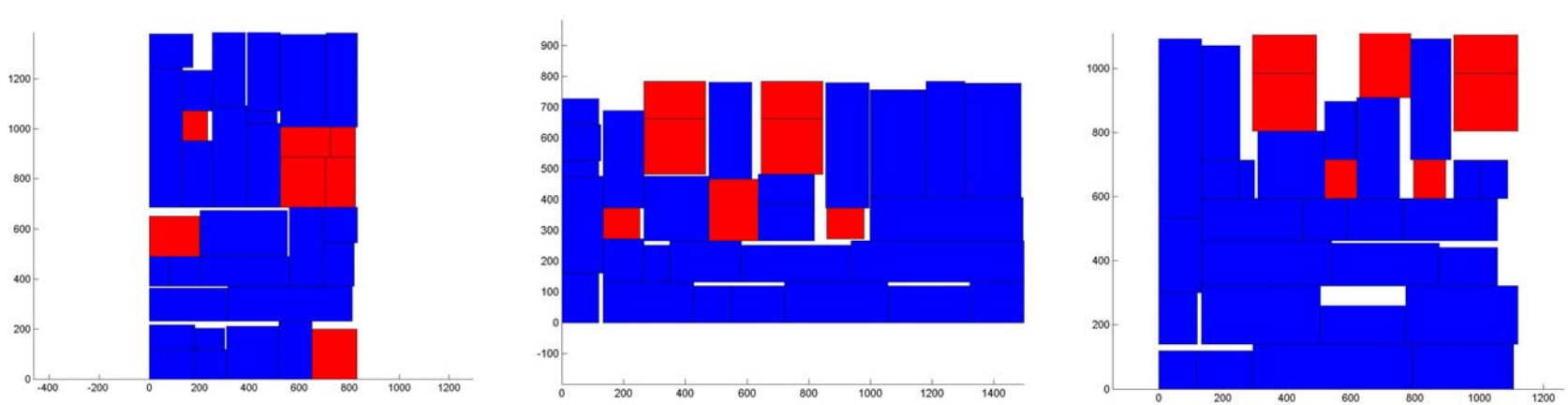
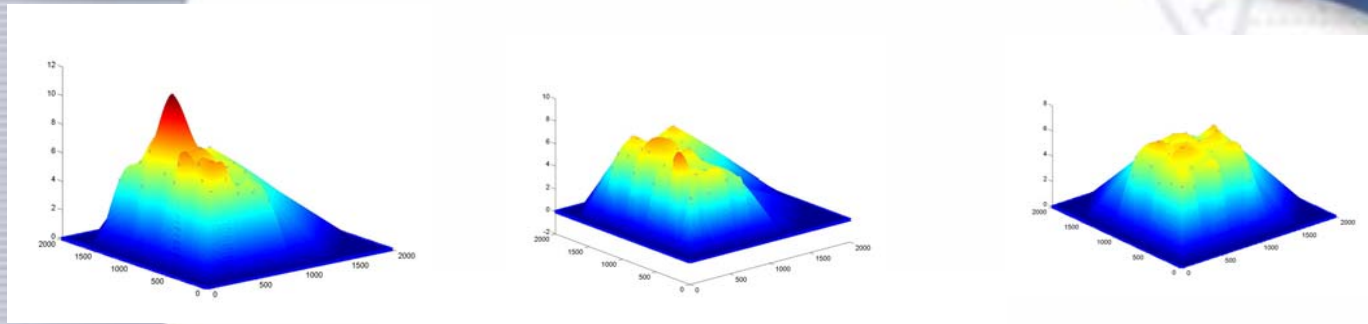
Ami33 Placement



(a) Without constraint; (b) With symmetry;
(c) With both symmetry and thermal constraints

Heat Distribution of ami33



(a) Without constraint; (b) With symmetry;
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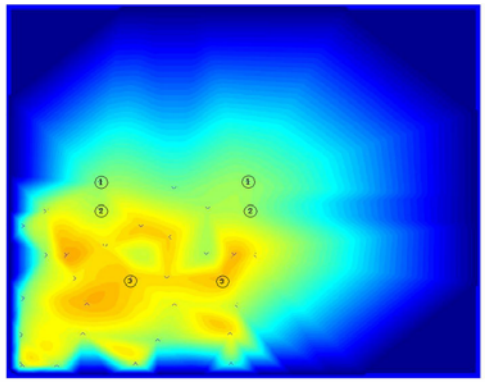
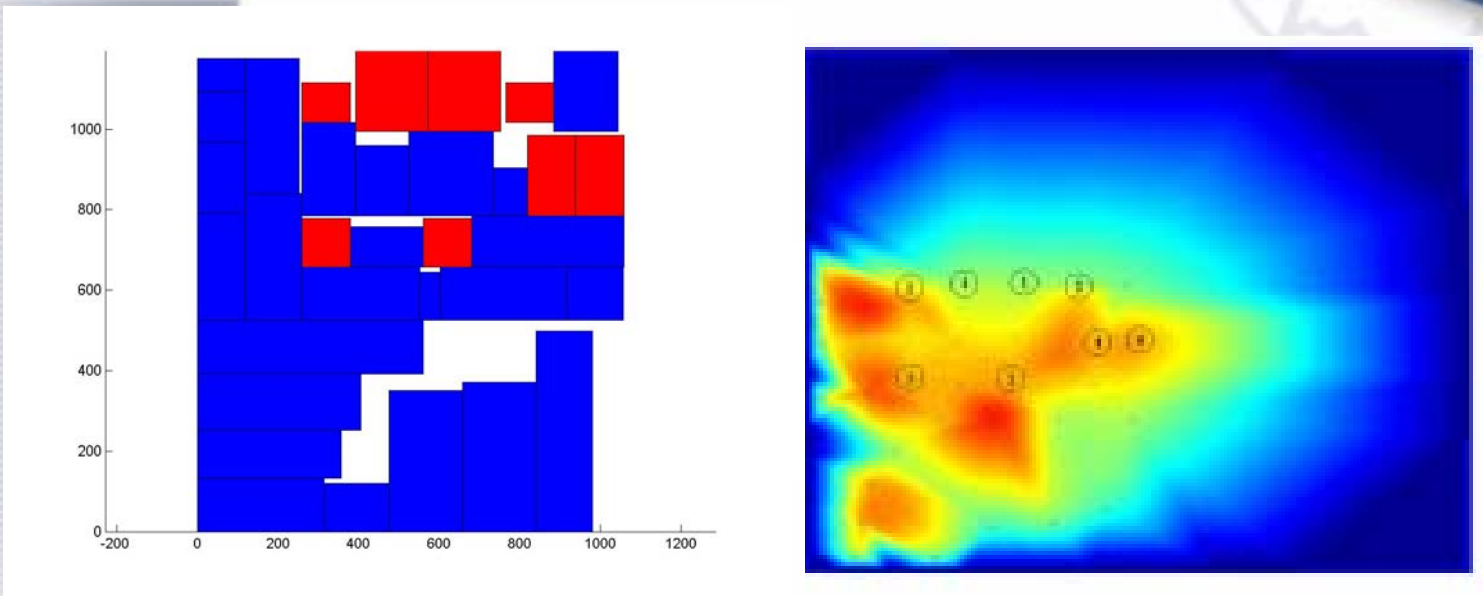


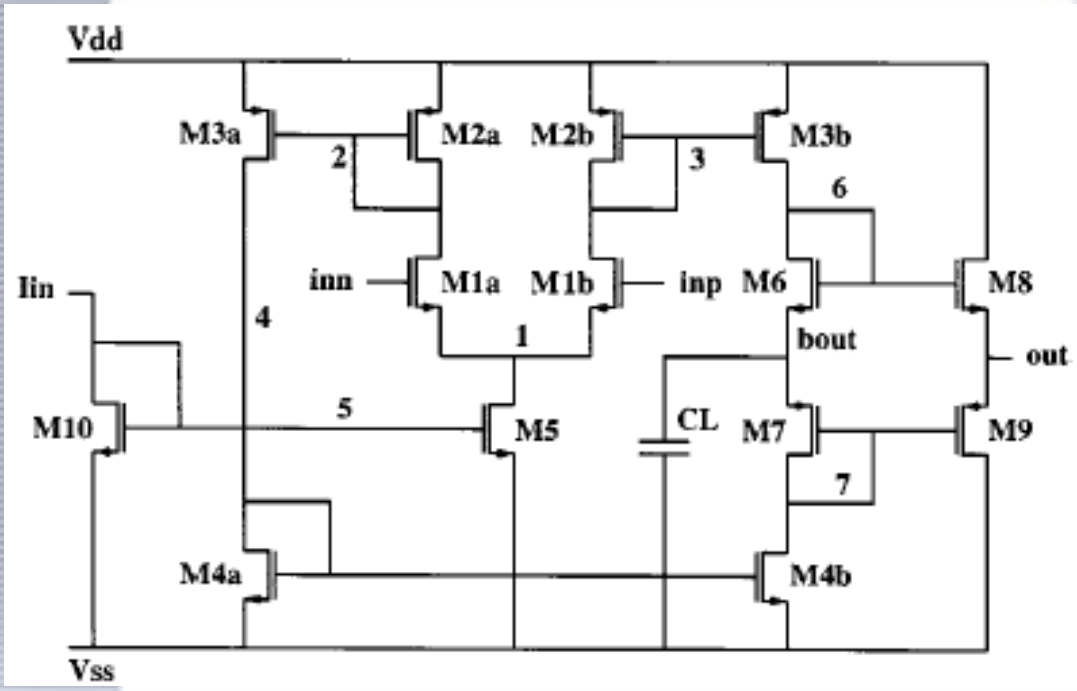
the planform of heat distribution for ami33

Multi-symmetry Axes



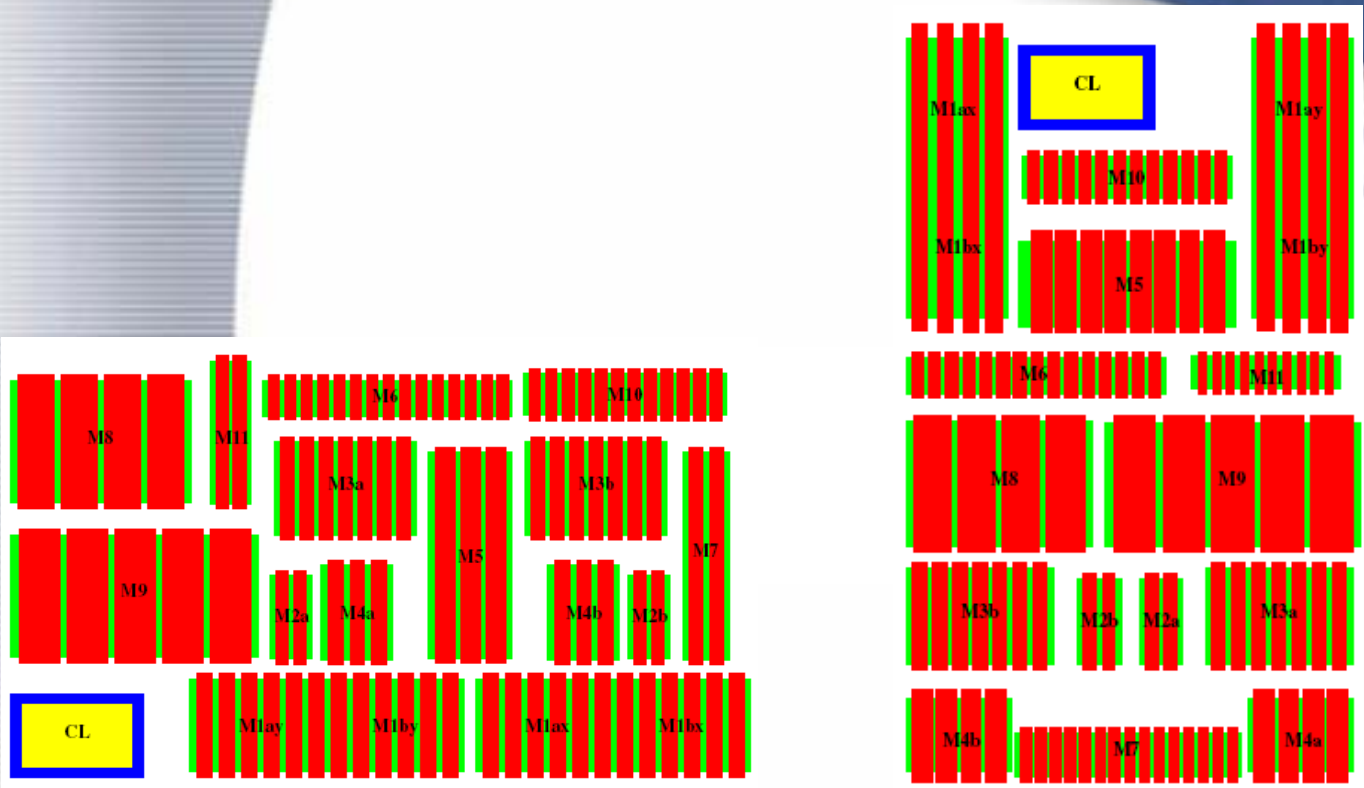
(a) Placement and of multi-symmetry axes
(b) Heat distribution of multi-symmetry axes

Analog Circuit Results



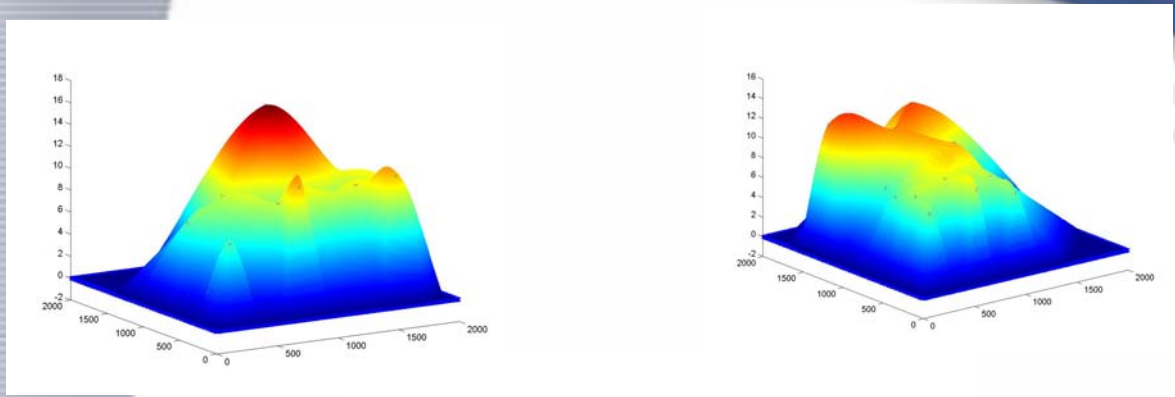
Schematic of a high-speed CMOS comparator

Placement of CMOS Comparator



(a) Layout with only symmetry constraint
(b) with both symmetry and thermal constraints

Heat Distribution



(a) Only with symmetry constraint;
(b) With both symmetry and thermal constraints

(a) Heat distribution planform with only symmetry
(b) both symmetry and thermal constraints

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Conclusions

- According to the analysis of thermal influence on matching/symmetry devices in analog circuit, it is clear that too high temperature on single device would cause performance failure and temperature gradient can affect the performance of symmetrical devices dramatically.
- Therefore, based on the traditional geometric symmetry constraint which is achieved with CBL representation for the first time, a thermal model is introduced to the placement process in order to decrease temperature gradient and avoid hot-spot.
- The final experimental results prove the effectiveness of our algorithm.

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