ASP-DAC 2007, YOKOHAMA
SESSION 2C.5
ANALOG CAD TECHNIQUES: FROM ANALYSIS TO VERIFICATION

STRUCTURED PLACEMENT WITH TOPOLOGICAL REGULARITY EVALUATION

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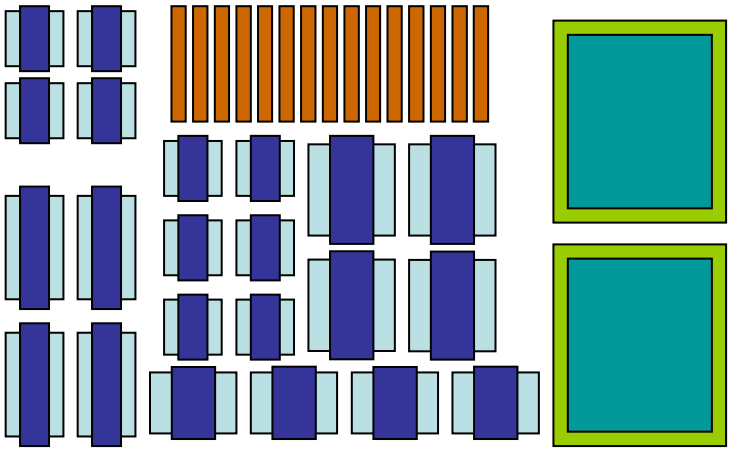
OUTLINE

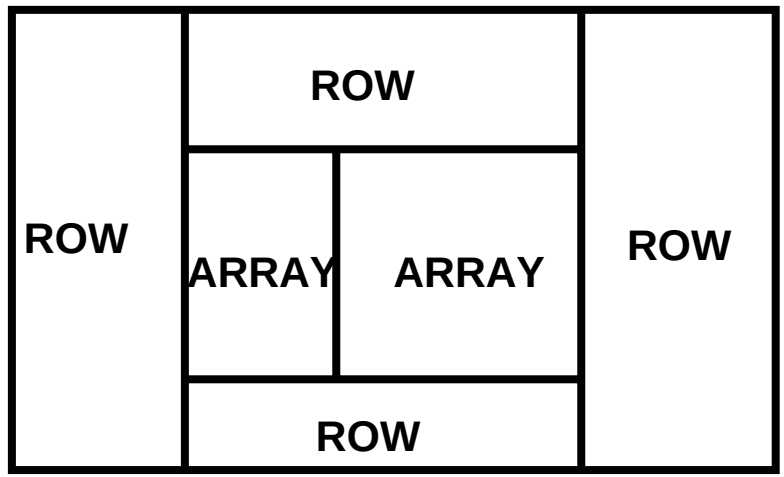
I. Analog Placement
II. Concept of Structured Placement
III. Extraction of Topological Regular Structure
IV. Evaluation of Regularity
V. Dual Simulated Annealing
VI. Experiments
VII. Conclusion

ANALOG PLACEMENT (1)

In analog placement,
human designers usually put REGULAR STRUCTURES into ROWS and ARRAYS



placement



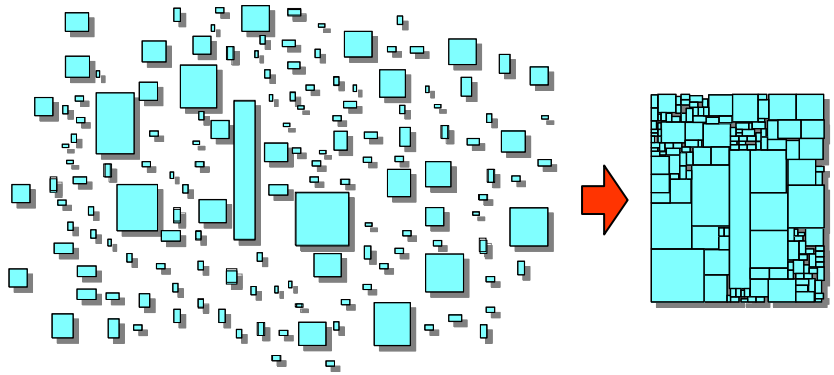
structure of placement

Typical analog placement has local regular structures
The regular structures serve high routability and suppression of variation on performances

ANALOG PLACEMENT (2)

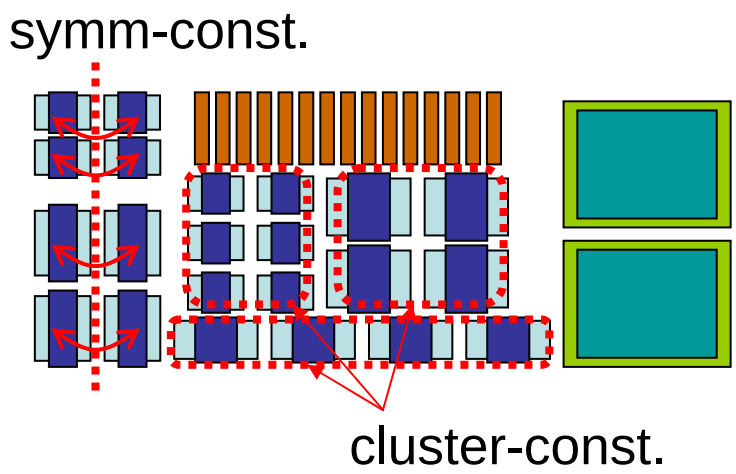
- **Rectangle Packing Approach**
  - Devices and blocks are regarded as rectangles
  - BSG, Sequence-Pair, O-tree, B*-tree, TCG-S can generate highly compacted placement

  BUT, less regularity



- **Constraint-Driven Approach**
  - Symmetry/Cluster constraint

  BUT, generation of constraint is still manual and time-consuming



Automation of analog placement is immature

STRUCTURED PLACEMENT

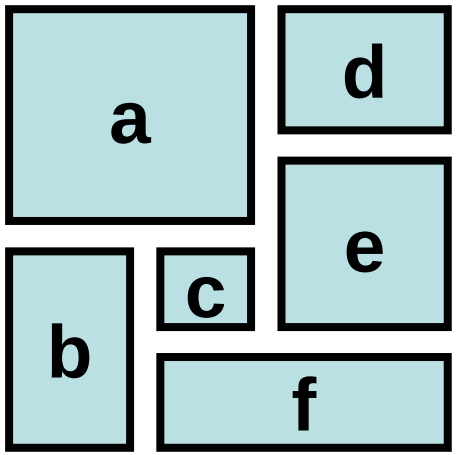
- **CONCEPT**
  - **Constraint-less**
  - **Naturally going** to a placement with many local regular structures such as arrays and rows
- **OUR APPROACH**
  - **Formulating topological regularity** that is extractable from a **sequence-pair**
  - **Evaluating the regularity** during optimization
  - **Separating topology** optimization and **physical dimension** optimization

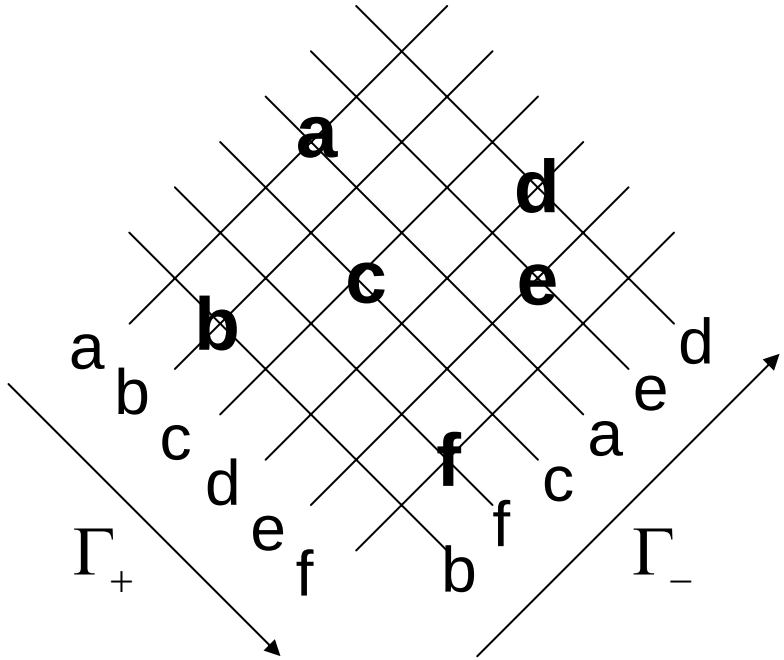
SEQUENCE-PAIR (*SP*)

Representation of Topology of Rectangle Placement [ICCAD'95]

Placement ***Sequence-Pair***

$$SP = (\Gamma_+, \Gamma_-) = (\text{abcdef}, \text{bfcaed})$$





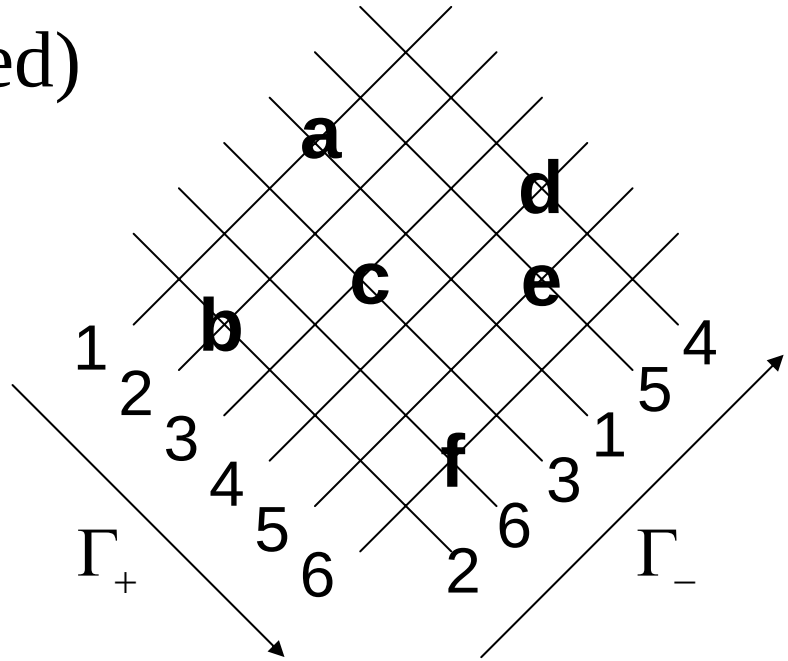
Oblique-Line-Grid: Equivalent Representation of SP

SINGLE-SEQUENCE (*S*)

Representation of **ONLY TOPOLOGICAL STRUCTURE** of Rectangle Placement [ISCAS'04]
(In a sense, *S* is standard representation of *SP*)

$$SP = (\Gamma_+, \Gamma_-) = (\text{abcdef}, \text{bfcaed})$$

$$S = 263154$$

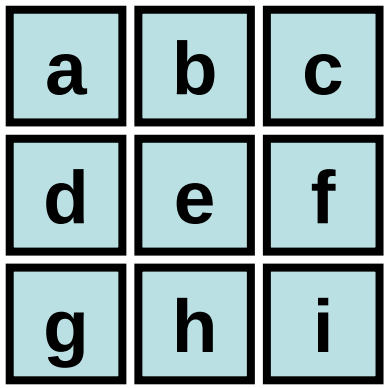


S is $\Gamma-$ when $\Gamma+ = 12345\cdots$

STRUCTURE IN TERMS OF *SP*

structure	*sequence-pair*	*single-sequence*

ARRAY

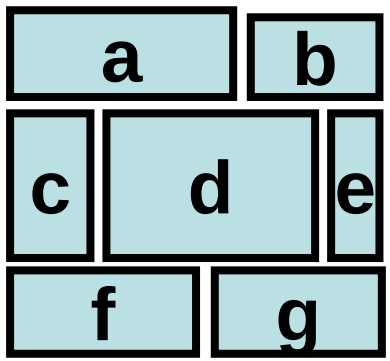


$\Gamma_+ = \text{abcdefghi}$

$\Gamma_- = \text{ghidefabc}$

$S = 789456123$

HORIZONTAL ROW



$\Gamma_+ = \text{abcdefg}$

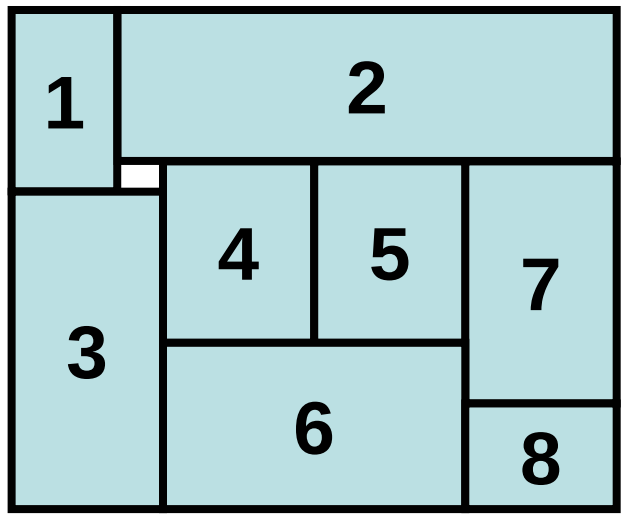
$\Gamma_- = \text{fgcdeab}$

$S = 6734512$

How to extract subsequences from *S* (or *SP*) corresponding to arrays or rows?

DEFINITION: RECTANGULAR EXTRACTABLE

- **Capturing local structure of placement as a subsequence of *S***
  - ***X*** is subsequence of single-sequence ***S***
  - ***X*** is **rectangular extractable**, if ***max(X)-min(X)+1=\|X\|***
- **Example**
  - Single-sequence:
    S=(3, 1, 6, 4, 5, 8, 7, 2)
  - Rectangular extractable sets:
    (4, 5), (6, 4, 5), (6, 4, 5, 8, 7), (3, 1, 6, 4, 5, 8, 7, 2)



DEFINITION: TOPOLOGICAL ROW AND ARRAY

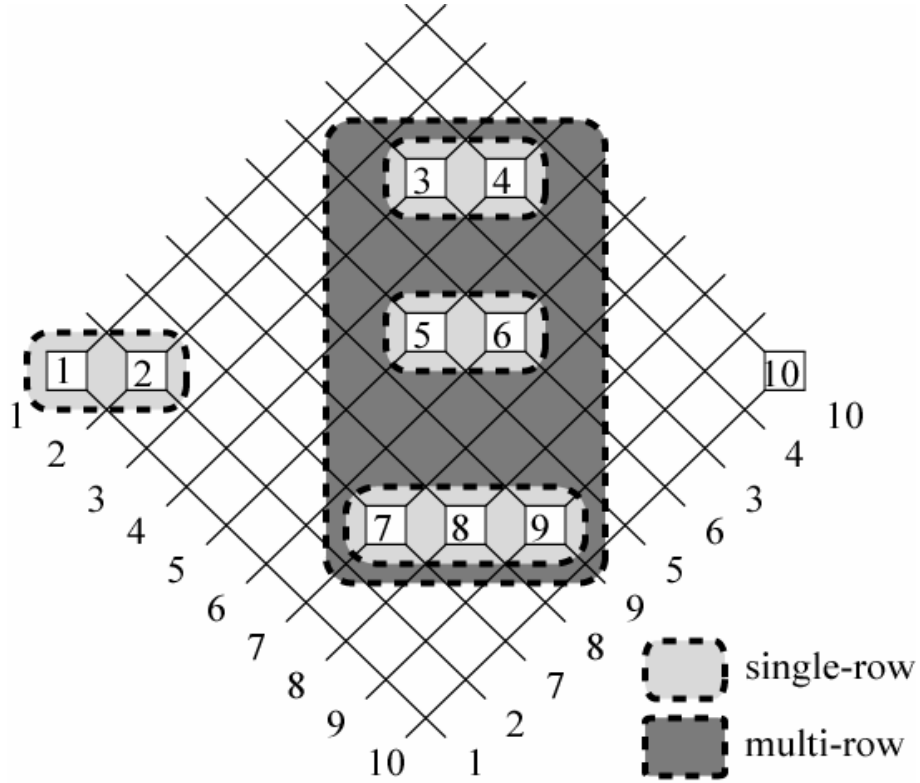
- **Horizontal Single Row**
  - subsequence $S_i=(s_1, .., s_k, s_{k+1}, \ldots)$ such that it is **rectangular extractable** and $s_{k+1}-s_k = 1$
- **Horizontal Multi-Row**
  - two or more horizontal single rows which can be stacked vertically
- **Array**
  - special multi-row each of which has the same length

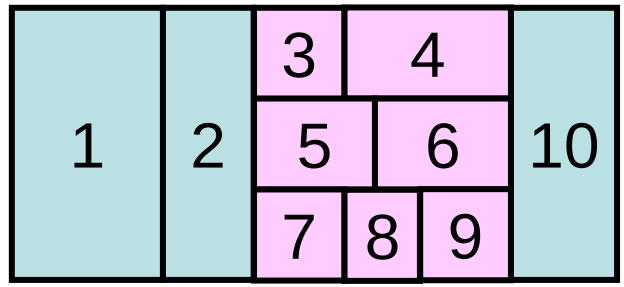
Theorem:

Given an SP, all multi-rows and arrays with maximal length in the SP can be extracted in O(n), where n is the number of blocks

EXTRACTION ALGORITHM OF TOPOLOGICAL ROW AND ARRAY

- **Divide** *S* into $S_1/S_2/\ldots/S_i/\ldots/S_l$ such that $S_{k+1}-S_k=1, S_{k+1}, S_k$ *in* S_i
  - *S=(1, 2, 7, 8, 9, 5, 6, 3, 4, 10)*
  - *(1,2)/(7, 8, 9)/(5, 6)/(3, 4)/(10)*
- **Calculate** *max and min*
  - $\{(min(S_i), max(S_i)\} = \{(1,2),(7,9),(5,6),(3,4),(10,10)\}$
- **Extract** vertical stackable pair S_i and S_{i+1} such that $min(S_i)-max(S_{i+1})=1$
  - *((7,8,9),(5,6)) and ((5,6),(3,4))*
- **Concatenate** two or more stackable pairs with common subseqs.
  - *((7,8,9),(5,6),(3,4))*





EVALUATION OF REGURARITY (1)

Evaluate a placement separating *topology* and *physical dimension*

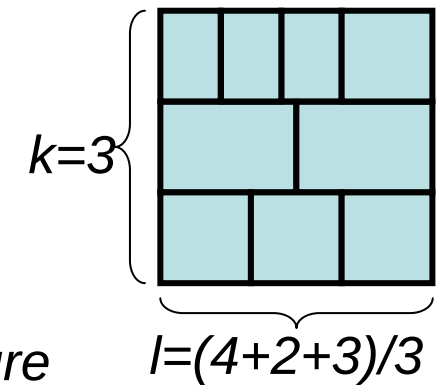
Cost function is designed by a combination of *topological structure value* and *physical dimension cost*

Topological Structure Value

$$V_{top} = \alpha \bullet \sum_{r \in R} \sigma(r) + \beta \bullet \sum_{a \in A} \sigma(a)$$

R is a set of multi-rows, A is a set of arrays

$\sigma(r) = \min(k,l) / \max(k,l)$ *if r has k x l structure*



EVALUATION OF REGURARITY (2)

Physical Dimension Cost

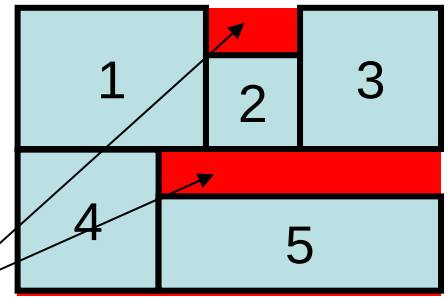
$$C_{phy}(r) = \alpha' \bullet \sum_{a \in A} (C_{cmp}(a) + C_{uni}(a)) + \beta' \bullet \sum_{r \in R} (C_{cmp}(r) + C_{uni}(r))$$

R is a set of multi-rows, A is a set of arrays

Local Compactness Cost

$$C_{cmp}(r) = \max_i \sum_j (w(r_{i,j})) \bullet \sum_i \max_j (h(r_{i,j})) - \sum_{i,j} a(r_{i,j})$$

$r_{i,j}$ is a horizontal multi-row

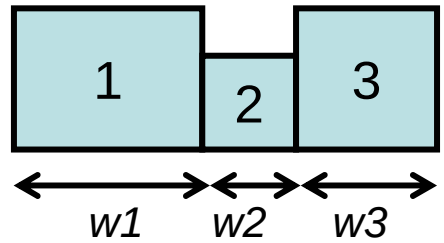


local compactness cost

Local Uniformity Cost

$$C_{uni}(r) = \sum_i (\max_j (w(r_{i,j}) - \min_j (w(r_{i,j}))))$$

$r_{i,j}$ is a horizontal multi-row

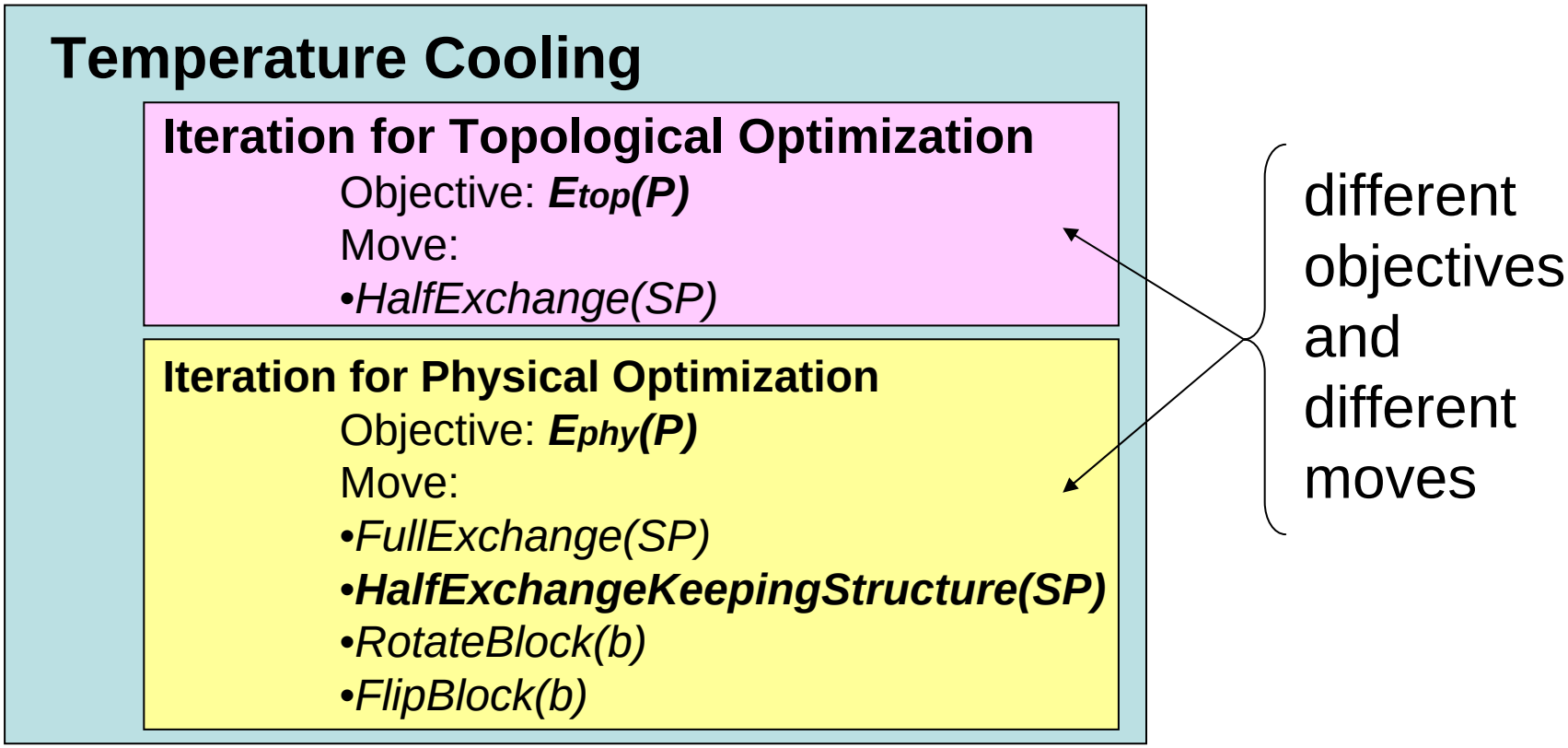


local uniformity cost = max(w1,w2,w3)-min(w1,w2,w3)

OPTIMIZTION: DUAL SIMULATED ANNEALING

Optimizing topological and physical objectives separately and alternately at step of each temperature

Optimization Framework (Input: Initial *SP*)



OBJECTIVES IN DUAL-SA

For topological optimization

$$E_{top}(P) = \frac{F(P)}{g(V_{top}(S))}$$

For physical optimization

$$E_{phy}(P) = F(P) \bullet g(C_{phy}(SP))$$

P: placement
S: single-sequence
SP: sequence-pair

F(P): primary objective such as chip area or wire length

$$g(x) \in [1.0, 1.1)$$

Ex. $g(x) = 1.0 + 0.1\exp\left(\frac{-x_m \log(0.5)}{x + \varepsilon}\right)$

xm is average of *{x}*

Note: Meaning of *g* is to be likely to degrade *F(P)* by 10% to obtain better *Vtop* or less *Cphy*

MOVE IN DUAL-SA

- **For Topological Optimization**
  - **HalfExchange(*SP*):** pair-interchange of blocks on either sequence of *SP*
- **For Physical Optimization**
  - **FullExchange(*SP*):** pair-interchange of blocks on both sequences of *SP*
  - **HalfExchangeKeepingStructure(*SP*):** pair-interchange of **subseqs** on either sequence of *SP*, where the **subseqs** correspond to multi-rows or arrays that are **rectangular extractable**
  - RoateBlock(*b*)
  - FlipBlock(*b*)

EXPERIMENTS: AREA V.S. STRUCTURE (1)

F(P) = chip area

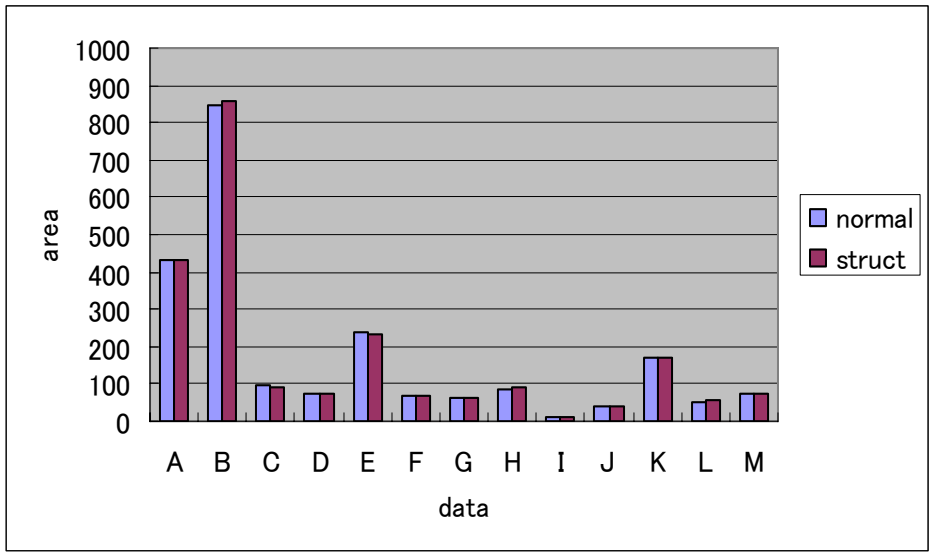
Numerical Data and Results

data	# blocks	# nets	normal		struct		area ratio
			area (μm^2)	str-cover (%)	area (μm^2)	str-cover (%)	struct/normal
A	23	44	432,876	9 (%)	432,595	96 (%)	1.00
B	53	90	848,114	0 (%)	857,419	96 (%)	1.01
C	122	91	98,868	5 (%)	93,720	72 (%)	0.95
D	60	46	75,078	17 (%)	75,594	87 (%)	1.01
E	113	80	238,392	4 (%)	235,128	68 (%)	0.99
F	32	22	65,367	19 (%)	68,150	69 (%)	1.04
G	54	49	63,248	15 (%)	64,904	72 (%)	1.03
H	90	58	87,870	9 (%)	88,960	77 (%)	1.01
I	60	36	10,265	3 (%)	10,192	82 (%)	0.99
J	101	78	39,619	5 (%)	40,591	84 (%)	1.02
K	66	29	168,866	12 (%)	170,990	79 (%)	1.01
L	64	49	53,710	0 (%)	54,108	88 (%)	1.01
M	166	105	72,945	5 (%)	71,714	49 (%)	0.98

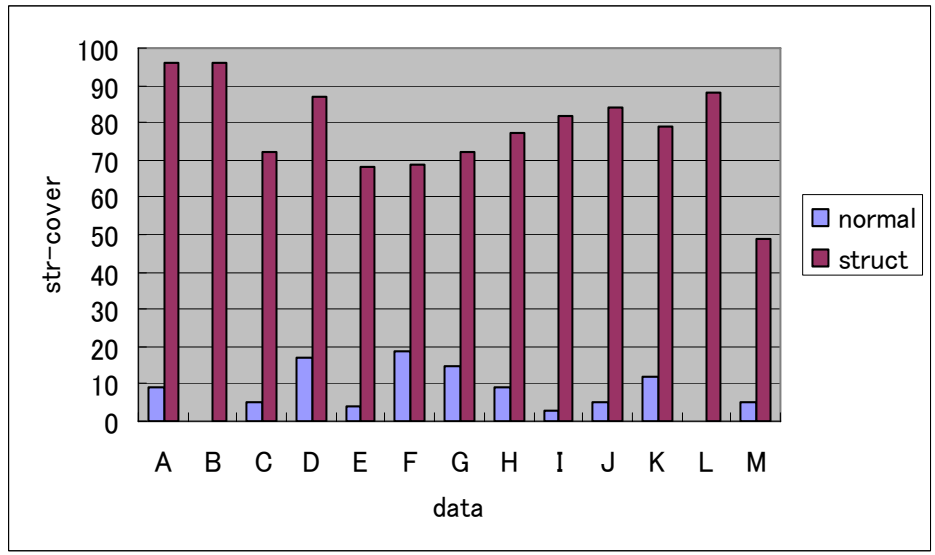
normal: normal placement
struct: our structured placement
str-cover: structure coverage ratio that is number of blocks composing topological arrays or rows by total number of blocks

EXPERIMENTS: AREA V.S. STRUCTURE (2)

w.r.t. chip area



w.r.t. str-cover



On average
area ratios(normal/struct) is **1.003**
- *str-cover* of *normal* is **7.9%**
- str-cover of *struct* is **73.5%**

EXPERIMENTS: AREA V.S. STRUCTURE (3)

data A: normal

data A: struct

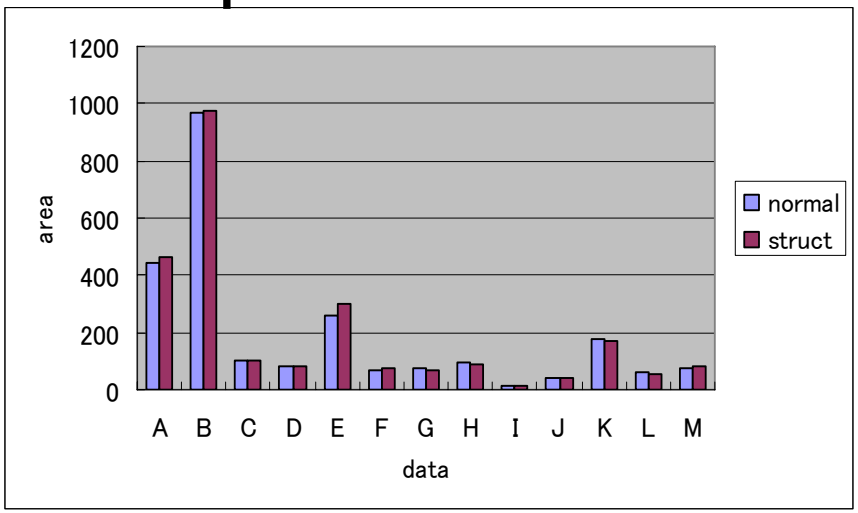
EXPERIMENTS: AREA*WIRE LENGTH V.S. STRUCTURE (1)

F(P) = chip area*wlre length

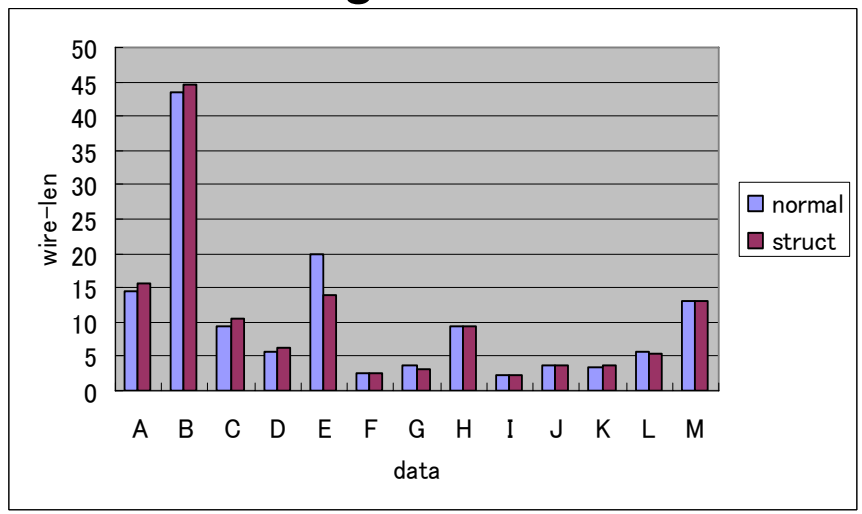
data	normal			struct			area*wire-len ratio
	area (μm^2)	wire-len (μm)	str-cover (%)	area (μm^2)	wire-len (μm)	str-cover (%)	struct/normal
A	444,566	14,488	26 (%)	463,810	15,717	87 (%)	1.13
B	970,759	43,554	11 (%)	973,116	44,693	71 (%)	1.03
C	104,895	9,326	5 (%)	99,231	10,612	64 (%)	1.08
D	81,073	5,794	17 (%)	79,605	6,250	62 (%)	1.06
E	261,332	19,926	7 (%)	296,800	13,985	73 (%)	0.80
F	67,680	2,632	13 (%)	72,380	2,491	91 (%)	1.01
G	72,192	3,750	15 (%)	68,906	3,241	87 (%)	0.82
H	97,280	9,412	9 (%)	89,694	9,249	66 (%)	0.91
I	10,779	2,413	7 (%)	10,554	2,205	78 (%)	0.89
J	41,800	3,695	2 (%)	40,460	3,779	71 (%)	0.99
K	173,870	3,529	3 (%)	173,040	3,620	64 (%)	1.02
L	58,629	5,603	9 (%)	57,002	5,361	83 (%)	0.93
M	77,451	12,997	1 (%)	80,575	13,126	58 (%)	1.05

EXPERIMENTS: AREA*WIRE LENGTH V.S. STRUCTURE (2)

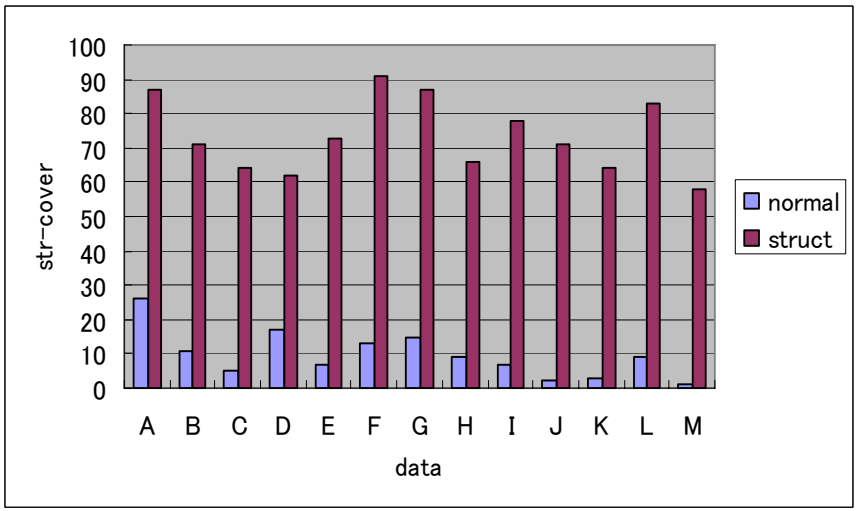
w.r.t. chip area



w.r.t. wire length



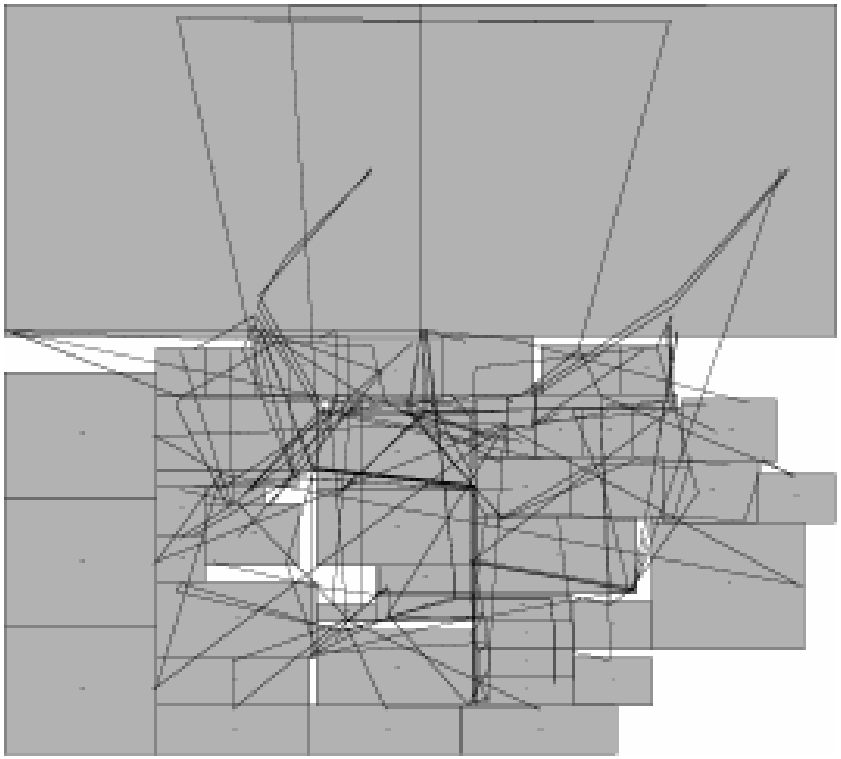
w.r.t. str-cover



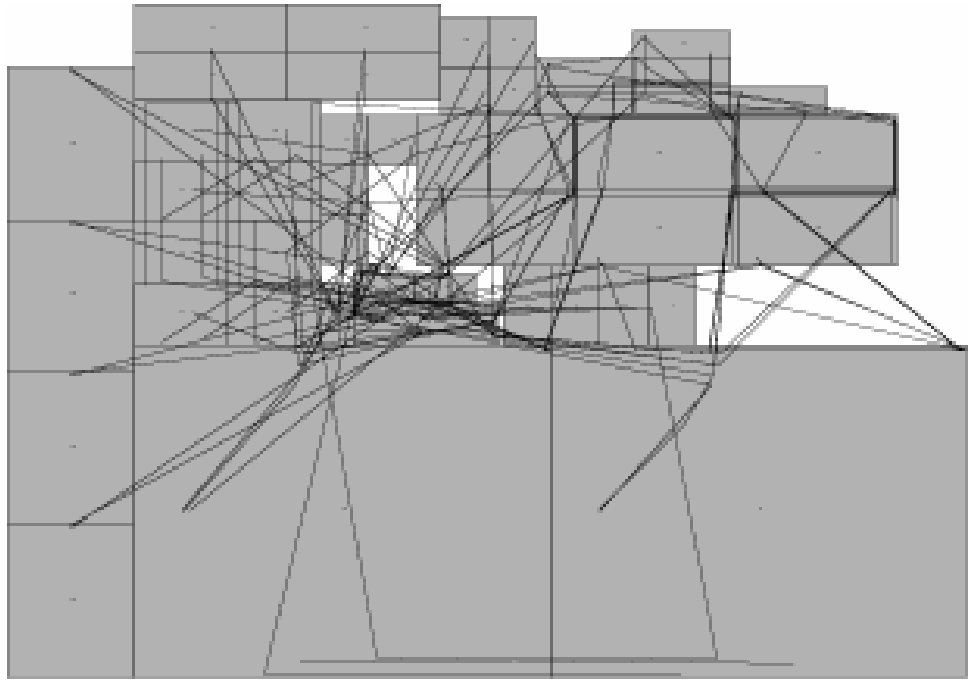
On average,

- *area*wire-len ratio (normal/struct)* is **0.978**
- *str-cover* of *normal* is **9.6%**
- str-cover of *struct* is **73.5%**

EXPERIMENTS: AREA*WIRE LENGTH V.S. STRUCTURE (3)



data B: normal



data B: struct

CONCLUSION

- *New Concept for Analog Placement*: **structured placement** that makes use of the regularity of topological structure as a key criterion
  - Constraint-less
  - Naturally going to a placement with many local regular structures such as arrays and rows
- *Our Structured Placement*:
  - **Extraction** and **evaluation** of topological regular structure such as **arrays and rows**
  - **Dual simulated annealing** optimizes topology and physical dimension separately
- *Future Works*:
  - Extraction and evaluation of **symmetry structure** and **hierarchical regular structure**
  - Further **practical extension**

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THANK YOU!