Modeling Sub-90nm On-Chip Variation Using Monte Carlo Method for DFM

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Outline

- Random vs. systematic BEOL variations
- BEOL profile based random variations
- Monte Carlo (MCGRC) simulations
- 2-dimensional capacitances
- 3-dimensional capacitances
- Validating corners for SSTA
- Conclusion

Random vs. Systematic BEOL Variations

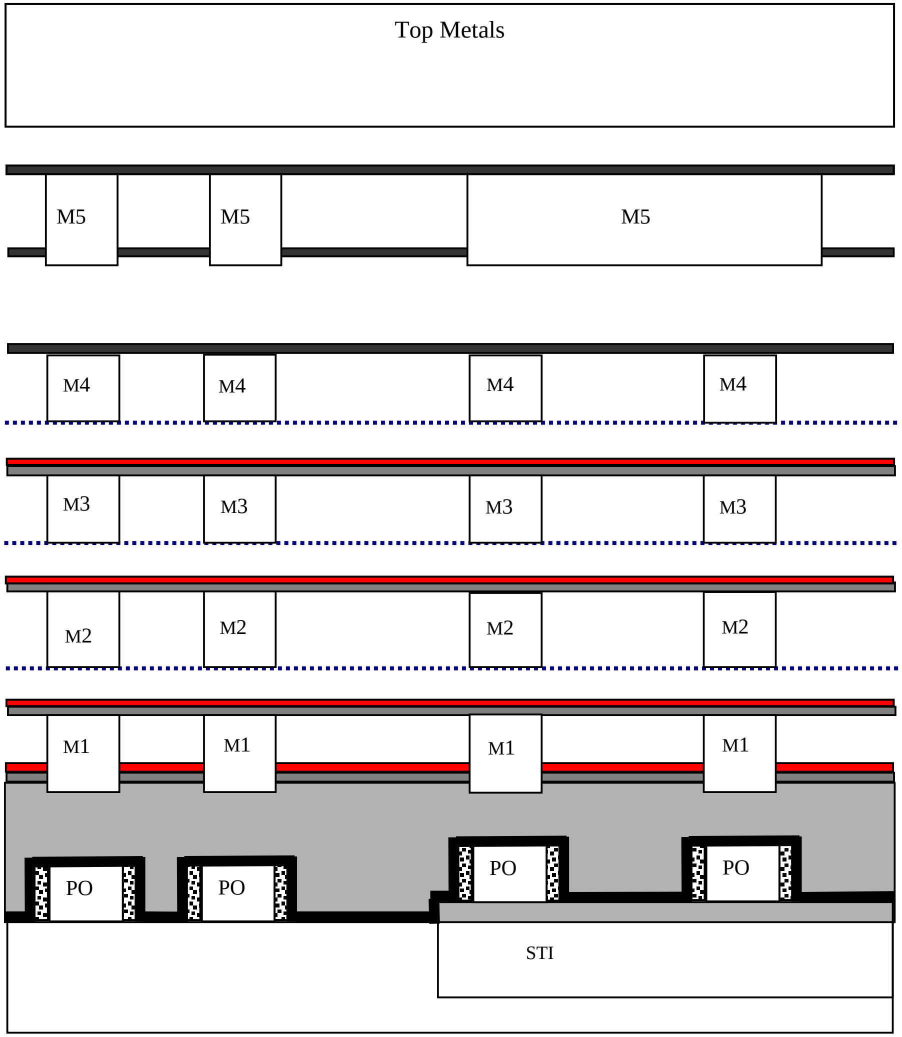
- **BEOL profiles are the geometrical dimensions and material properties of the “back-end of the line,” i.e. the interconnects.**
- **Systematic variations, deterministic in nature, with a varying trend and pattern of BEOL profiles**
  - **Methods to correctly include OPC, dummy fill, etc.**
- **Random variations, a stochastic phenomenon without a clear trend or pattern of BEOL profiles**
  - **Statistical modeling and timing closure for chip designs.**

Ref. [1] [2]

Targeting BEOL Random Variations

- Replicating structures with identical environments;
- Avoiding systematic variations;
- Avoiding spatial variations;
- Avoiding measurement noises;
- Concentrating on on-chip variations.

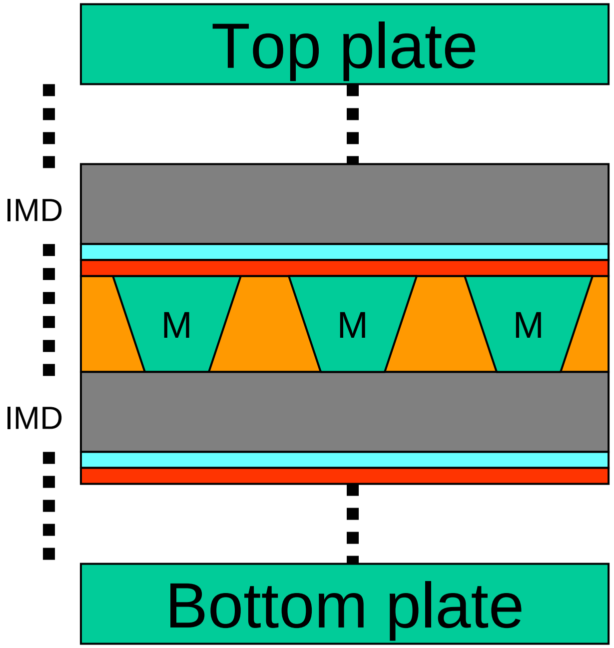
Profiling the Cu-Based Node



Source: Unpublished TSMC 2001 document

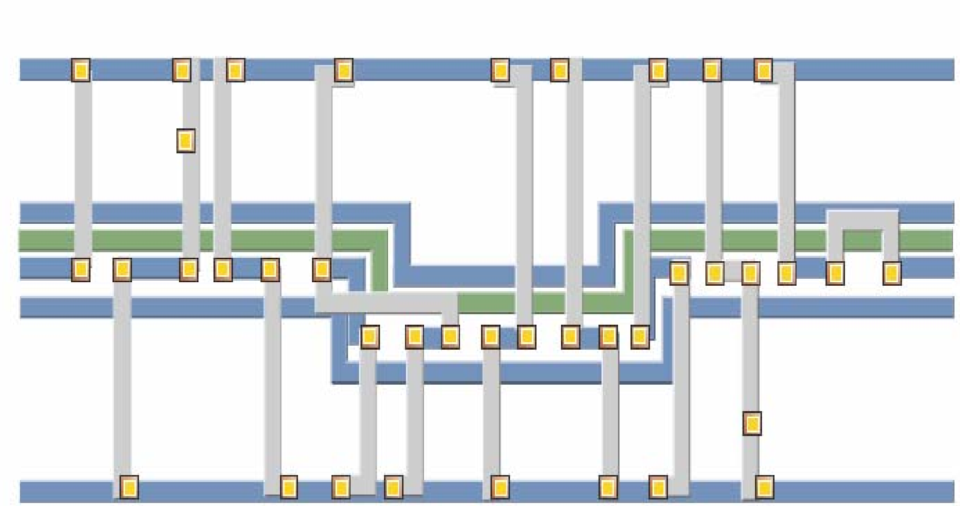
Monte Carlo (MCGRC) Simulations

- **Random parameters of BEOL profiles that affect capacitance and resistance： (-3 σ ~ +3 σ)**
  - **Top and bottom plates/grids thickness plus pitch when 3D**
  - **Metal signal lines' thickness and pitch**
  - **Thickness / ε_r of IMD between top and bottom plates**



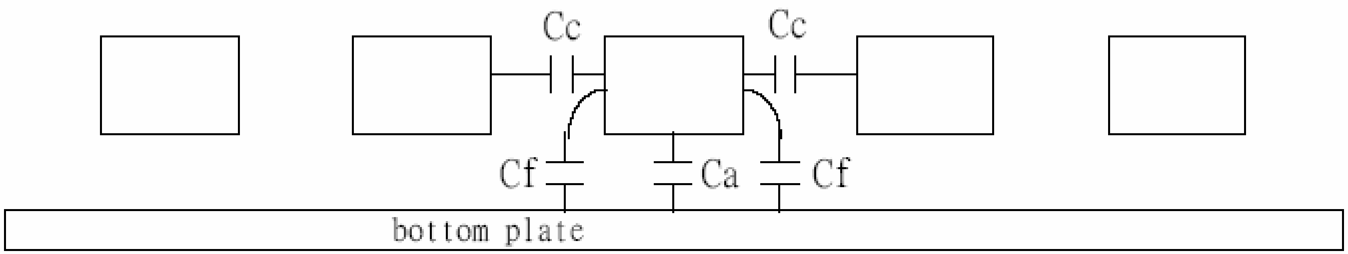
Three Main Experimental Structures

- Dense 2-D RC structures
  - Signal lines between two adjacent plates
- “Sparse” 2-D RC structures
  - Signal lines between two far-away plates
- 3-D structures
  - ASIC-style real 3-D lines in 3-D environments

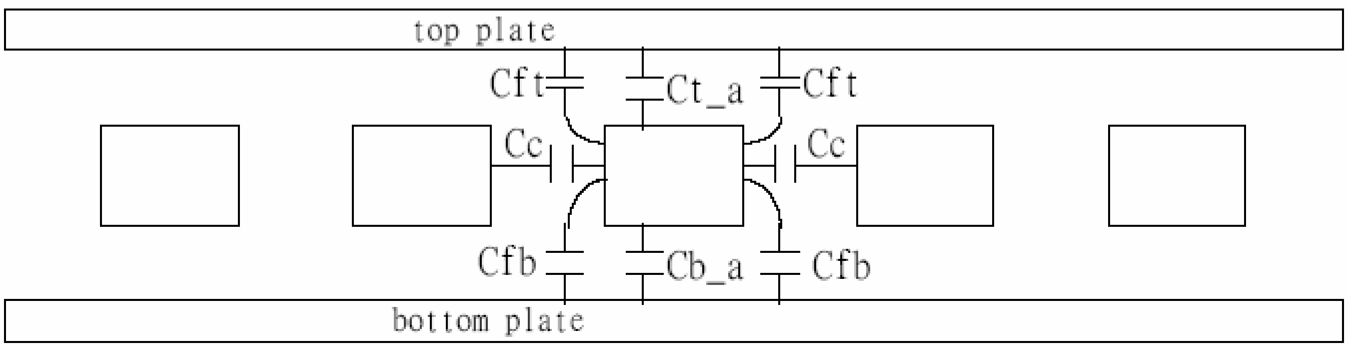


2-Dimensional Capacitances

Structure A - Conductors array above an infinite plate:



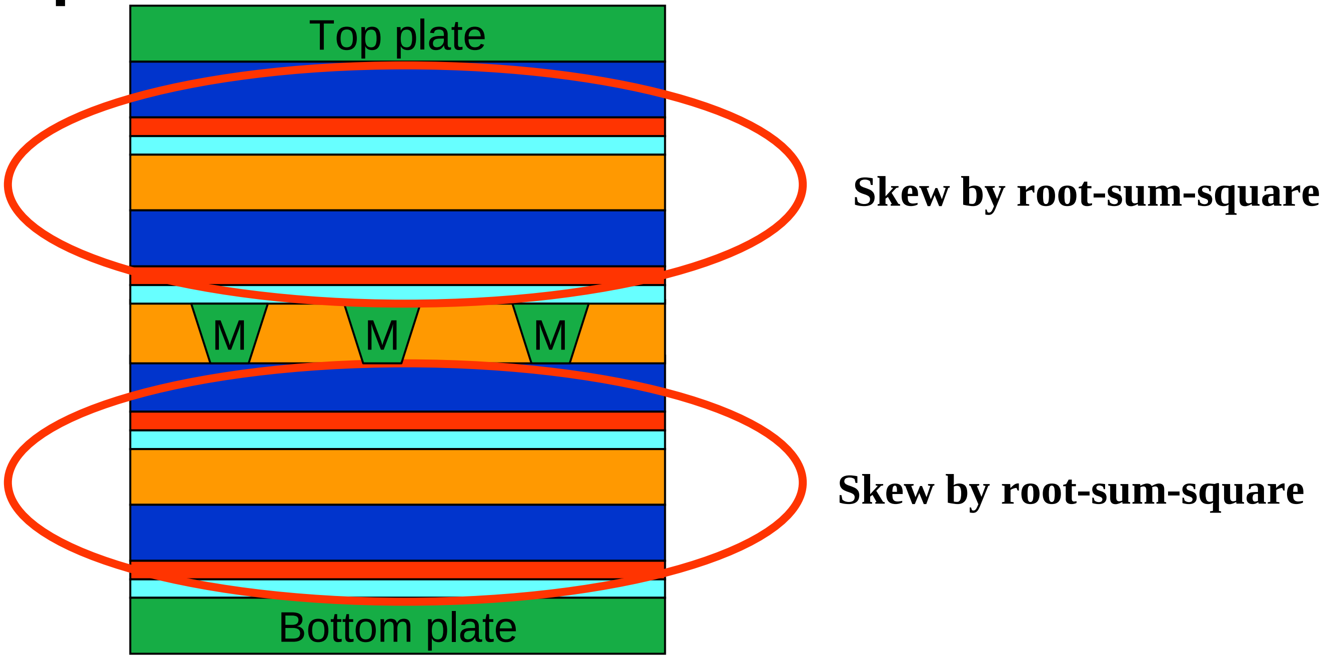
Structure B - Conductors array between two infinite plates:



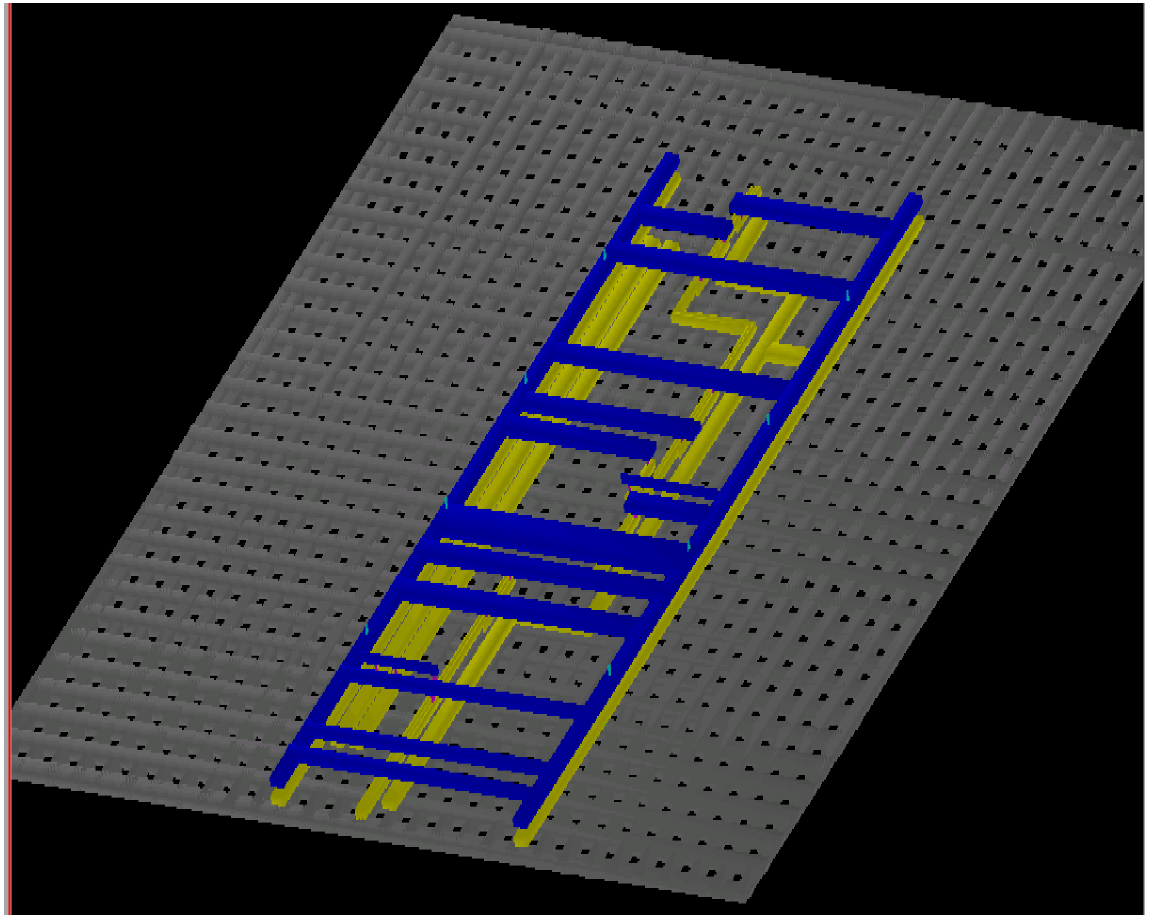
Source: Unpublished
TSMC 2001 document

RSS of BEOL Profiles for MCGRC

- **Skew all IMD between the top plate and the lines based on RSS**
- **Skew all IMD between the lines and the bottom plate based on RSS.**

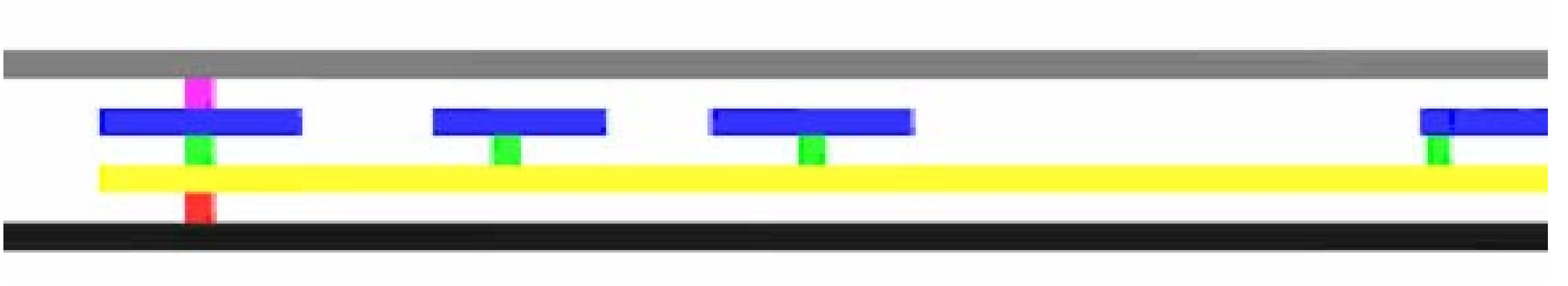


A 3-Dimensional Structure



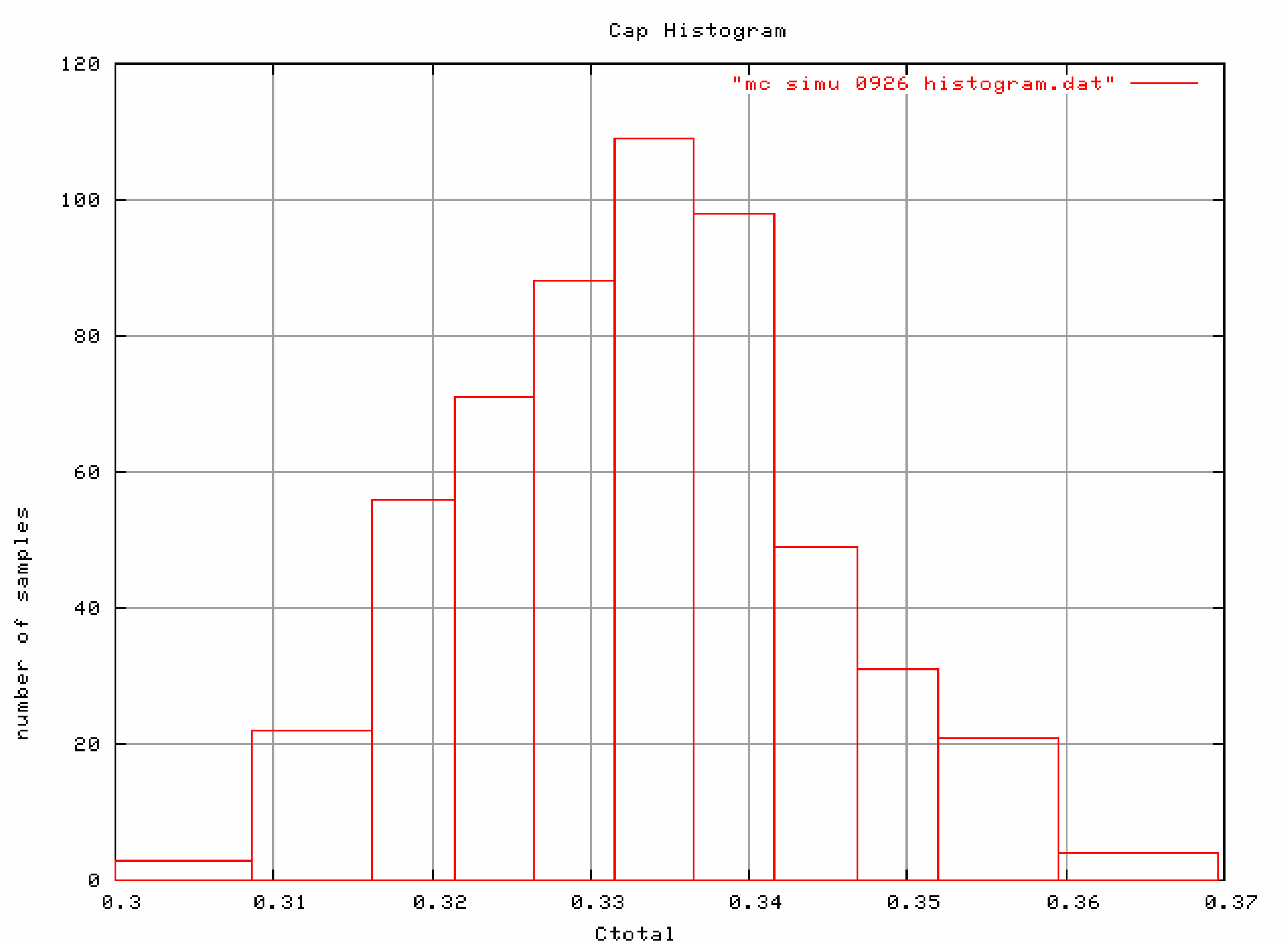
Ref: [4]

The Cross Section of the 3-D Structure

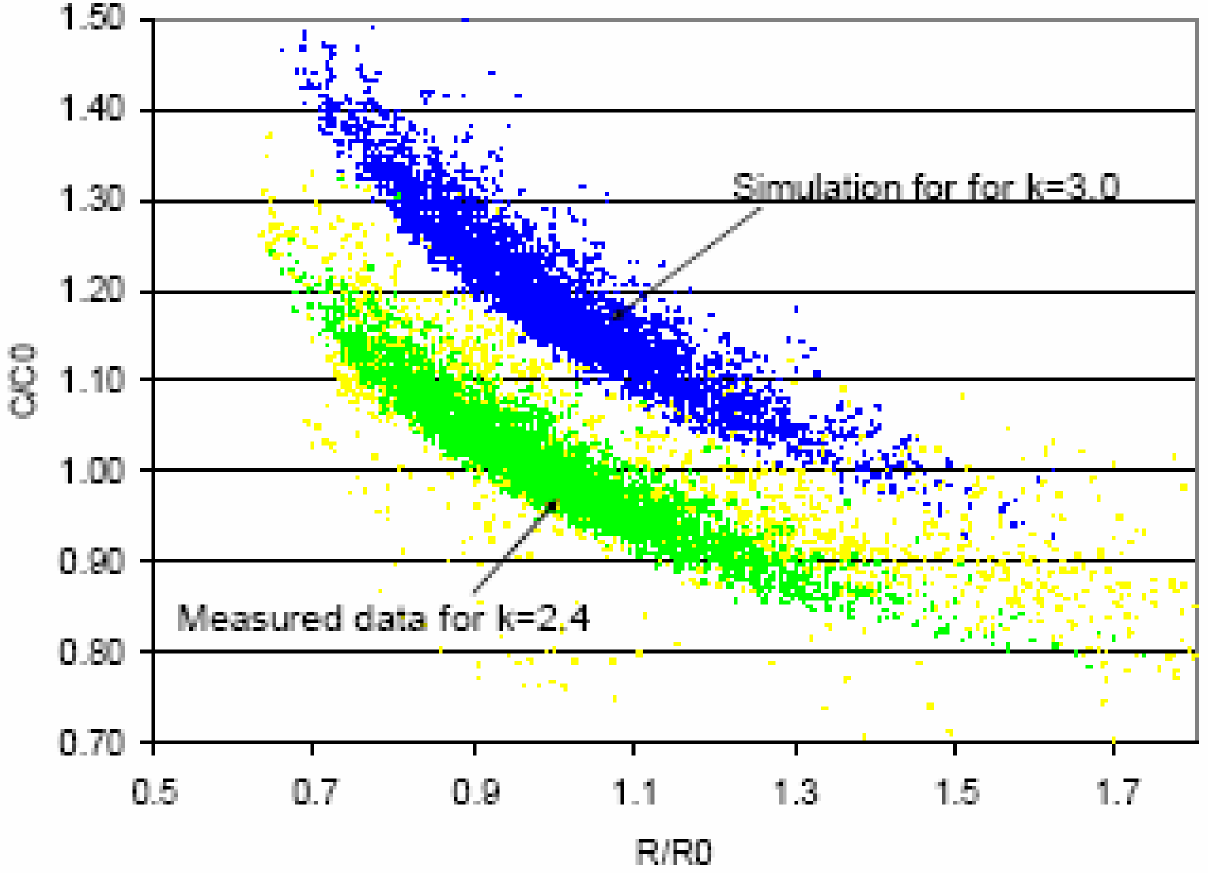


Note: M_{i-1}, M_i, M_{i+1}, M_{i+2}, and the surrounding IMD layers are all 3-D and their profiles are varying.

3-D Random Capacitance Variations

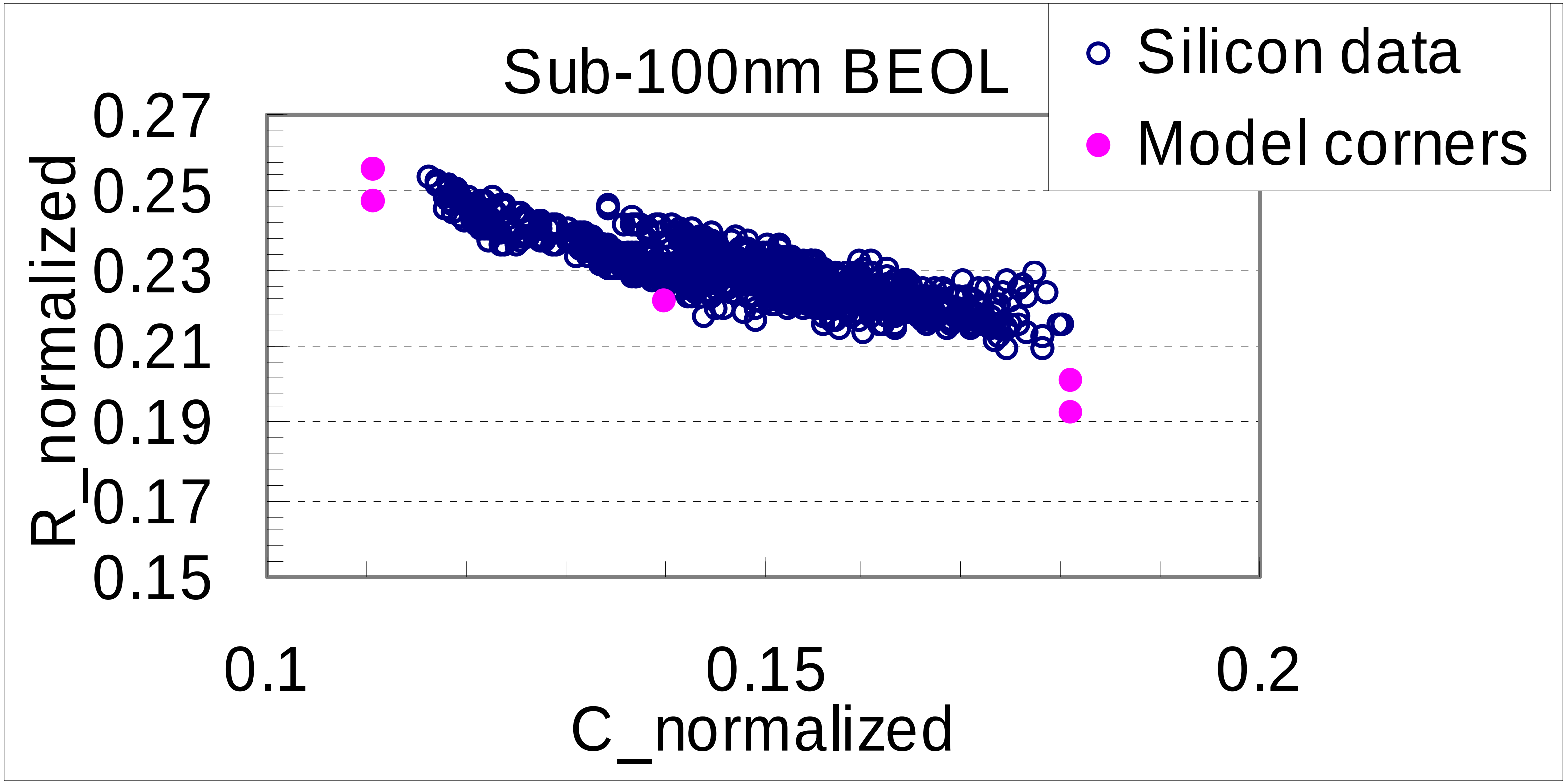


Recently Published BEOL Variations

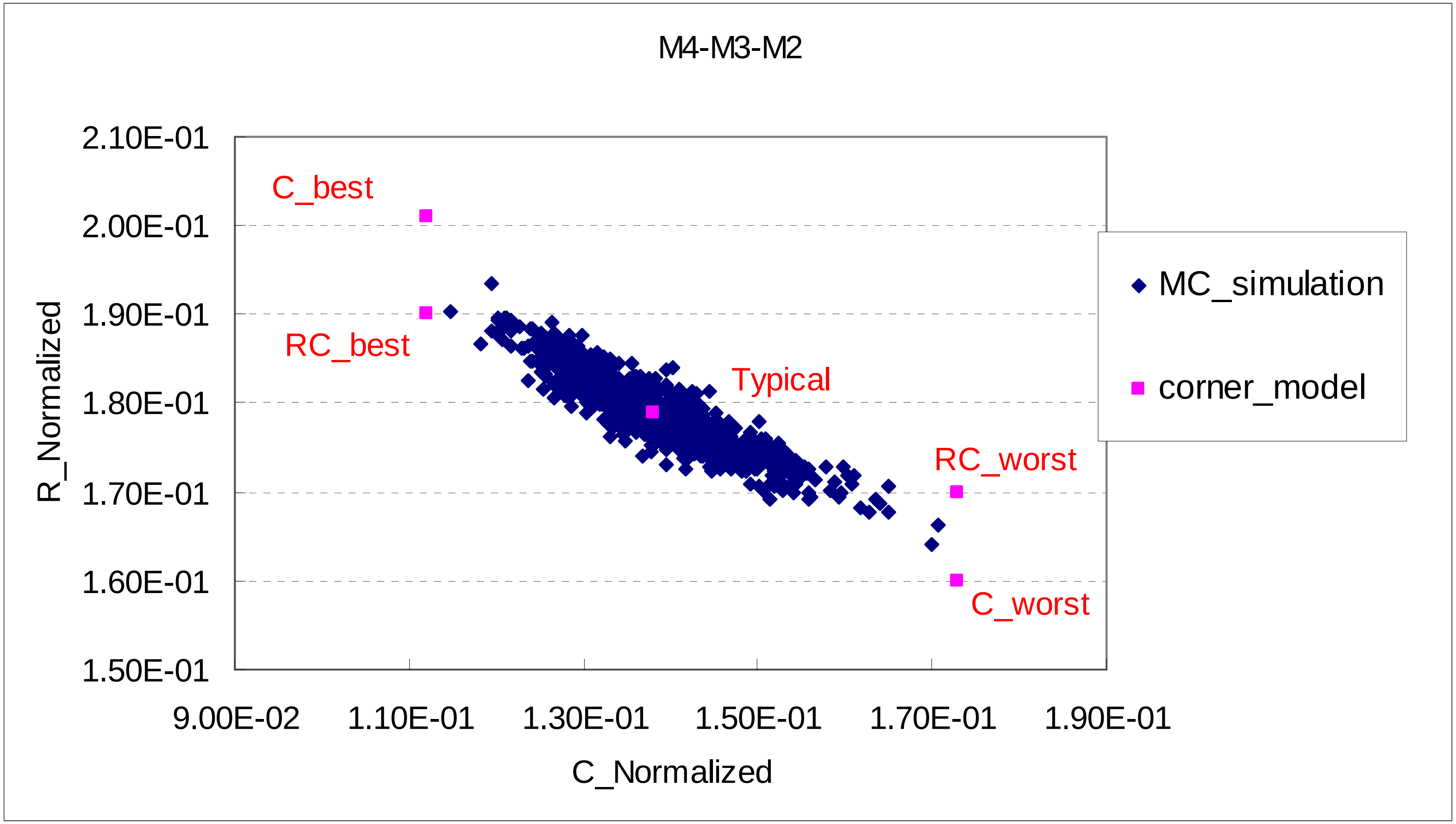


Ref. [3]

Measured BEOL Variation Patterns

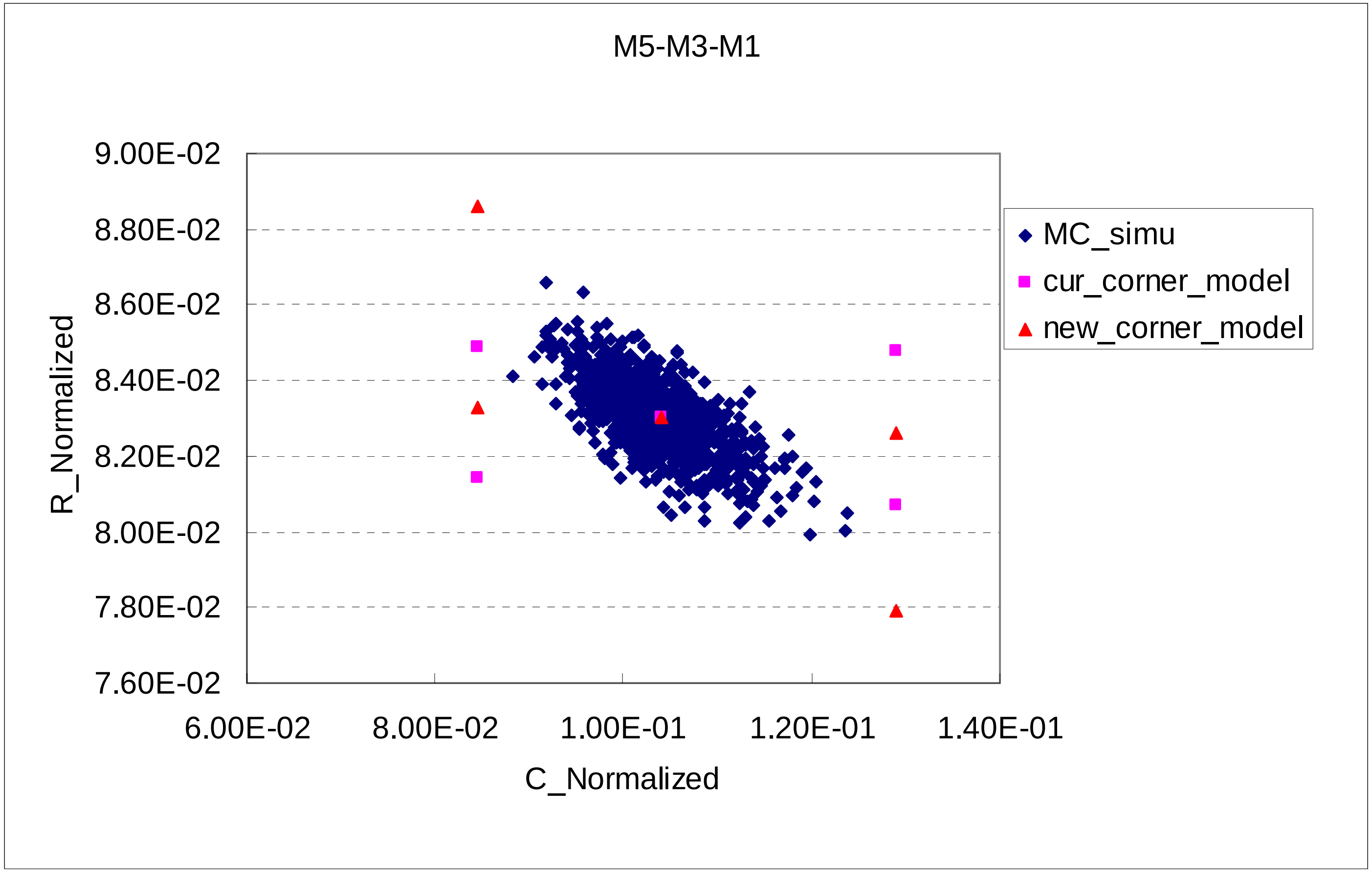


MCGRC BEOL Variation Patterns



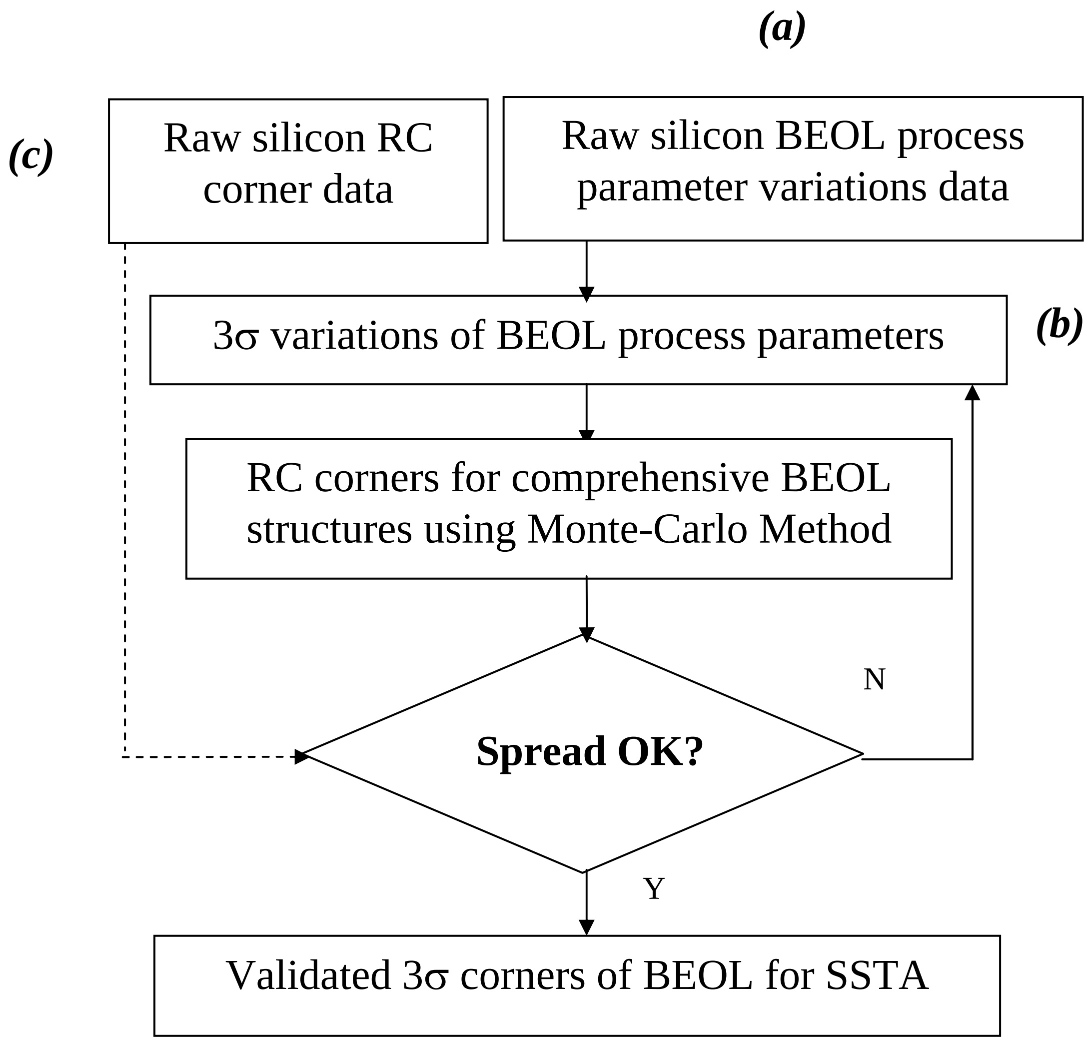
Note: The above should replace Figure 10 of Page 224, ASPDAC07.

Revising Our Corner Models

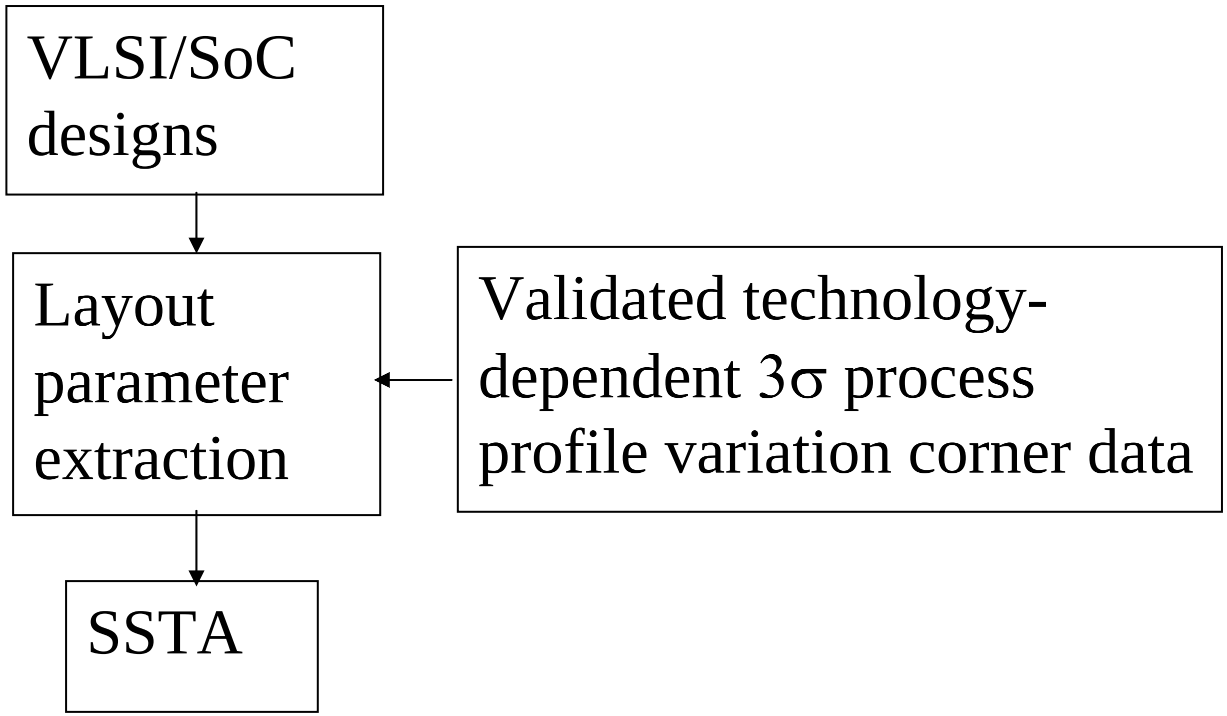


The above revision happens for sparse and wide metals.

Our Method Leading to SSTA



Validating Corners for SSTA



Conclusion

- **Successful Monte-Carlo Guided RC Simulations help revise RC corners for sparse and wide metals**
- **New high-throughput servers help the MCGRC performance and help save test chip designs and costs**
- **Extracted random variations can be used for SSTA for DFM.**

References

[1] K. Chang, "Accurate onchip variation modeling to achieve design for manufacturability." *Proc. 4th IEEE IWSOC*, Banff, 2004.

[2] J. Xiong *et al*., "Robust extraction of spatial correlation," *Proc. IEEE ISPD*, San Jose, 2006.

[3] S. Sankaran *et al*., "A 45 nm CMOS node Cu/Low-k/Ultra Low-k PECVD SiCOH (k=2.4) BEOL technology," *Proc. IEEE IEDM*, San Francisco, 2006.

[4] TSMC, *Foundry Watch*, Hsinchu, April 2002.