

DFM reality in Sub-Nanometer IC Design

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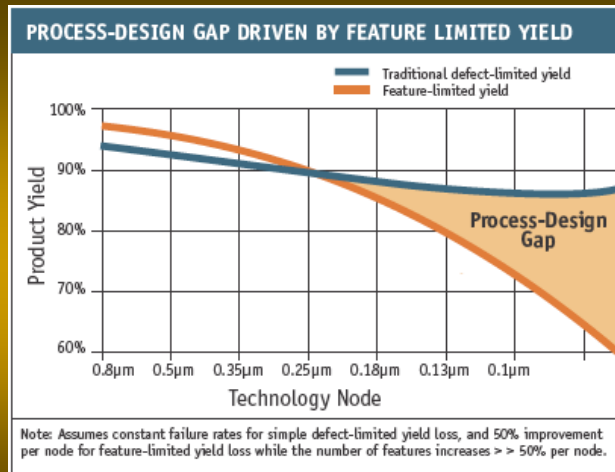
Move from ideal-GDSII to
Model based Silicon Accurate Design



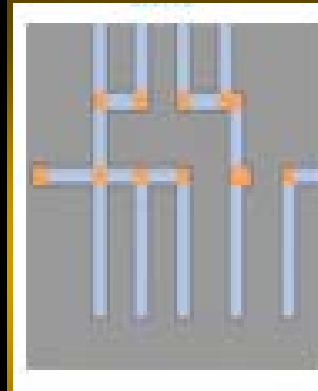
Outline of DFM reality in Sub-Nanometer IC Design

- ◆ 65nm Technology Trends
- ◆ Addressing 65nm Challenges during Design
- ◆ Summary

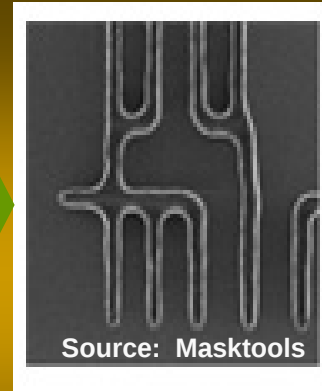
Sub-Nanometer Failures Cause Systematic Yield Loss



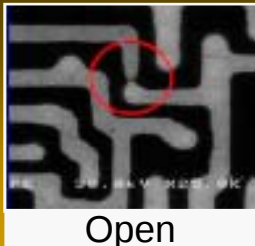
Systematic Yield is now Dominant



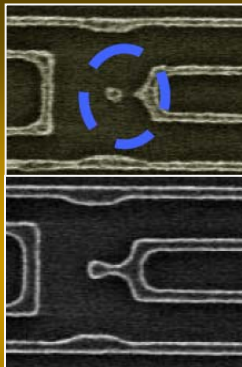
RET+
MFG.



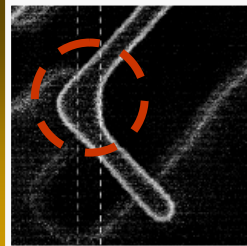
What you design is NOT
what you print on Silicon



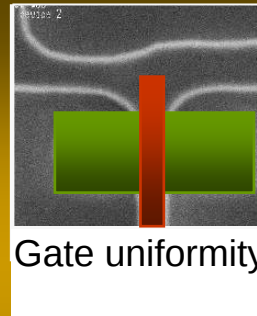
Open



Open across PW



Catastrophic
failure due to
flaring

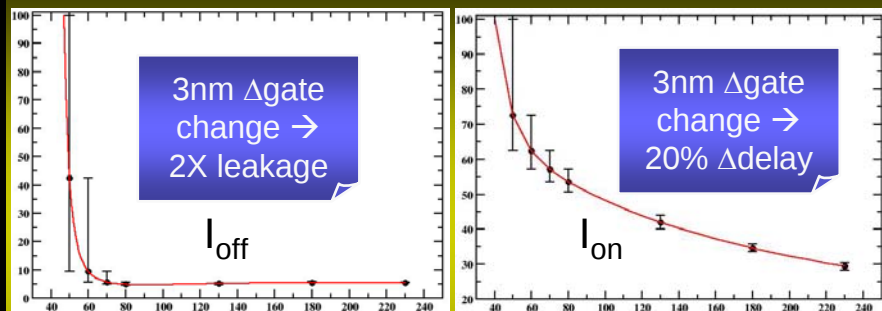


Gate uniformity

- ◆ DRC is not sufficient anymore
- ◆ Risk costly respins or poor utilization of process
- ◆ Need to design tools to prevent catastrophic systematic failures

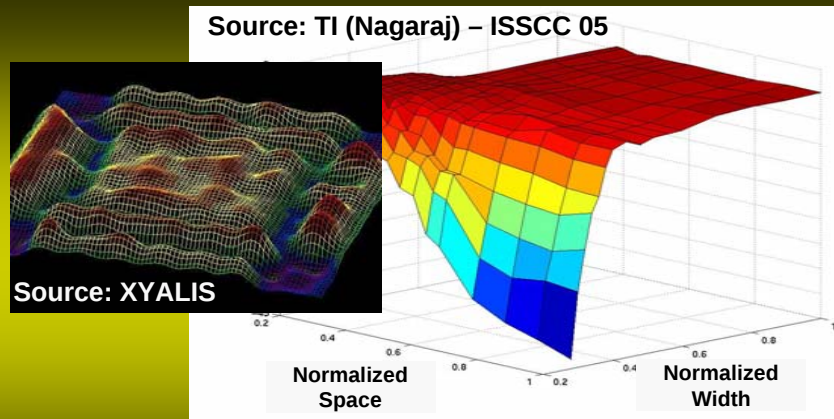
Catastrophic Failures Impact Yield

Sub-Nanometer Failures Cause Parametric Yield Loss



Non-linear variations of transistor delay and leakage with gate length variations

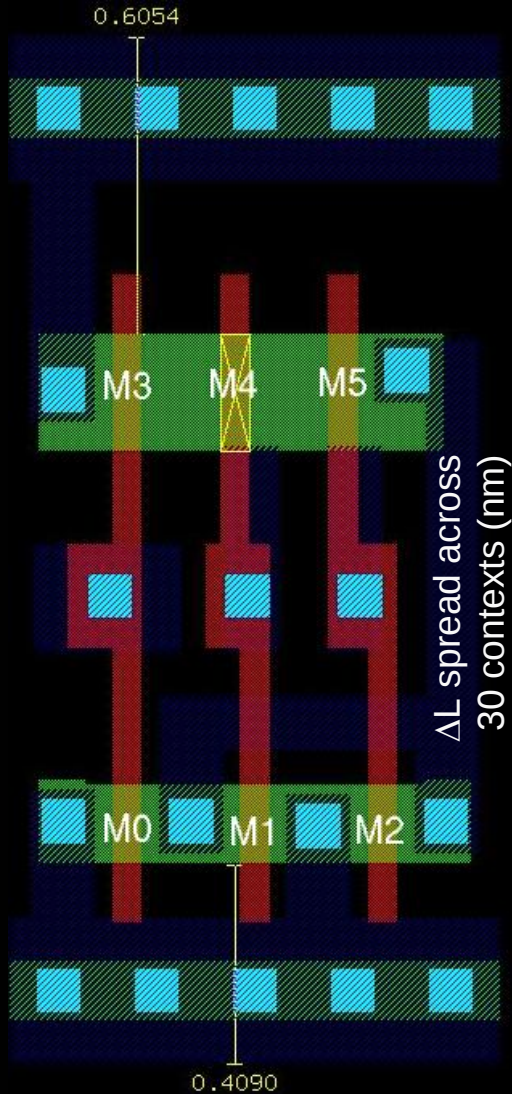
Device variations cause leakage power and delay failures



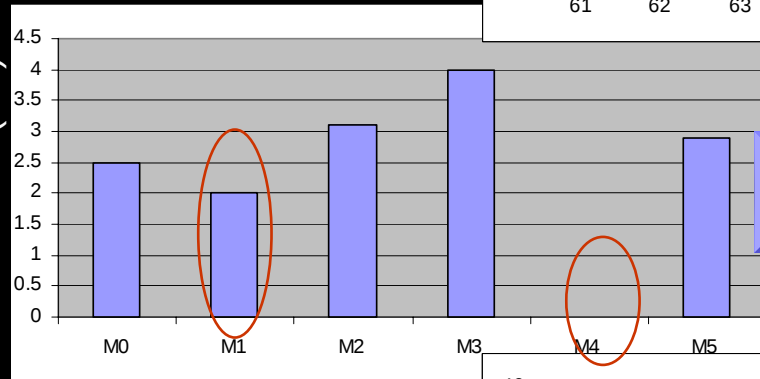
Interconnect variations create delay variations

- ◆ Increased sensitivity to manufacturing variations on both devices and interconnect
- ◆ Current design flows based on ideal GDSII, margins and rules translates in large margins, over-design and long timing closure or undetected parametric failures

Context dependent Variability cannot be Addressed by Rules and Margins

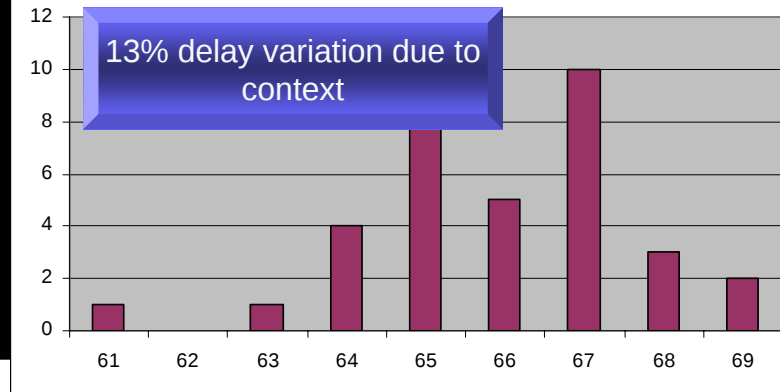


ΔL spread across 30 contexts (nm)



Courtesy of a leading foundry, a Clear Shape partner

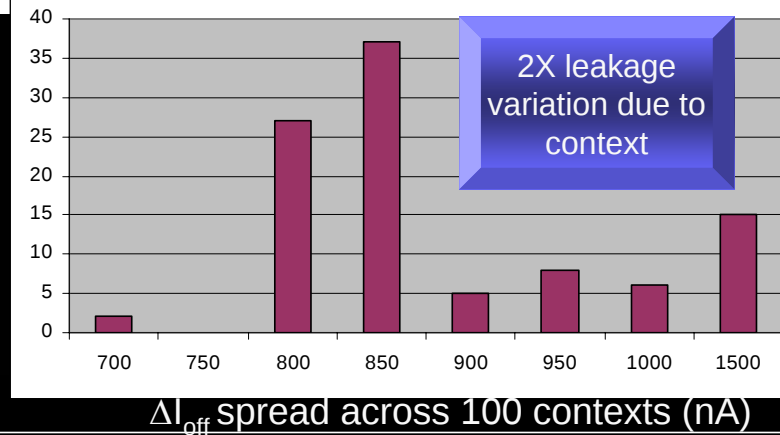
Number of contexts



$\Delta\tau$ spread across 30 contexts (ps)

Top and bottom context impacts transistor CD !

Number of contexts

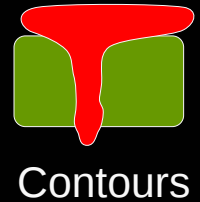


ΔI_{off} spread across 100 contexts (nA)

Traditional ideal-GDSII based design methodology is failing....

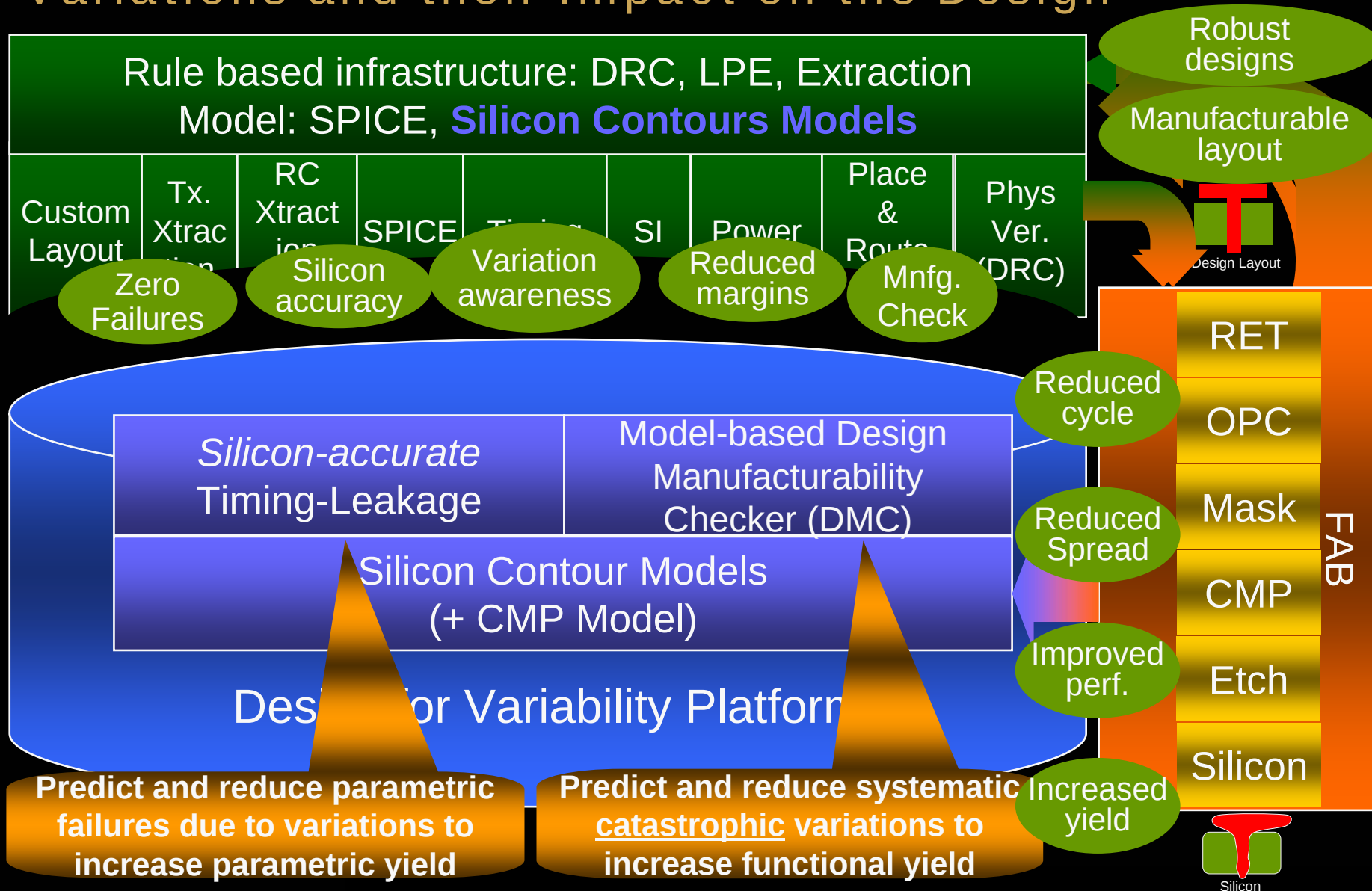


Designers need to move
from ideal GDSII
to contour-based design tools
to predict nanometer silicon behavior

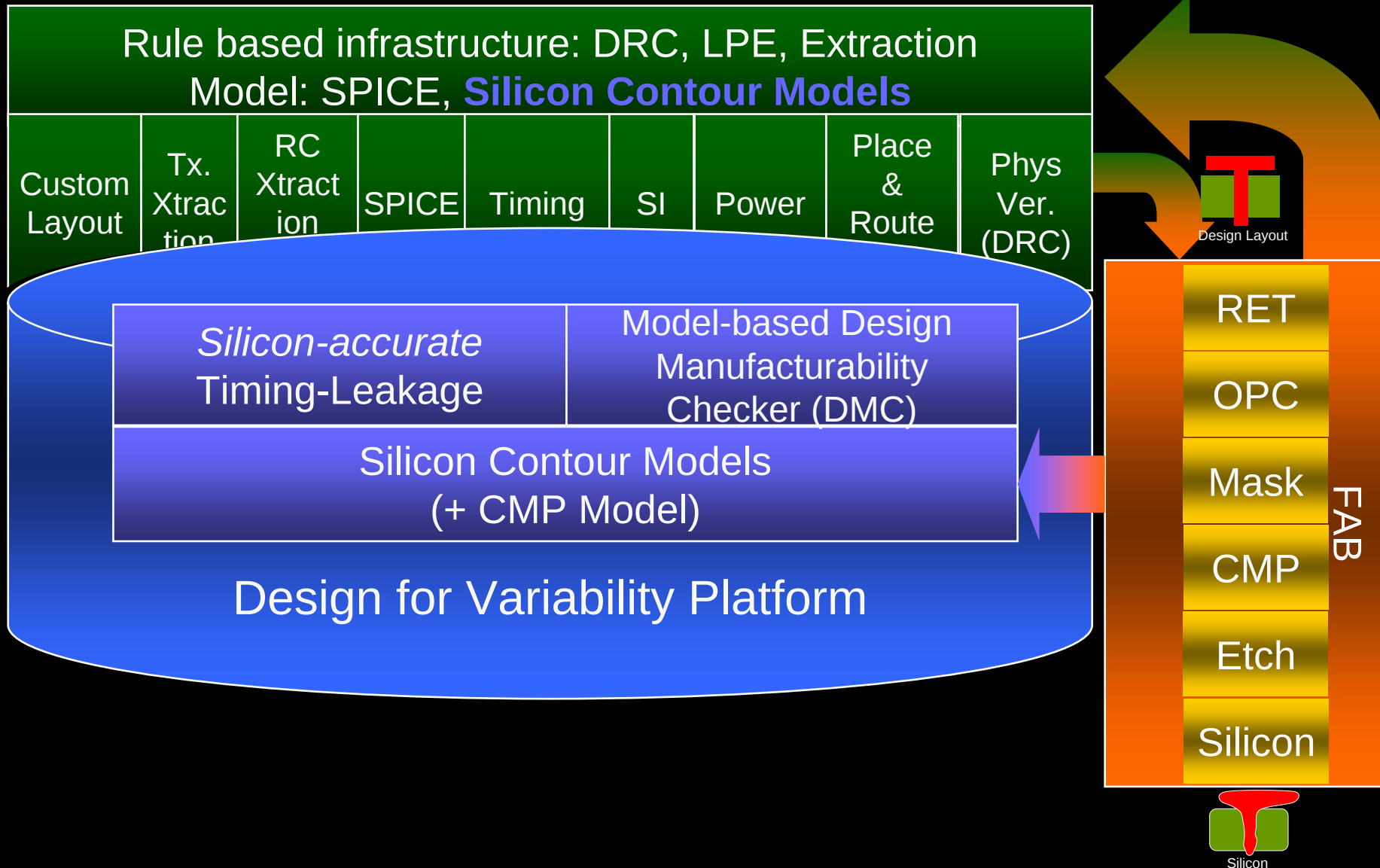


- ◆ Si-accuracy requires upfront FAB validation
- ◆ Must work with traditional design flows
- ◆ Library, IP, and Full-chip level
- ◆ Runtime in hours for full-chip
- ◆ Manufacturing/OPC TOOL independent
- ◆ Address both catastrophic and parametric yield issues

Design Infrastructure Evolution to Predict Mfg. Variations and their Impact on the Design



Disruptive Technology to Improve Yield without Disrupting Design Flows



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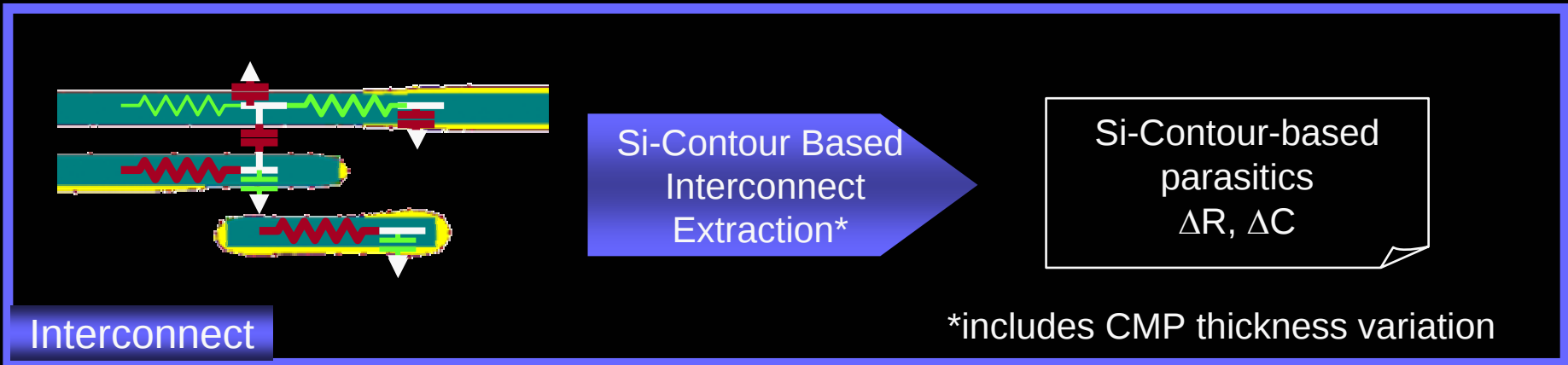
Manufacturing Post-GDSII RET/OPC Flow



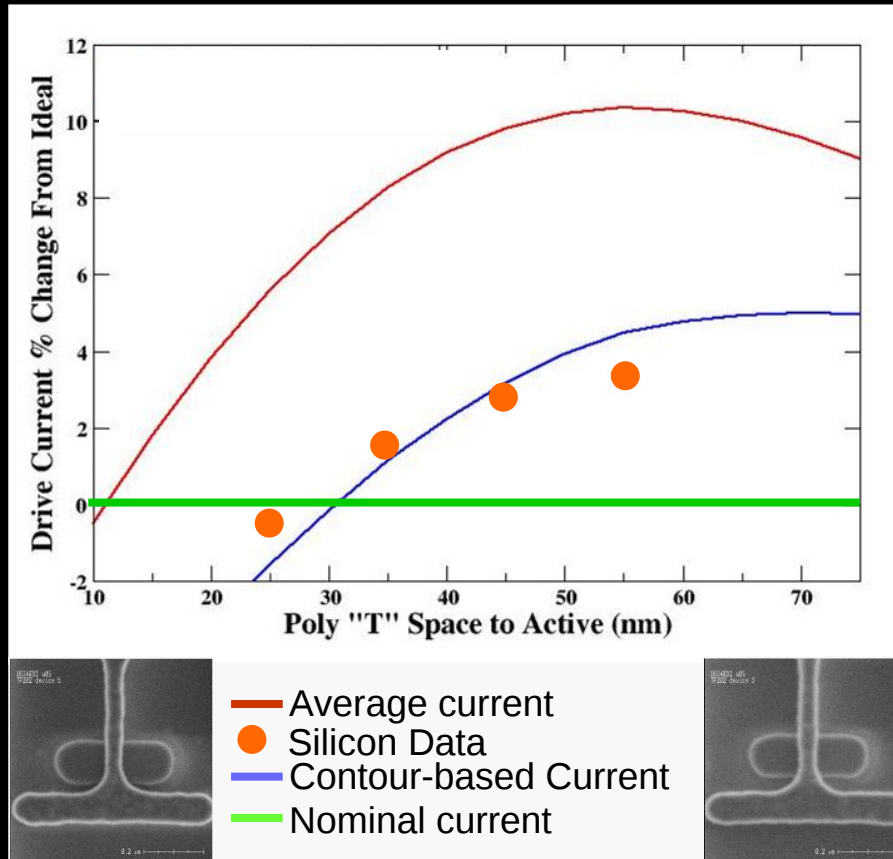
Design Layout



Contour-based Extraction Delivers Silicon-Accurate Parametric Analysis



Silicon Validation of Contour-based Device Modeling

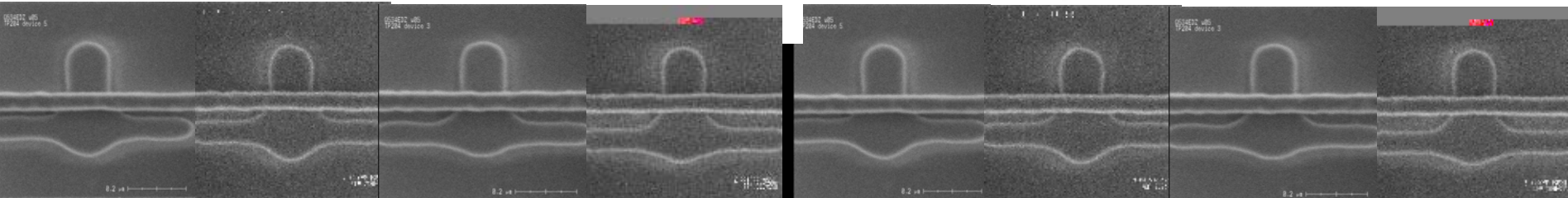
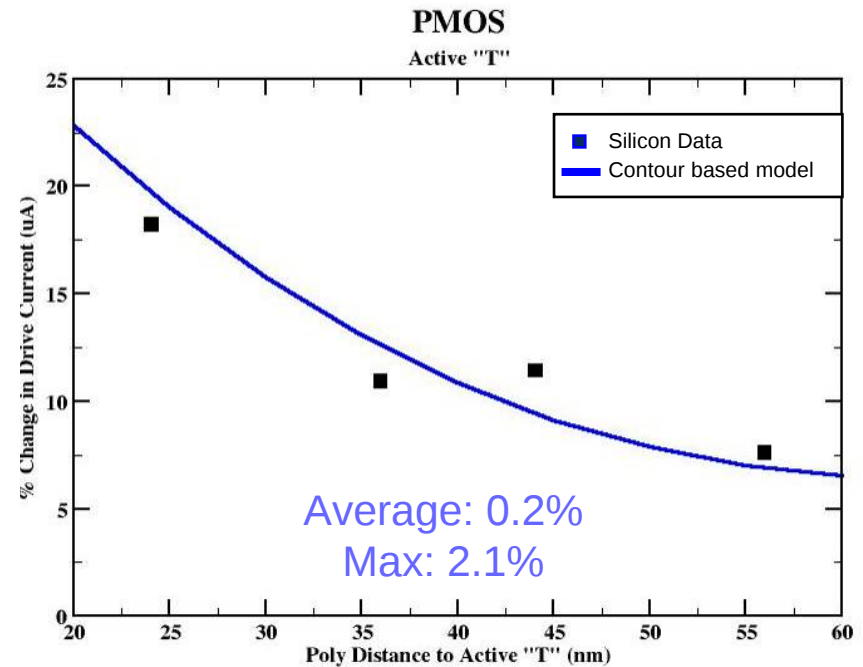
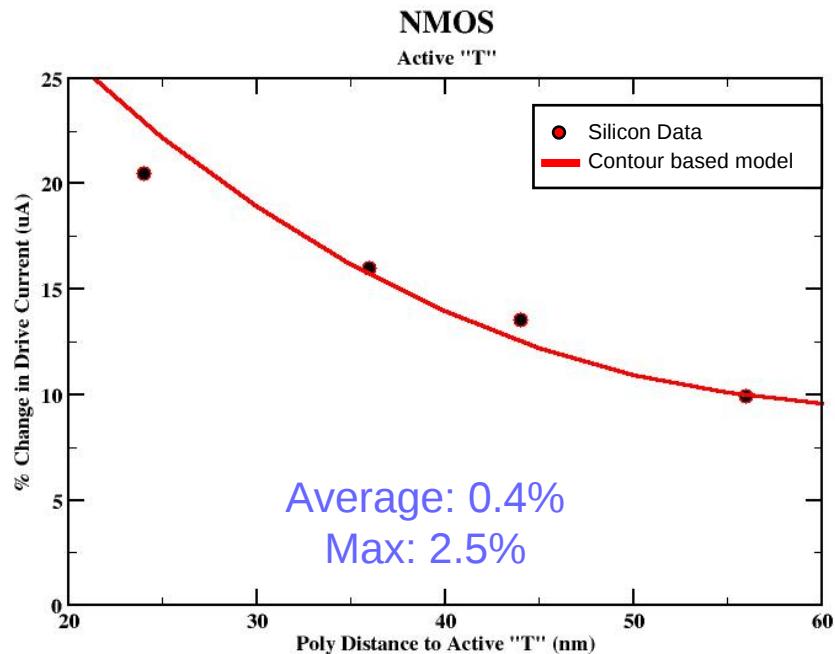


- ◆ Generate Contour for Poly flaring structures
- ◆ Compared current predicted with contour-based device model and silicon measurement
- ◆ Must take into account electrical behavior of sub-nanometer transistors

Courtesy of a 65nm major semiconductor vendor,
Clear Shape partner

Predicted silicon within 2%

Silicon-Proven Device Modeling



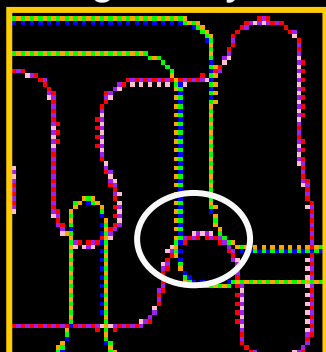
Courtesy of a 65nm major semiconductor vendor, Clear Shape partner

Prediction within 2.5% of Silicon

Contour-based Analysis Detects and Reduces Catastrophic Systematic & Parametric Variations

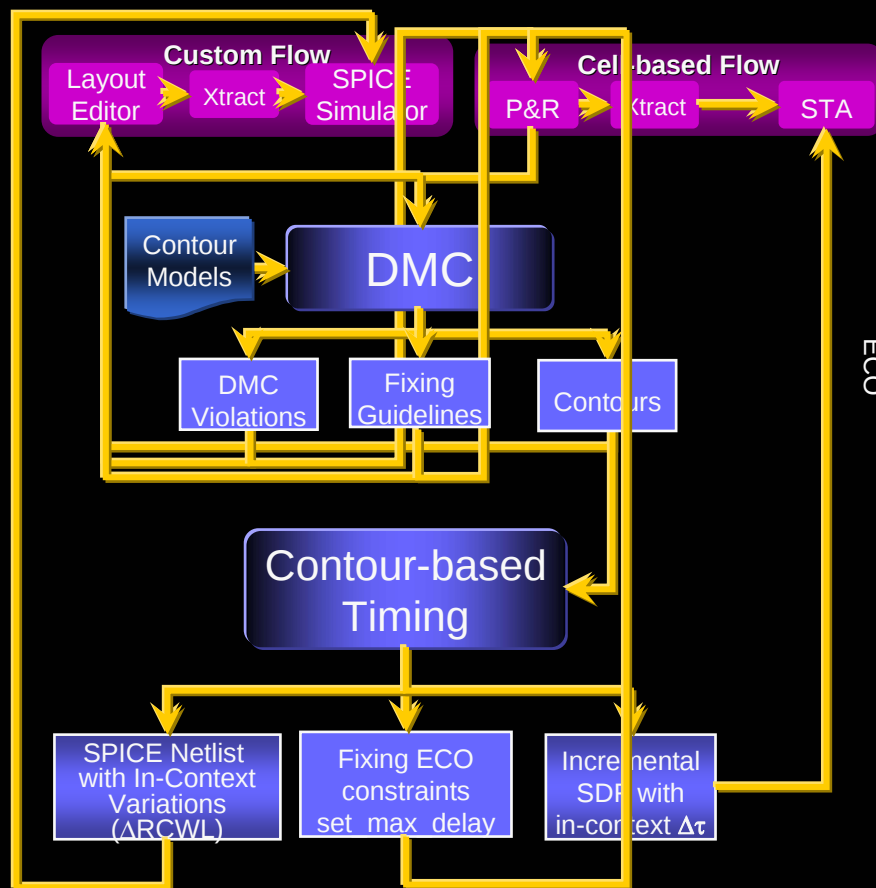


Original layout

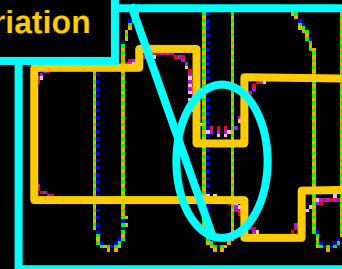


Clear Shape Results

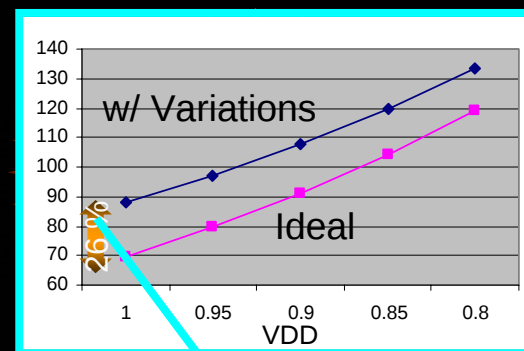
Predict & reduce systematic catastrophic variations to increase functional yield



25% W variation



Clear Shape Results



26% longer hold time

Predict & reduce parametric failures due to variations to increase parametric yield

Outline

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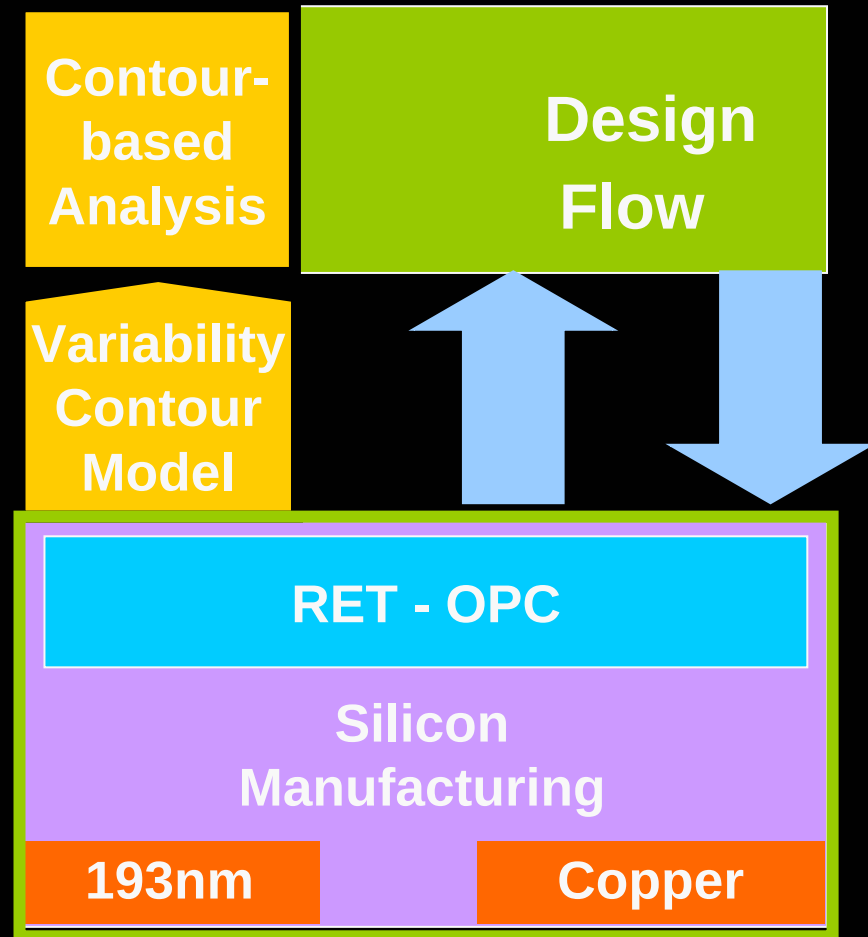
Designers Need Universal Solutions to Address Systematic and Parametric Failures

Contour-based Design Manufacturability Checker

- ◆ Need fast and accurate hotspot detection and contour prediction
 - Full-chip, blocks or cells - in hours!
- ◆ Easy to use with DRC-like use-model
- ◆ Endorsed by foundries and fabs
- ◆ OPC-tool independent

Contour-based Variability Analysis

- ◆ Predict impact of device and interconnect variations during design
- ◆ Silicon-proven device modeling
- ◆ Remove margins
- ◆ Accelerate timing closure
- ◆ Better Yield



Work with an Fab and Fit into any existing design flows

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