DFM/DFY Practices During Physical Designs for Timing, Signal Integrity, and Power

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Outline

- Introduction and Knowledge Background
- Practices in 65nm DFM topics (CAA/VCMP)
- Production yield analysis (example)
- IR drop impact to yield and prevention
- Conclusions

Introduction (1/2)

- Design Closure Challenge at Nanometer Dimensions
  - timing
  - signal integrity
  - low power
  - deep sub-wavelength lithography limitations
  - manufacturing closure.
- DFM and DFY Methodologies Required for Profitable Yield
  - process variation of device and interconnect
  - RC corners are considered for timing closure
  - defect vs. yield analysis is moving from rule-based to statistic-based

Introduction (2/2)

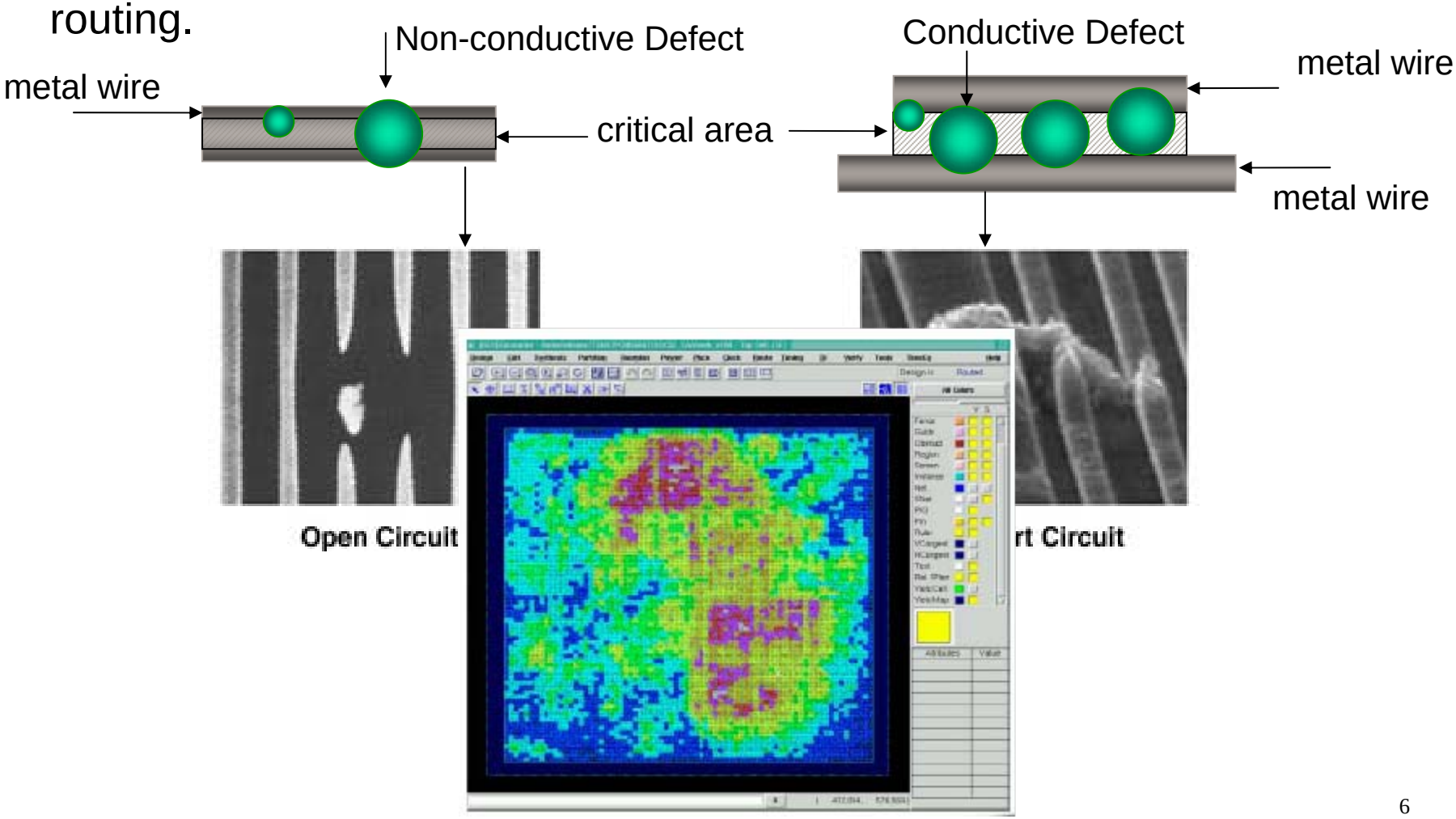
- Chip Defect Categories:
  - Random defects:
    - random particles
    - result in open/short, resistive pinching, and additional coupling
  - Systematic defects:
    - design process technology
    - chemical impact on process materials
    - mechanical impact on manufacturing/lithographic processes
    - planarity, antenna effects, via opens, and various other effects
  - Parametric defects:
    - logical function correctly, but with
    - timing, signal integrity, and voltage-drop issues

Knowledge Background

- DFM concept raised since 0.13um technology node.
  - Focused on OPC (Optical Proximity Correction) at 0.13um.
  - Additional CAA, CMP and LPC effects at 90nm and 65nm.
- Many EDA vendors put resources to develop DFM analysis tools
- A comprehensive yield optimization throughout the design flow should cover:
  - *Yield Optimization with Cell Mapping*
  - ✓ *Yield Optimization during Chip Prototyping*
  - ✓ *Yield Optimization during Routing*
  - ✓ *Yield Improvement on Testing (DFT)*
- We will present our experience of DFM analysis on 65nm designs and also show some silicon examples for yield analysis and improvement.

CAA Analysis (1/2)

- By analyzing the critical areas, defect-limited yield can be estimated based on the probability of the failures of vias and point defects on routing.



CAA Analysis (2/2)

- The experiment illustrates that the impact of double cut via insertion on yield. After replacing around 34% 1-cut via (single via) with 2-cut via (double via), the yield loss due to via defect (Y1) is reduced around 0.14%.

Yield improvement by adding redundant via

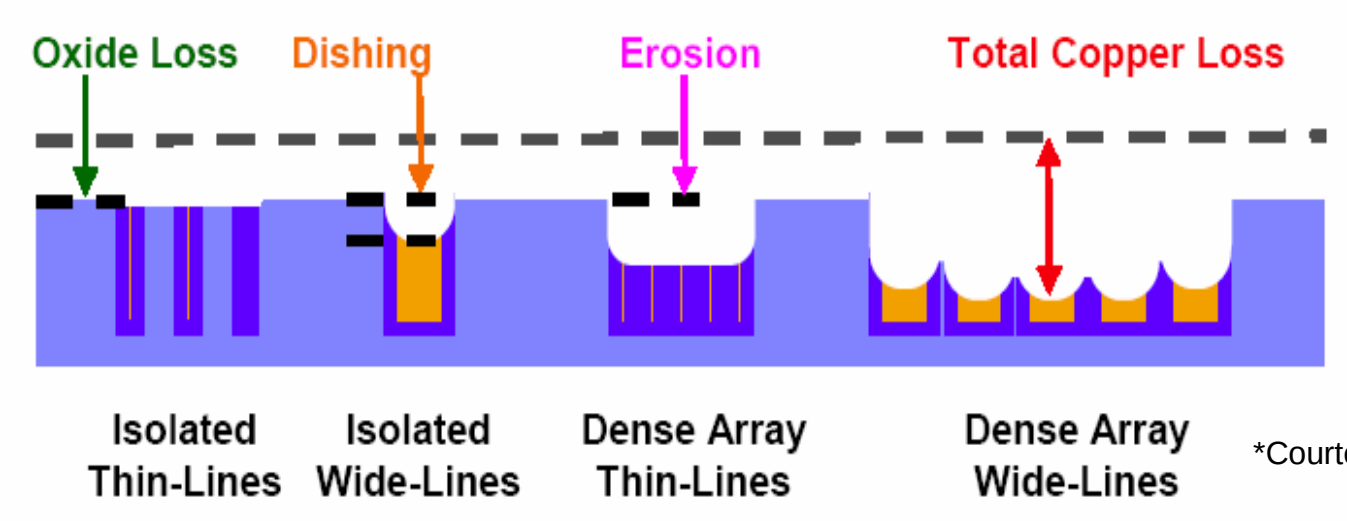
	1-cut via#	2-cut via#	Y1	Y2	Y3
w/o double via	5.33E+06	3.25E+03	0.712%	0.305%	1.015%
w/i double via	3.51E+06	1.82E+06	0.571%	0.314%	0.883%

*Y1: Yeild lost% due to via defect
*Y2: Yield lost% due to wire defect
*Y3: Total yield lost%

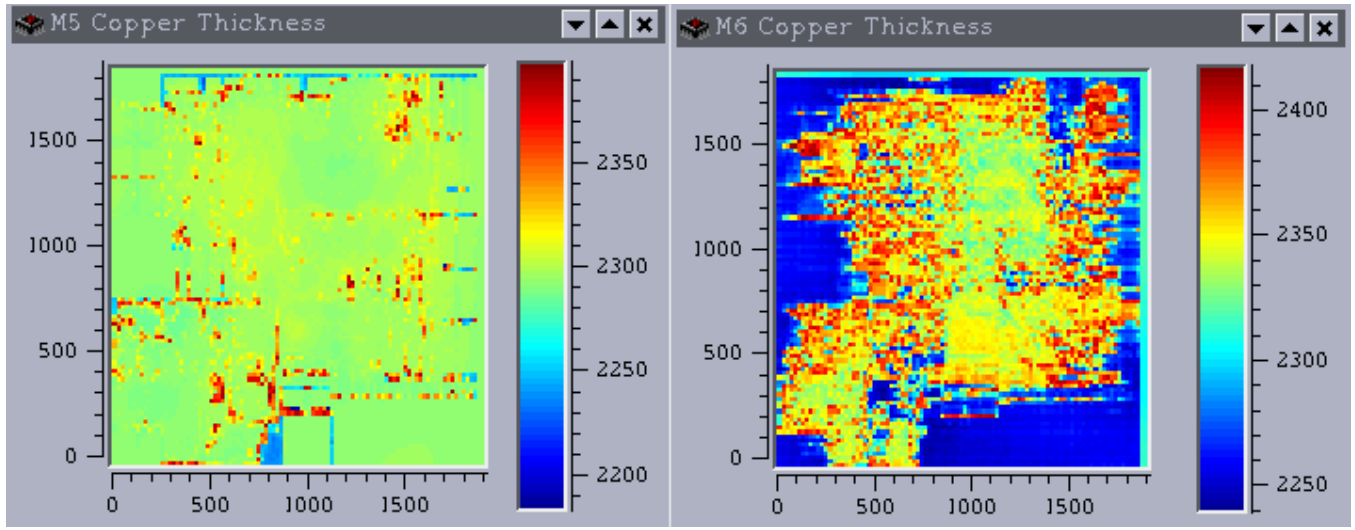
-0.14%

VCMP (Thickness Simulation) (1/4)

- Metal thickness is layout pattern dependent



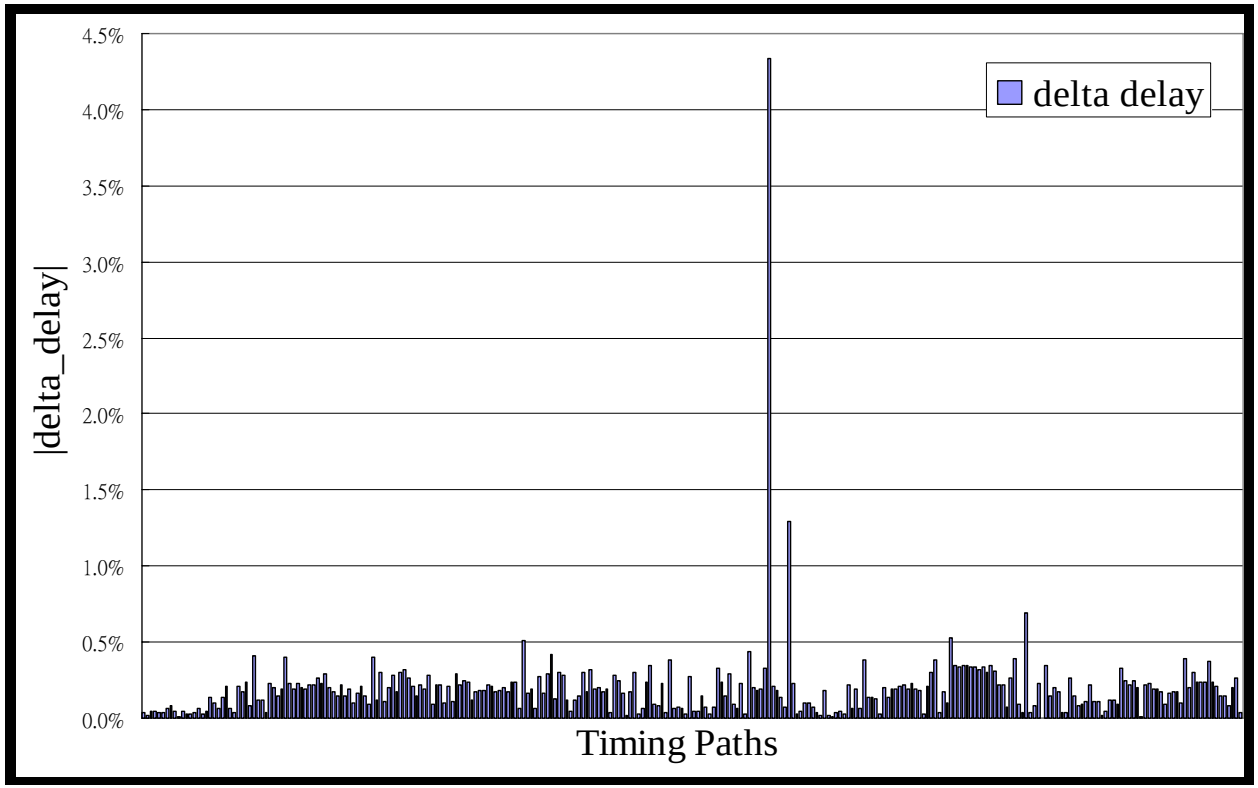
*Courtesy of TSMC Ref_Flow 7.0



Simulation result for 65nm case

VCMP to Timing Impact (2/4)

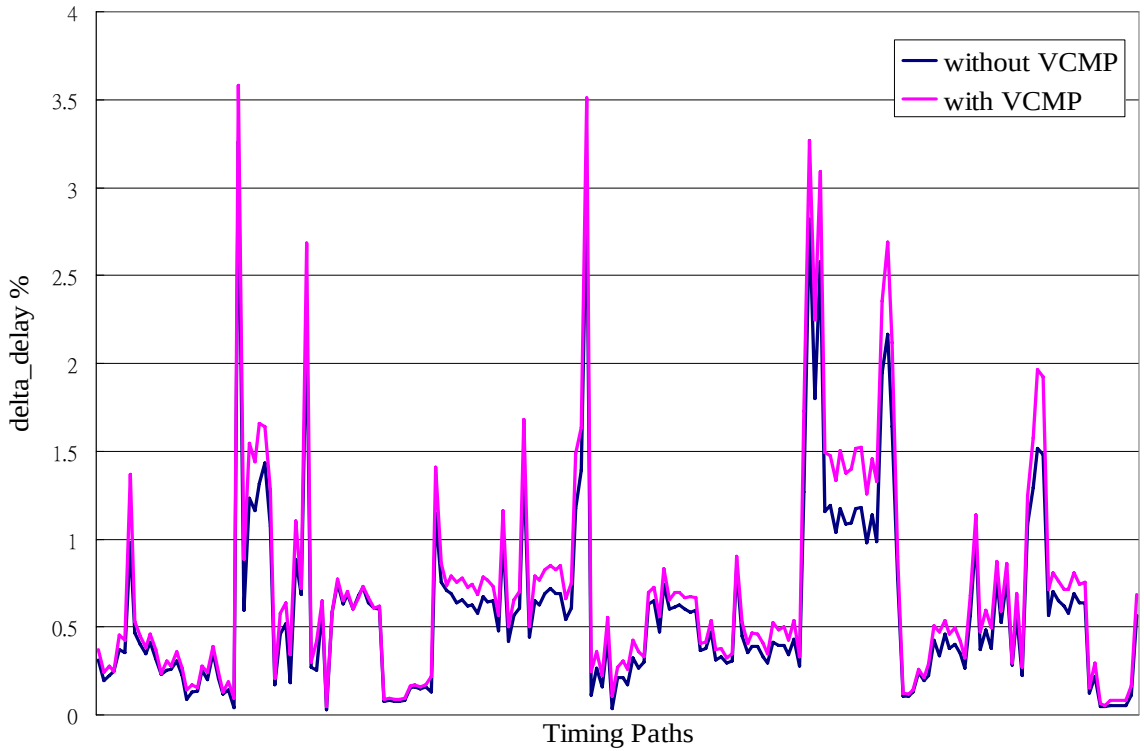
- CMP Effect is considered during RC extraction
- Some foundries support DFM data kits (e.g. TSMC's DFM Data Kit)
- Some case shows timing difference of VCMP vs non-VCMP to be around 4.5%.



The timing comparison of RC extraction with and without VCMP simulation

VCMP to Timing Impact (3/4)

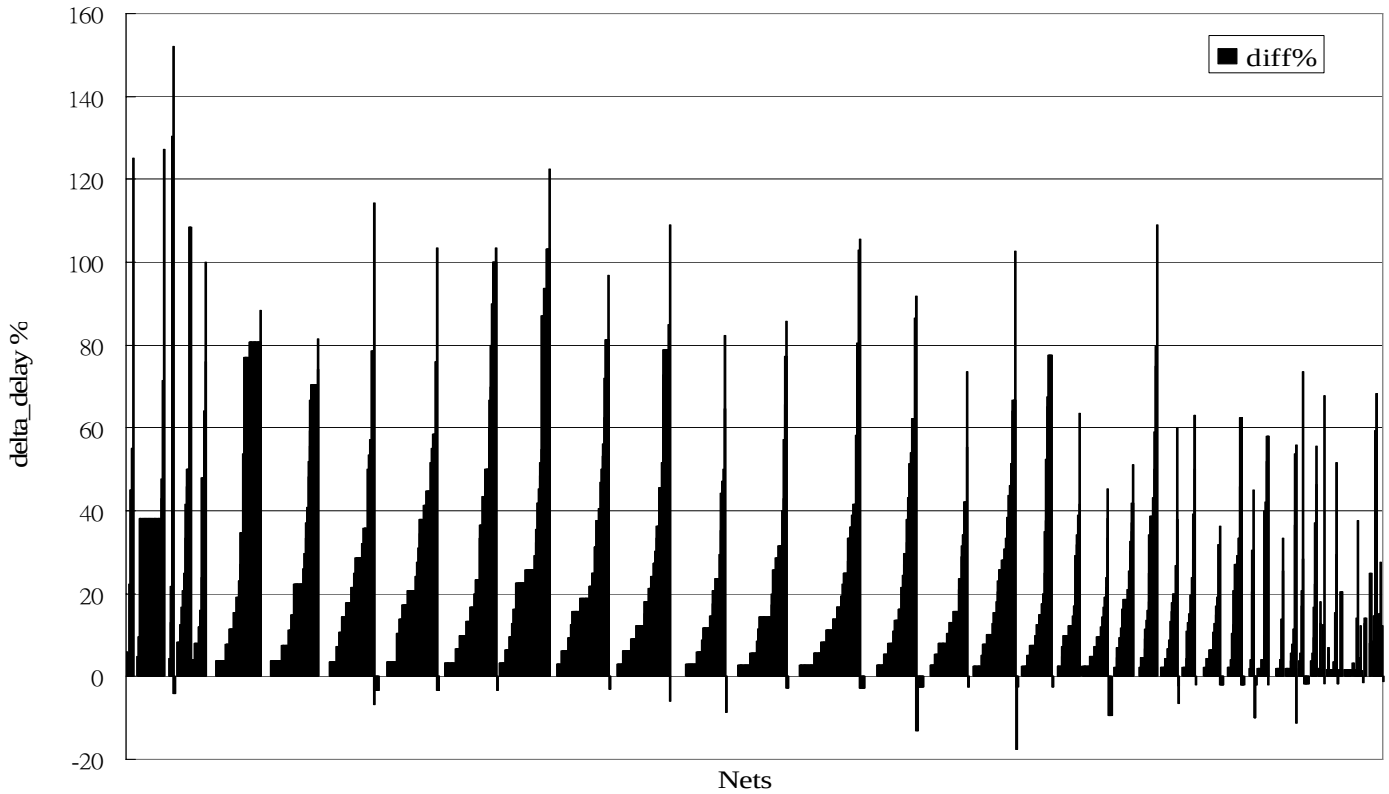
- Dummy metal fill can be used to minimize the impact of CMP effect.
- Virtual CMP simulation should still be integrated with the flow to predict metal and layout thickness for more accurate parasitic extraction and better timing accuracy.



Timing impact due to dummy metal fills

VCMP to Timing Impact (4/4)

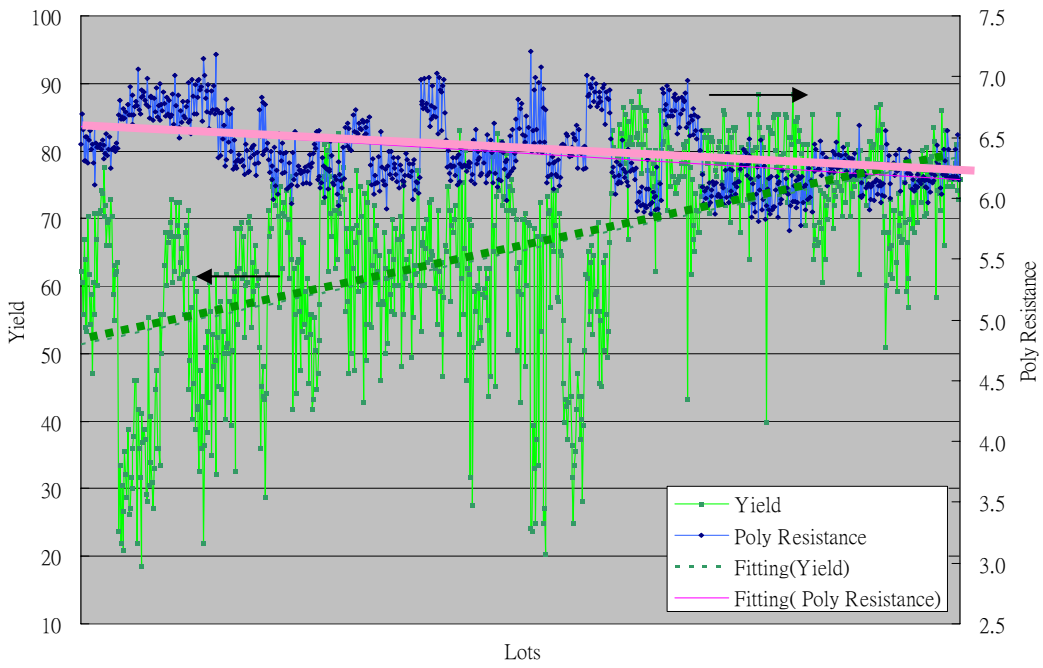
- Dummy metal insertion also brings extra work on timing closure.
- Example below shows the impact of SI incremental delay due to dummy metal fills. SI incremental delays of some timing paths may have 1.5x increase and some paths may have 20% decrease.



SI timing impact due to dummy metal fills

Yield Trend Analysis and Correlation

- Another case with more yield trend related to poly resistance, but not covered by current DFM solutions.
- The results indicate parameters other than CAA, CMP, and LPC might also affect the yield significantly, but not well modeled in current DFM tools.



Poly resistance versus CP-Yield analysis

Each spot of a dot line indicates the CP-yield of a single lot and the associated fitting curve of those CP-yields is highlighted with a wider dot line.

Each ohm value in respect to poly resistance is denoted with a spot of a solid line and its associated fitting curve is highlighted with the narrower dot line.

It is obvious that when the ohm value of poly resistance is lower, the CP-yield can be improved from 50 percent to 85 percent.

Dynamic IR (1/4)

- Yield fluctuation found on below CASE1 and CASE2
- Before IR drop is considered for timing, both are timing closed.
- With dynamic IR drop considered, hold violations paths show up for CASE1 and CASE2 with degraded cell timing as in Table below.
- For this situation, yield may be over-killing if dynamic IR drop is not resolved before tape-out.

Timing Checks with IR Drop Consideration

	Average %delta	Min %delta	Max %delta	Worst Slack	#failed paths
CASE 1	0.28%	-0.31%	1.59%	-138.8ps	51
CASE 2	0.41%	-0.09%	0.65%	-117.8ps	> 100

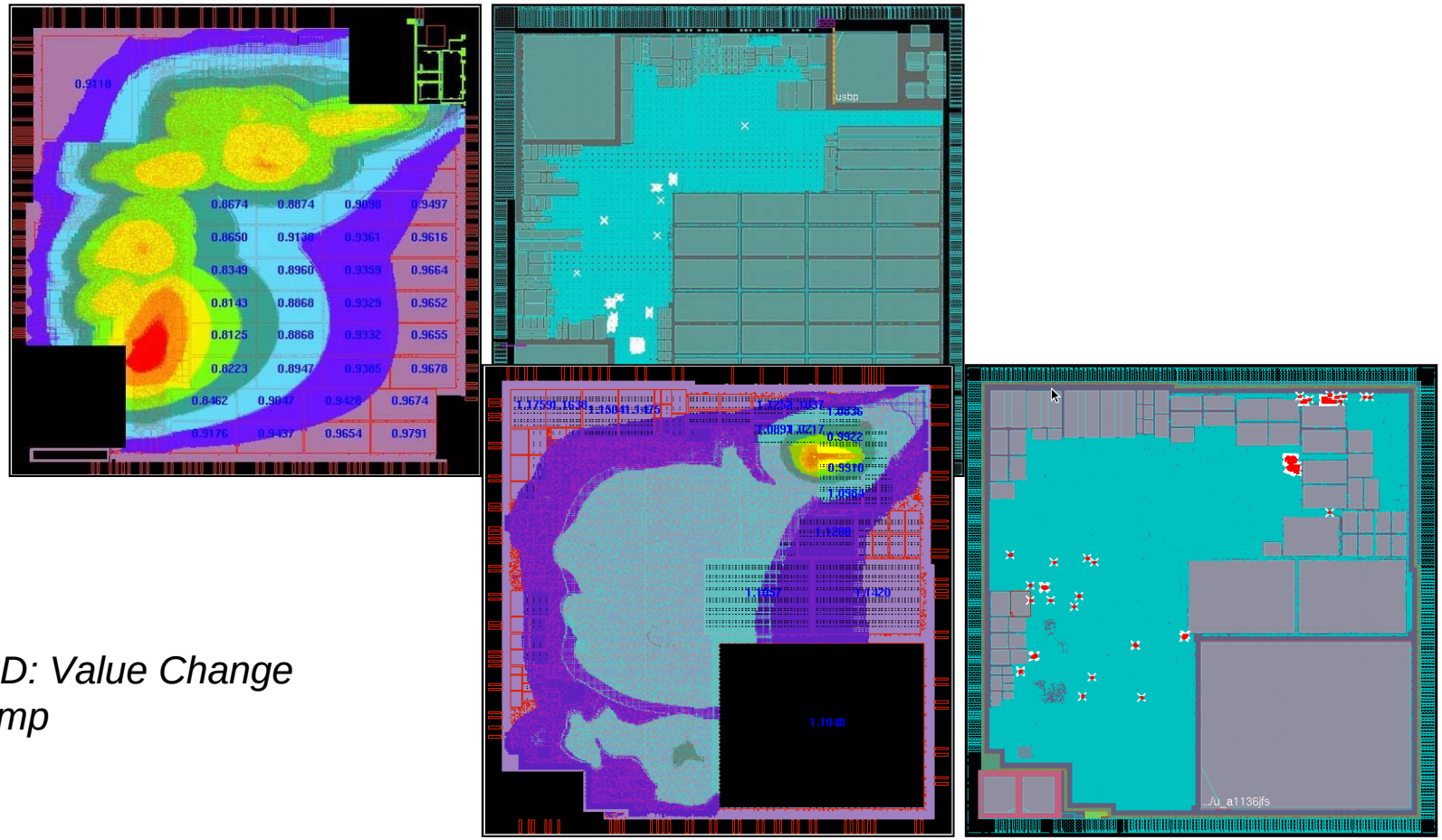
* Delta means the cell timing degradation with IR effect

Dynamic IR (2/4)

- Another case is found with yield overkill due to dynamic IR drop at ATE testing while all function patterns pass on tester and the design was also proven on system verification. However, the yield is around 30% due to DFT testing.
- After investigating the failures, we found that scan mode hold time violation due to dynamic IR is the root cause. After adjusting test clock delay, improving the power plan and reserving more timing margin for dynamic IR drop, the yield is improved to over 90%.
- From the above cases, we also see some issues on current tool flow trying to predict dynamic power behaviors.
- More IR simulations examples following next page.

Dynamic IR Prevention & Verification (3/4)

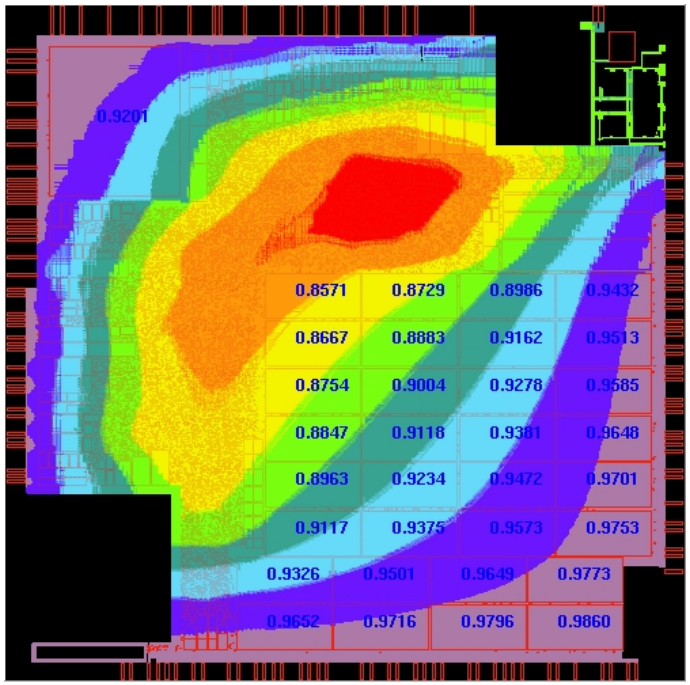
- Existing approaches: Vector-less and VCD-based analysis
- The experiment results of flip-flop density check reveals a significantly high correlation with VCD-based dynamic IR analysis.



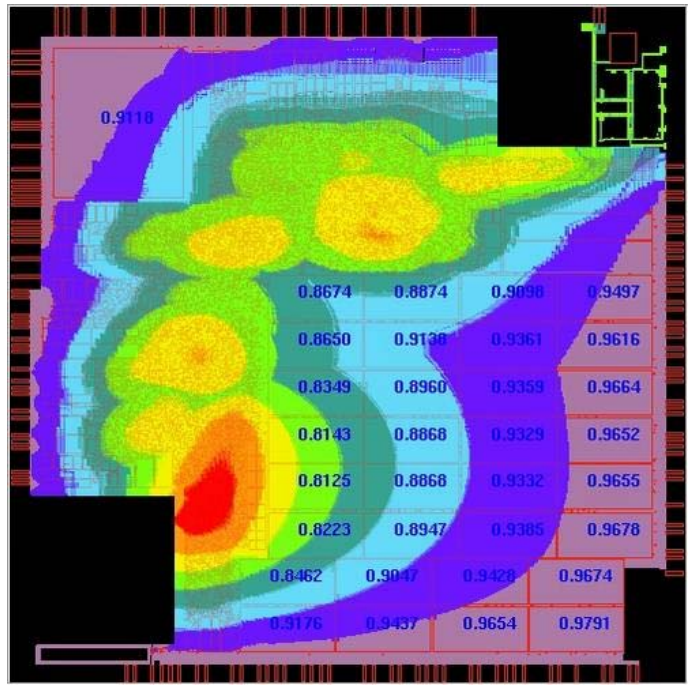
VCD: Value Change Dump

Dynamic IR (4/4)

- Comparison of vector-less and VCD-bases results suggests that there still have room to improve vector-less based dynamic IR analysis



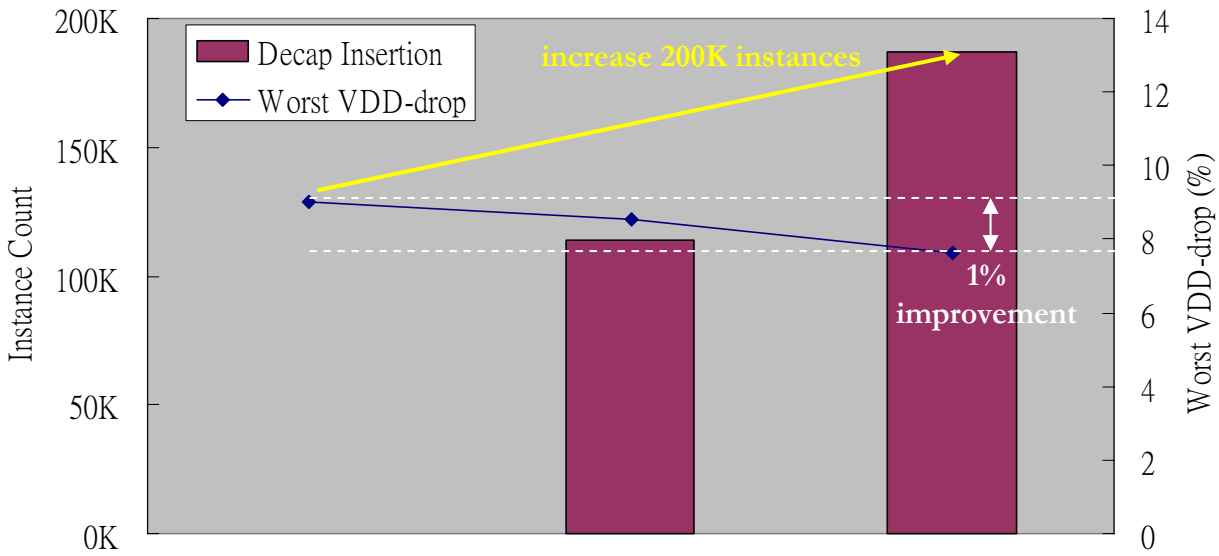
Vector-less Analysis



VCD-based Analysis

Dynamic IR Prevention & Verification (1/2)

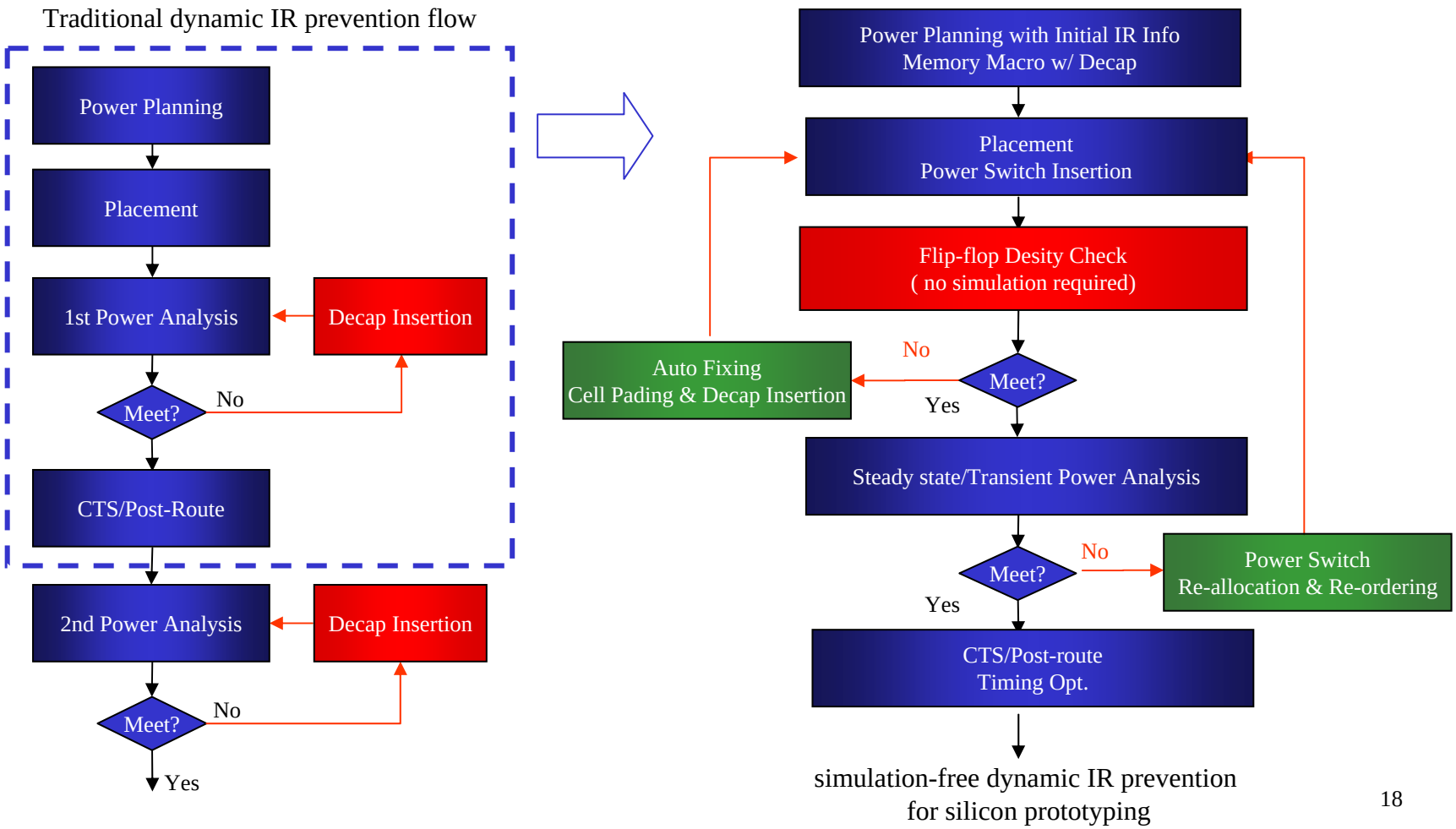
- Decap insertion is a typical way to address Dynamic IR issue, but at the late stage of implementation, there simply is no space available to solve the hot spot.
- As illustrated below, the improvement in voltage drop may be trivial, even while the number of decap cells inserted is increased dramatically towards 200K instances.



Dynamic IR drop improvement by decap insertion

Dynamic IR Prevention & Verification (2/2)

- VCD-based simulation pattern is typical available late in design flow
- A simulation-free IR drop prevention flow is established



Conclusions

- For designs advanced to nanometer processes, DFM/DFY topics have become must-check items before GDS release to ensure profitable production.
- We share several real case data and analysis on DFM (CAA/VCMP) topics. The methodology and flow are considerably established. However, some case results suggest the analysis of WAT parameters also has great help on yield. This implies some room for overall DFY coverage enhancement remains.
- In parametric defect, we also shows case data related to dynamic IR issues. Analysis based on simulation vectors is more accurate but tends to be too late in design phase.
- A low cost and efficient methodology for dynamic-IR prevention is therefore developed, which have been applied to various designs and correlated through state-of-the-art dynamic IR analysis.