Recent Research and Emerging Challenges in Physical Design for Manufacturability/Reliability

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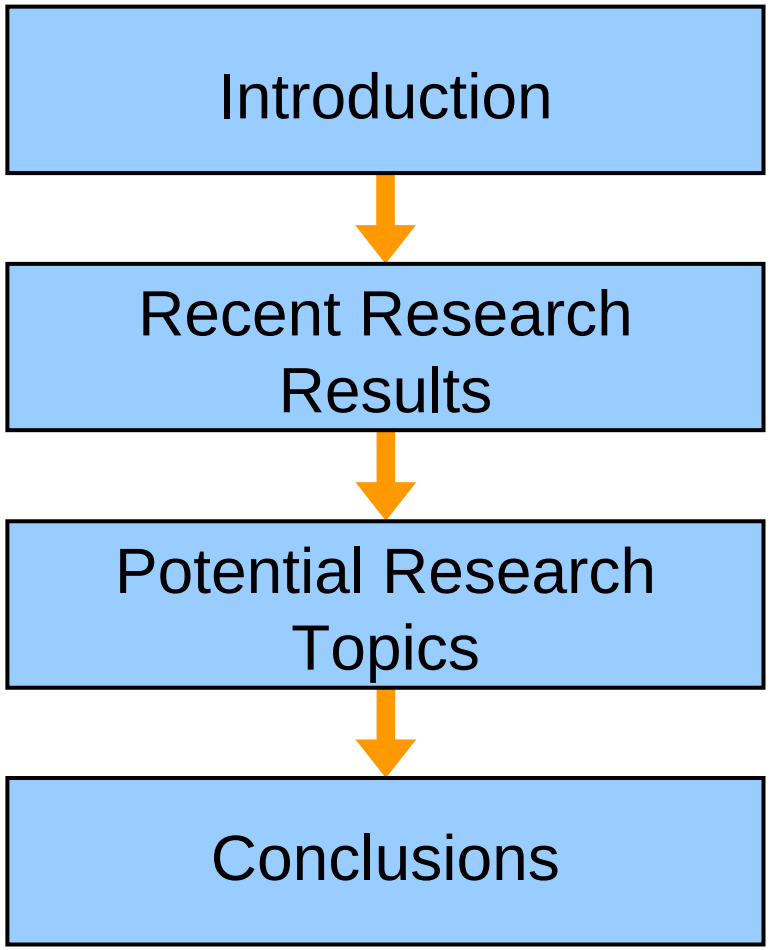
Outline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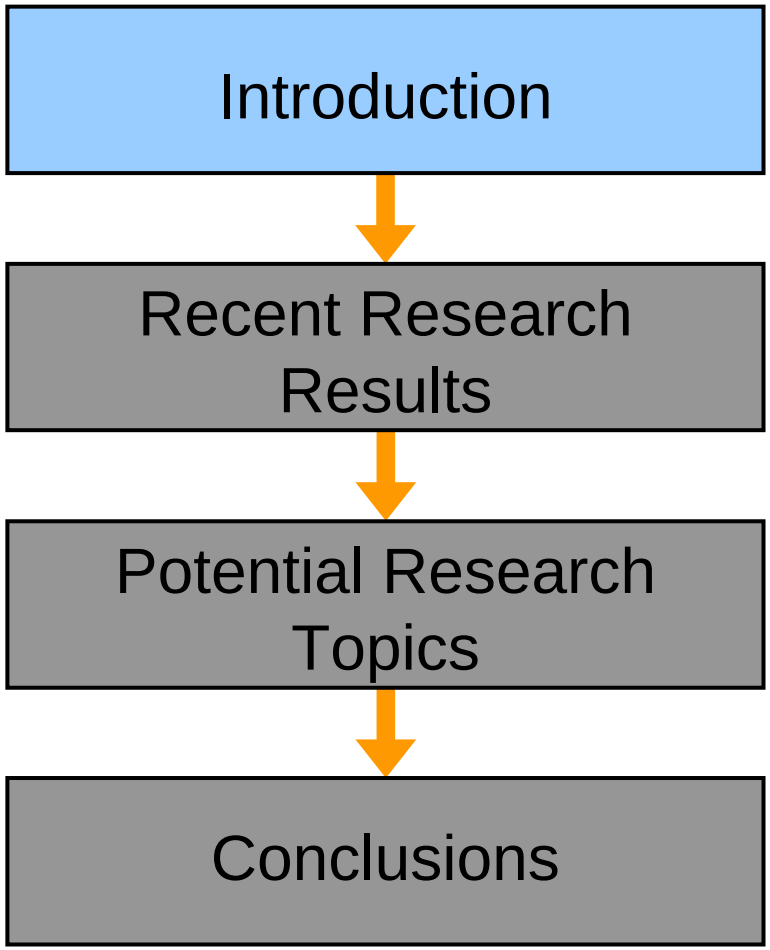
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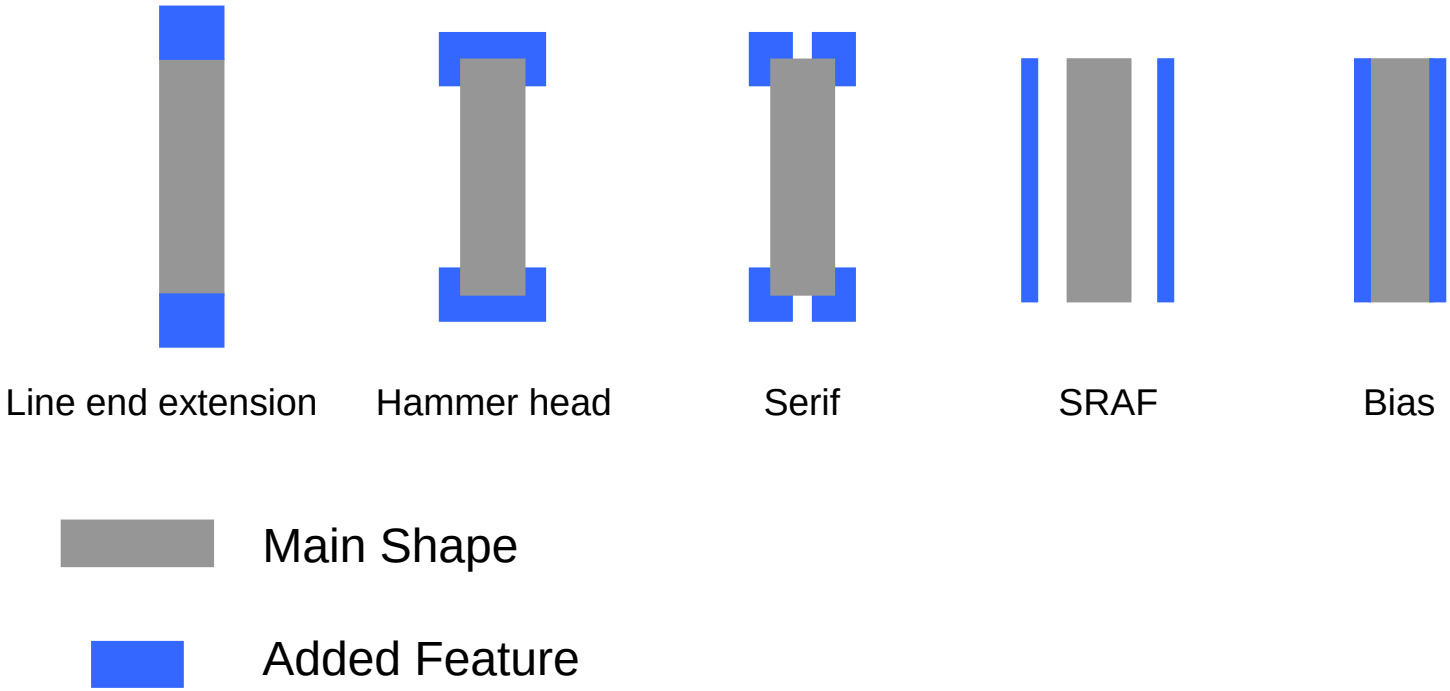
Introduction

- As IC process geometries scale down, the industry faces severe challenges in manufacturability and reliability.
  - Lithography
  - Chemical Mechanical Polishing (CMP)
  - Via failure
  - Antenna effect
  - …
- Resolution enhancement techniques (RETs) are employed to achieve better lithographic printability.
  - Optical proximity correction (OPC)
  - Phase-shifting mask (PSM)
  - Off-axis illumination (OAI)

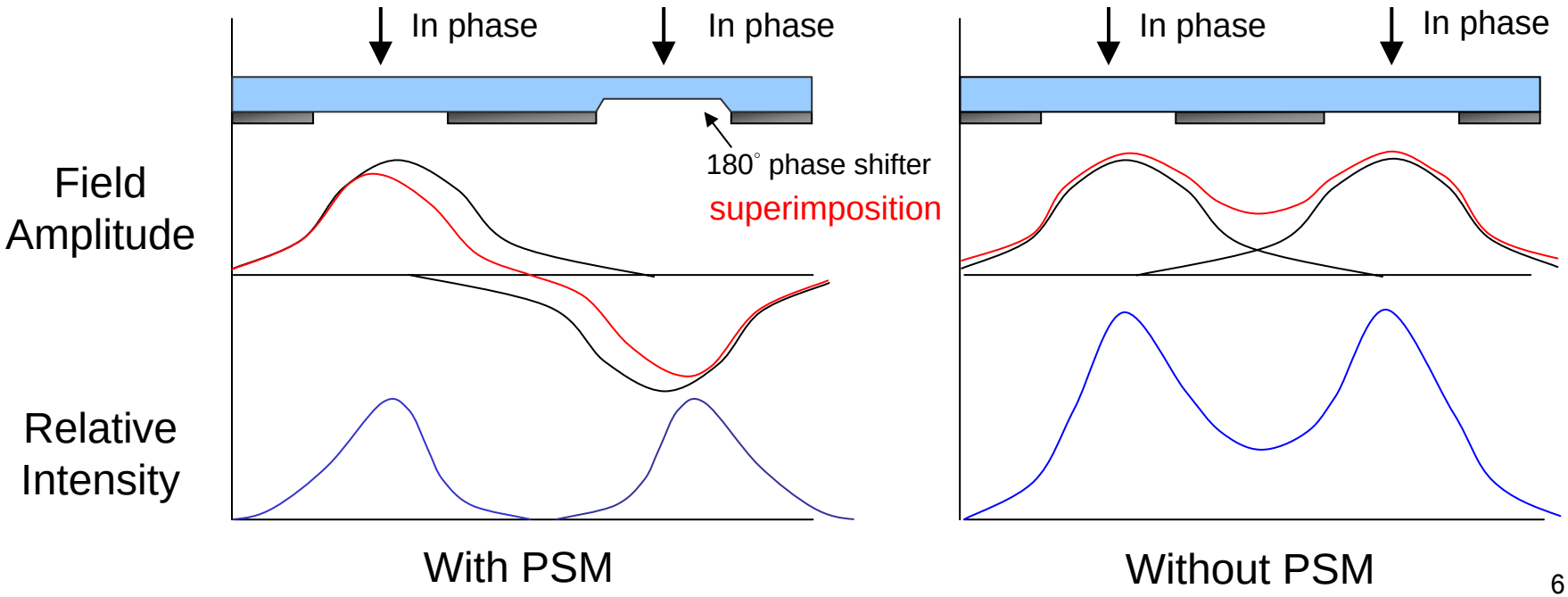
OPC

- OPC is done by adding or subtracting some features near main shapes.



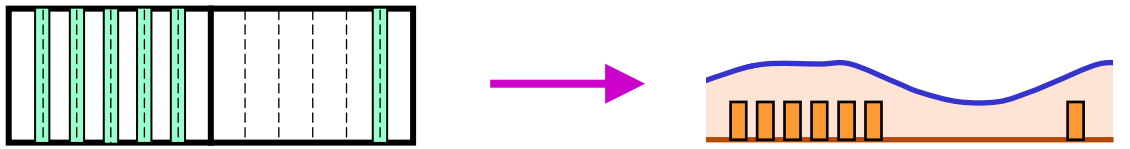
PSM

- PSM generates the phase difference to improve the aerial image.
  - Alternative PSM (AltPSM): Assign clear fields to opposite phases.
  - Attenuated PSM (AttPSM): Allow 5% - 10% of light to penetrate the “opaque” part of a mask.



CMP

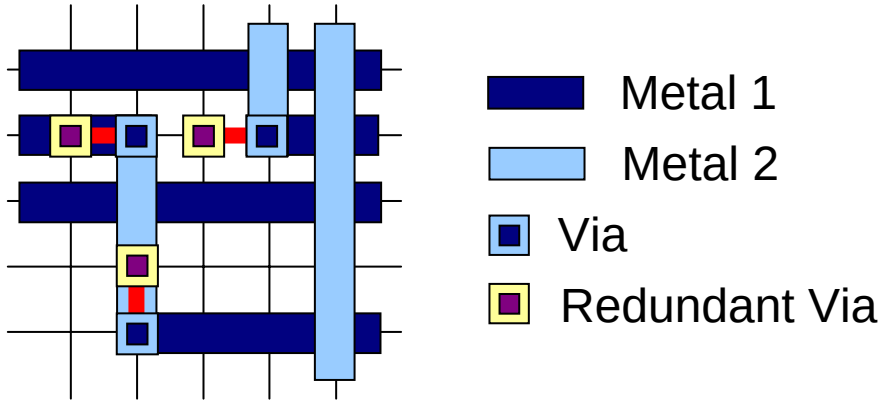
- Lithographic depth of focus (DOF) is limited, and therefore the thickness variation of a wafer must be strictly controlled.
- Post-CMP thickness is sensitive to layout density.
- A popular solution:
  - Dummy metal insertion



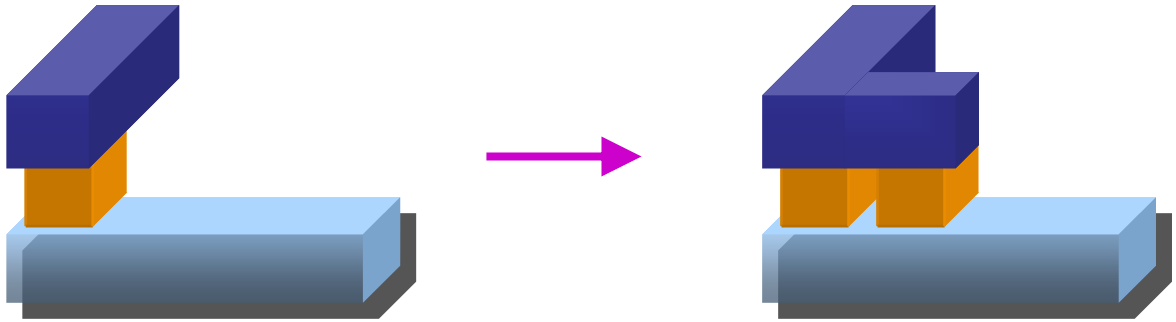
Larger density variations among neighboring sub-regions lead to more significant post-CMP thickness irregularities.

Via failure

- Vias may fail during fabrication or later
- A popular solution:
  - Double-via insertion: adding redundant vias to serve as fault-tolerant substitutes



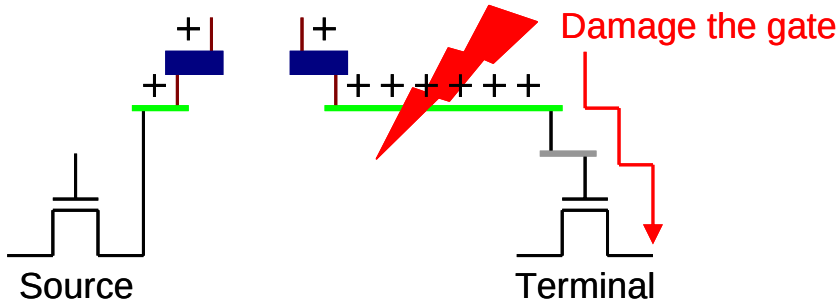
Double-Via Insertion



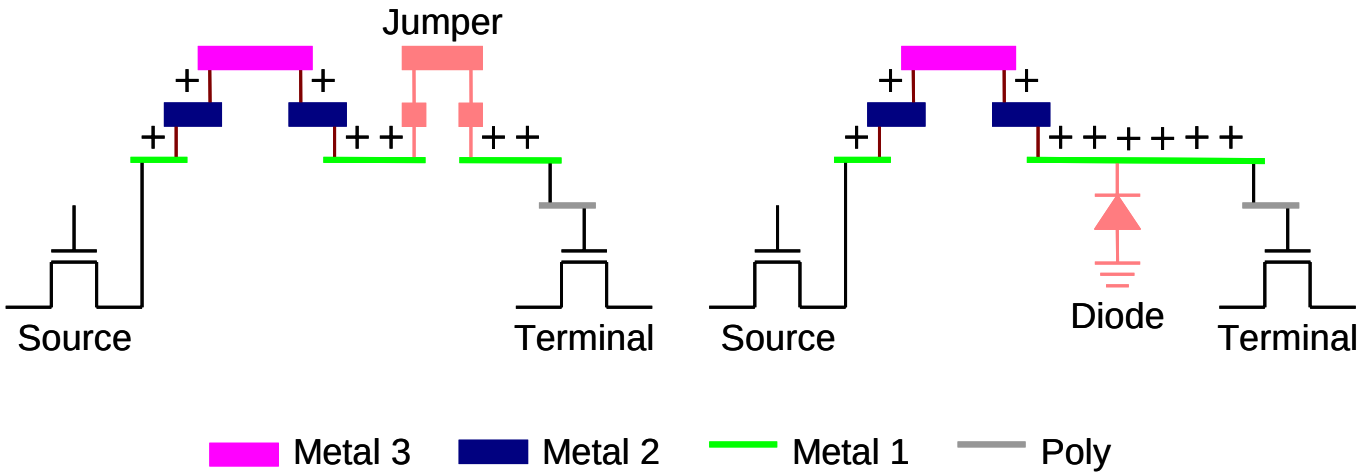
Double-Via Insertion

Antenna Effect

- During the plasma process, heavily accumulated charges on long floating interconnects will damage the gate oxide of active devices.
- Popular solutions:
  - Jumper insertion
  - Diode insertion



Accumulated charge damages the gate



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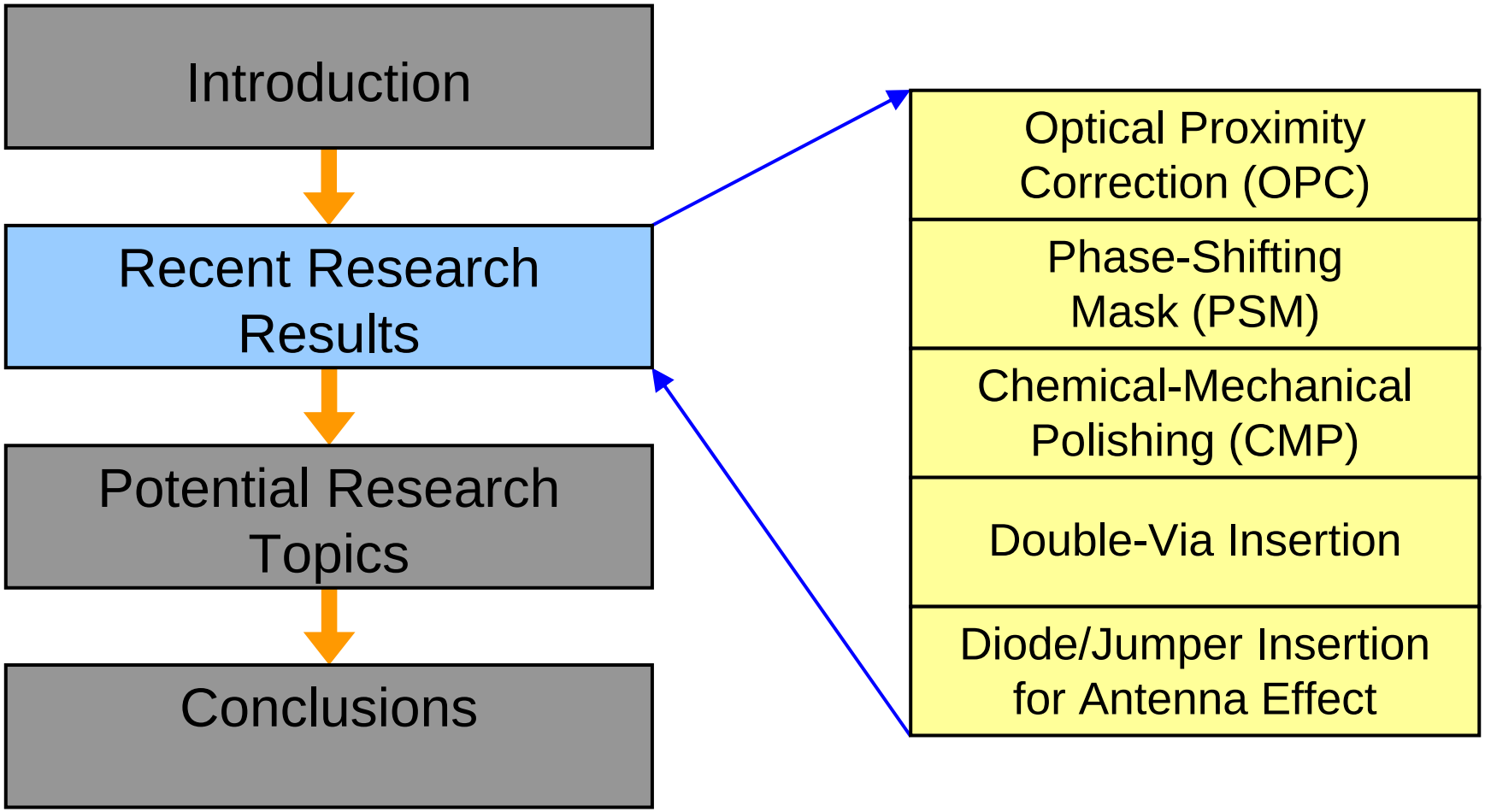
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Diode/Jumper Insertion for Antenna Effect

OPC-Aware Maze Routing

- Huang and Wong, “Optical proximity correction (OPC)-friendly maze routing,” DAC-04.
  - It is a pioneering work on OPC-friendly maze routing based on the Lagrangian relaxation formulation.
  - The router handles only hundreds of two-pin connections.
- Wu et al., “Maze routing with OPC consideration,” ASP-DAC-05.
  - Two OPC-aware routing problems are formulated and solved by modifying the Lee algorithm.
  - The local OPC cost of each routing grid cell is constrained as well.

OPC-Aware Multilevel Gridless Routing

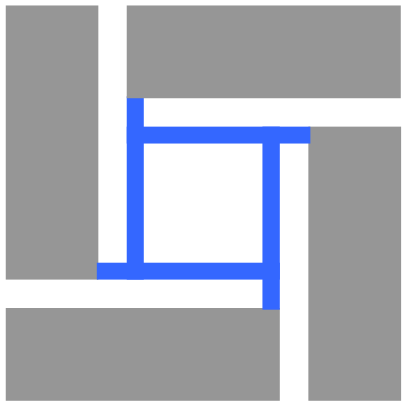
- Chen and Chang, “Multilevel full-chip gridless routing considering optical proximity correction,” ASP-DAC-05.
  - It can handle non-uniform wire widths and consider routability and OPC simultaneously.
  - The OPC cost of a line is defined as the number of added features.
  - It not only efficiently obtains better routing solutions with 100% routing completion, but also archives an effective reduction of OPC features.

RET-Aware Routing Using Simulations

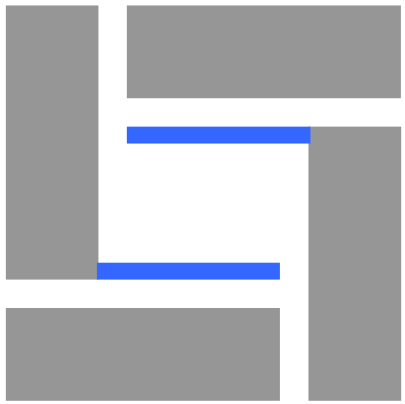
- Mitra et al., “RADAR: RET-aware detailed routing using fast lithography simulations,” DAC-05.
  - An RET-aware detailed router is developed to enhance the overall printability.
  - After the initial routing result, a fast lithography simulation is applied to introduce the lithography hotspot map (LHM).
  - According to the LHM, the router generates routing blockages for the stage of ripup and reroute.

2D SRAF Placement by Voronoi Diagram

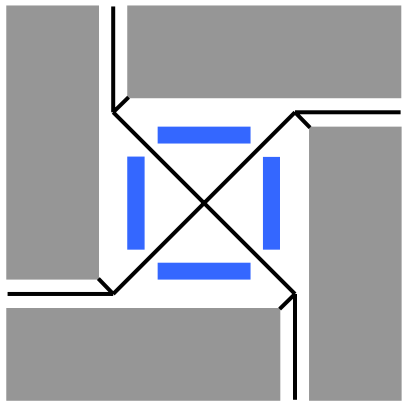
- Mukherjee et al., “The problem of optimal placement of sub-resolution assist features (SRAF),” SPIE-05, vol. 5754.
  - The Voronoi diagram is used to prevent possible conflicts in a two-dimensional SRAF placement.



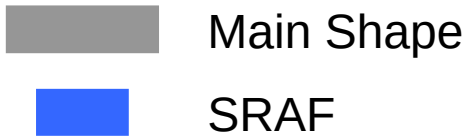
SRAFS One-Dimensional Rules



Traditional Method

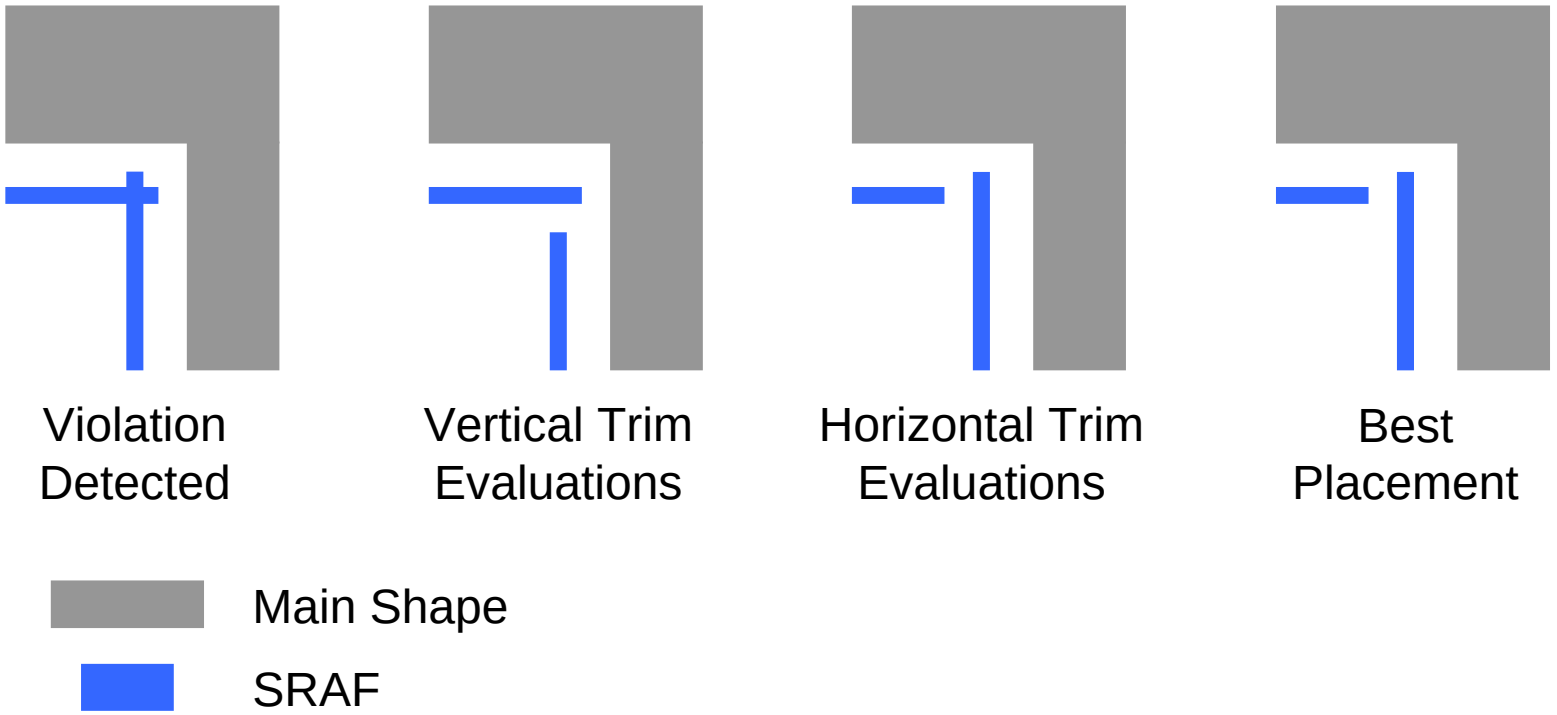


Voronoi Diagram



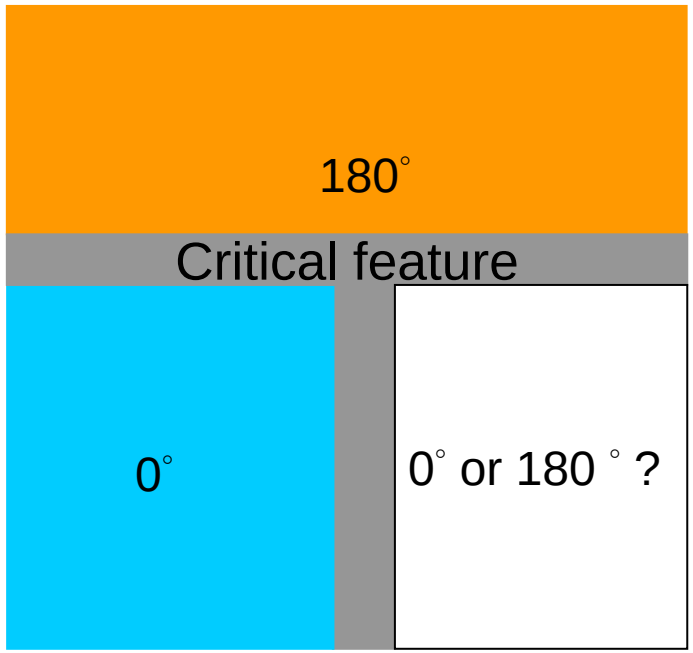
2D SRAF Placement by Model Evaluations

- Barnes et al., “Model-based placement and optimization of sub-resolution assist features,” SPIE-06, vol. 6154.
  - A model-based conflict resolution is performed, also to prevent possible conflicts in a two-dimensional SRAF placement.



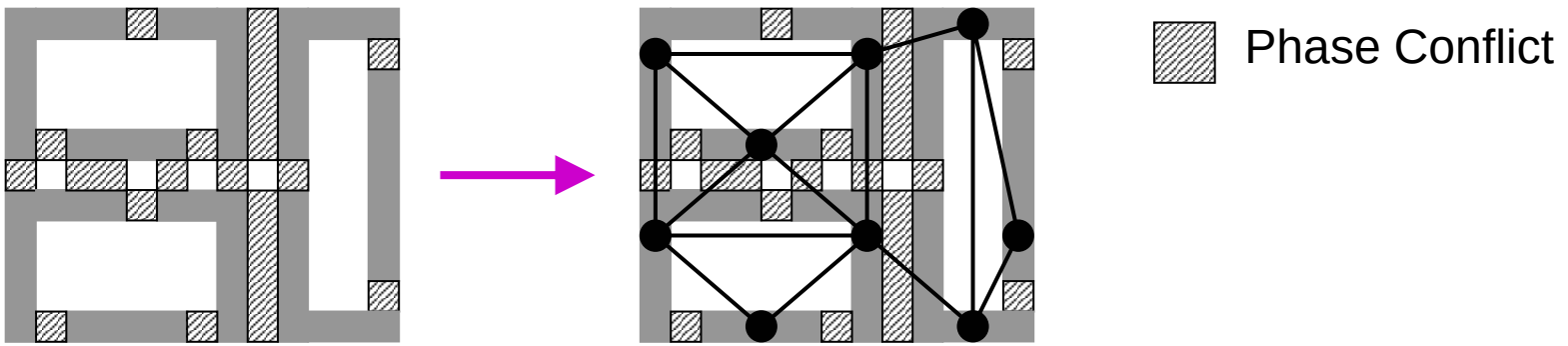
Phase Conflict Problem in PSM

- Phase conflict problem:
  - A pair of phase shifters of both sides of each critical feature must be assign to opposite phases. This phase assignment is not always achievable.



Phase Conflict Removal (1/2)

- Berman et al., “Optimal phase conflict removal for layout of dark field alternating phase shifting masks,” TCAD-2K, vol. 18.
  - A layout modification and phase-assignment algorithm is presented for dark-field AltPSM.
  - The algorithm first constructs a graph to account for phase conflicts, and then deletes a set of edges with the minimum total weight to remove odd cycles as many as possible.



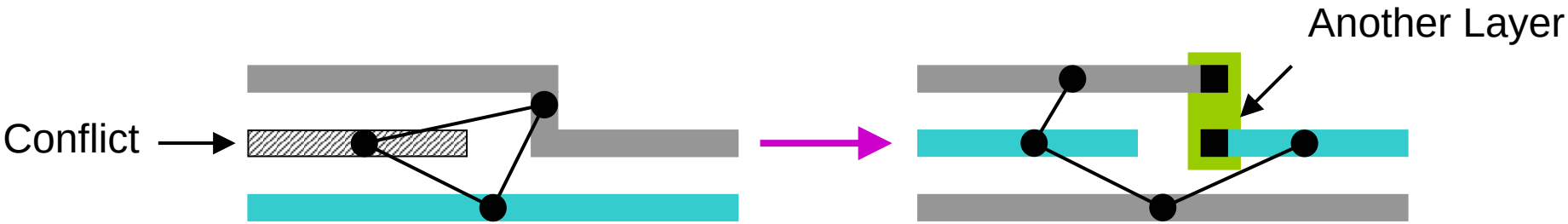
Phase Conflict Removal (2/2)

- Chiang et al., “Fast and efficient phase conflict detection and correction in standard-cell layouts,” ICCAD-05.
  - A new algorithm is presented to solve the phase-conflict problem for the bright-field AltPSM.
  - The problem is formulated as a minimum weighted conflict-cycle removal problem.
- Cao et al., “Library cell layout with Alt-PSM compliance and composability,” ASP-DAC-05.
  - The phase-conflict problems are divided into intra-cell compliance and inter-cell composability problems from the viewpoint of cell-library design.
  - Both the problems are formulated as Boolean satisfiability (SAT) problems solved by a SAT solver.

Phase Correct Routing

- McCullen, “Phase correct routing for alternating phase shift masks,” DAC-04.
  - A phase-correct routing algorithm for the dark-field AltPSM is proposed.
  - Some phase conflicts are solved by widening the distance between two line ends, or moving the wiring jog to another layer.

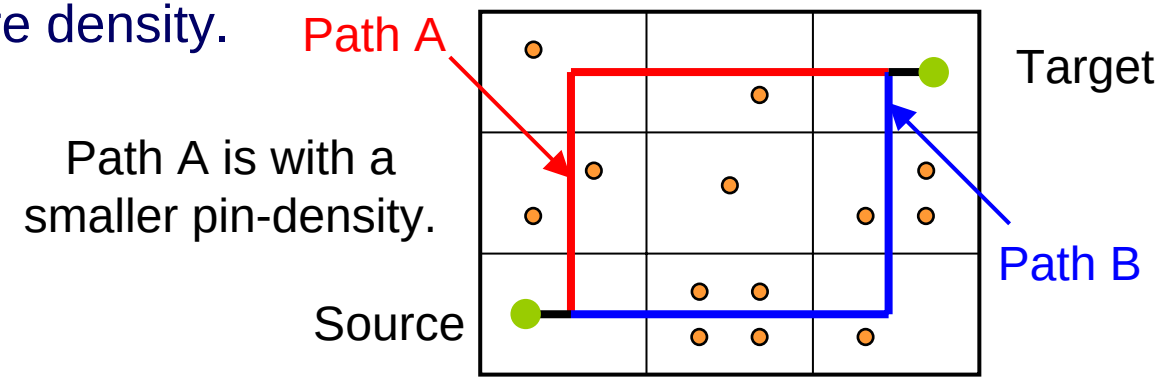
Widening the distance between two lines



Moving the wiring jog to another layer

CMP

- Li et al., “Multilevel full-chip routing with testability and yield enhancement,” SLIP-05.
  - It is the first routing system addressing the CMP induced variation.
  - By setting the desired density in the cost function of global routing, the routing results have more balanced interconnect distribution.
- Cho et al., “Wire density driven global routing for CMP variation and timing,” ICCAD-06.
  - It considers CMP variation during global routing.
  - A predicted CMP density model is empirically developed.
  - A minimum pin-density algorithm is proposed to reduce the maximum wire density.



Double-Via Aware Maze Routing

- Xu et al.,“Redundant-via enhanced maze routing for yield improvement,” ASP-DAC-05.
  - It is the first work to consider double-via insertion during maze routing.
  - A grid based sequential routing algorithm is proposed while considering the feasibility of redundant via insertions.
  - A multi-objective maze routing problem is formulated and solved by Lagrangian relaxation.

Double-Via Aware Routing

- Chen et al., “Novel full-chip gridless routing considering double-via insertion,” DAC-06.
  - The router applies a routability-driven multi-level routing framework.
  - The cost of a net is defined as a weighted sum of the number of vias and related penalty for the net.
  - A post-layout double-via insertion algorithm based on bipartite graph matching, is also proposed.

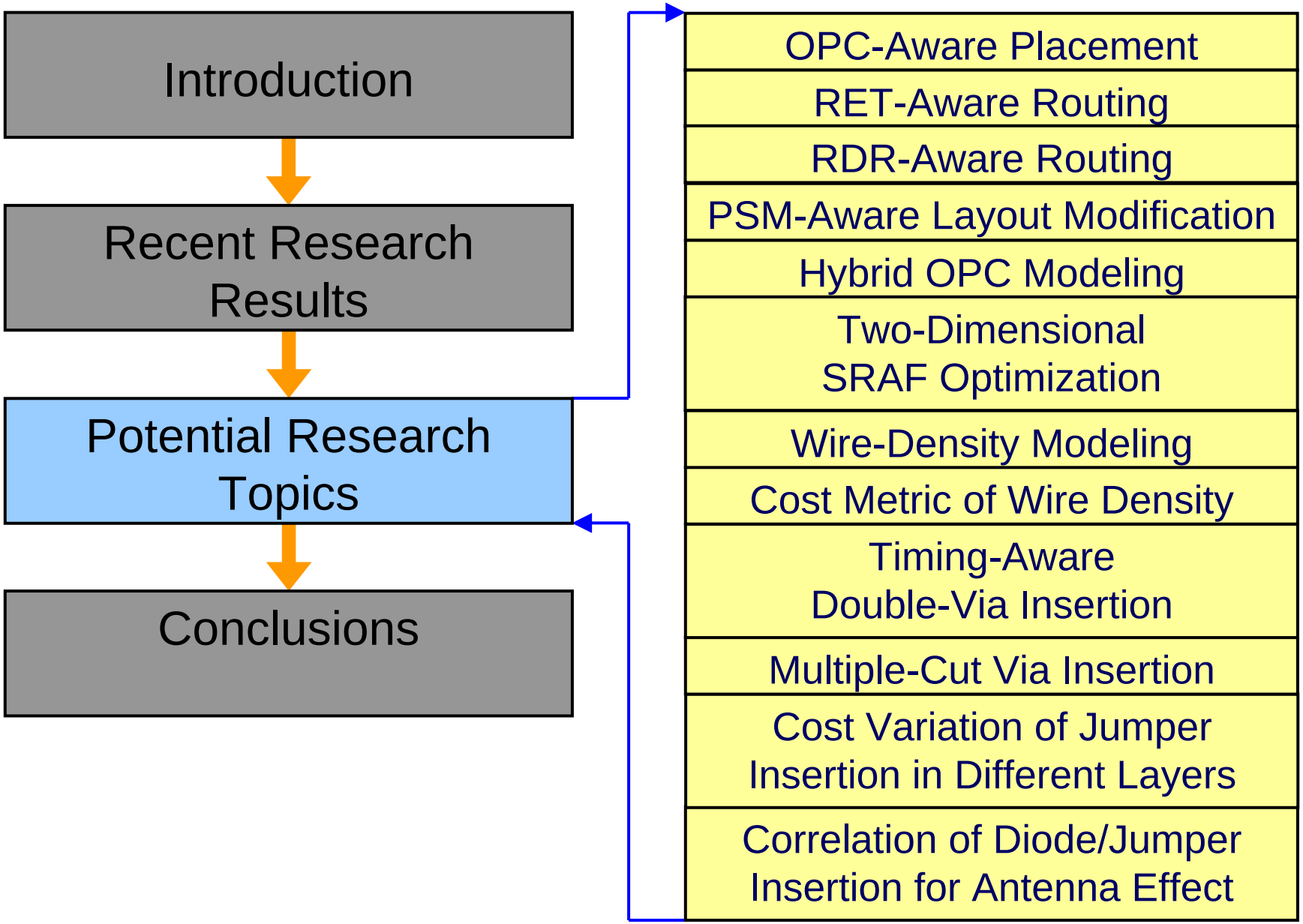
Post-Layout Double-Via Insertion

- Lee and Wang, “Post-routing redundant via insertion for yield/reliability improvement,” ASP-DAC-06.
  - The double-via insertion problem is formulated as a maximum independent-set (MIS) problem and solved by heuristic.
- Luo et al., “Yield-preferred via insertion based on novel geotopological technology,” ASP-DAC-06.
  - The single vias of a design is considered one by one to perform redundant-via insertion.
- Lee et al., “Post-routing redundant via insertion and line end extension with via density consideration,” ICCAD-06.
  - It addresses the problem of simultaneously performing redundant-via insertion and line-end extension under via-density consideration.

Diode/Jumper Insertion for Antenna Effect

- Su and Chang, “An exact jumper insertion algorithm for antenna effect avoidance/fixing,” DAC-05
  - The jumper insertion for antenna avoidance/fixing is formulated as a tree-cutting problem.
  - It is shown that the tree-cutting problem exhibits the properties of optimal substructures and greedy choices.
- Jiang and Chang, “An optimal simultaneous diode/jumper insertion algorithm for antenna fixing,” ICCAD-06.
  - An optimal simultaneous diode/jumper insertion algorithm is presented based on a minimum-cost network-flow formulation,
  - It achieves much higher antenna fixing rates than the other works with jumper insertion or diode insertion alone.

Outline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RDR-Aware Routing
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Cost Metric of Wire Density
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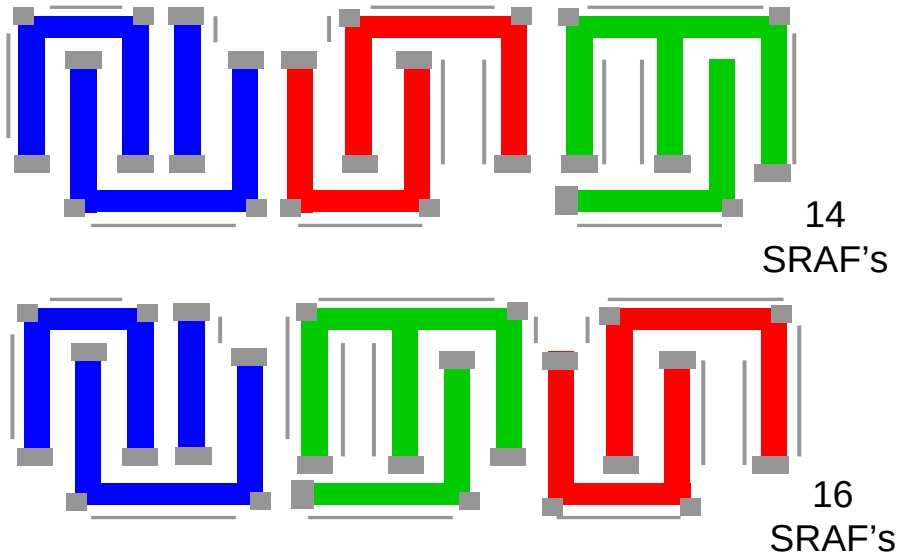
Multiple-Cut Via Insertion
Cost Variation of Jumper Insertion in Different Layers
Correlation of Diode/Jumper Insertion for Antenna Effect

1. OPC-Aware Placement

- Placement results affect the mask design and the final yield.
- An OPC-friendly placement can greatly reduce the computational time and the size of mask database.

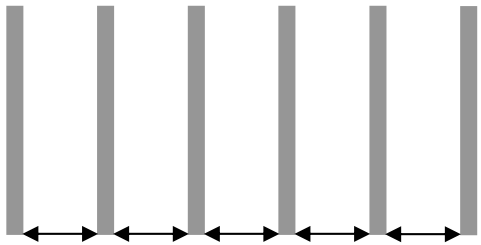


2. RET-Aware Routing

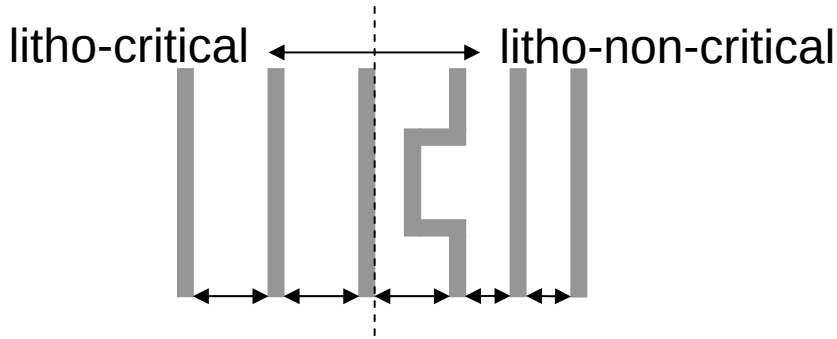
- Although RET-aware routing has been studied to some degree, there is still much room for research in this topic.
  - It is desired to develop a technique that can accurately predict RET behaviors.
  - The router can consider OPC, PSM, or more than one RET at the same time.
- Since the simulation for RET behaviors is very time-consuming, the efficiency should always be considered.

3. RDR-Aware Routing

- Restricted design rules (RDRs) appears to enhance manufacturability by restricting produced layouts.
  - Using only regular features in a layout will improve lithographic printability and make RETs easier to implement.
  - Since over-restricted rules may decrease the performance and increase the area, it is difficult to strictly follow RDRs in practice.
- An appropriate RDR-aware router should:
  - Follow RDRs in lithographically critical regions, and
  - Allow some exceptions of RDRs in non-critical regions to optimize the performance and the chip area.



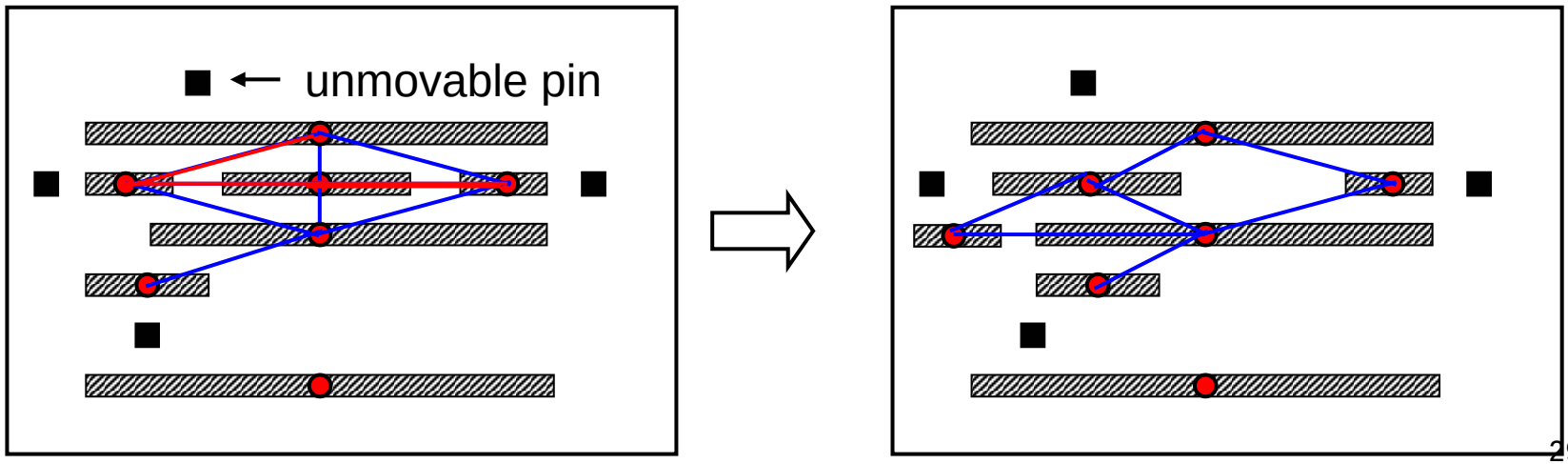
They are restricted by RDRs to be placed on the fixed pitch.



An appropriate router should consider other metrics.

4. PSM-Aware Layout Modification

- Existing approaches solve this problem in two separate steps: deleting a set of edges with minimum total cost from the graph to remove odd cycles, and then modifying the layout according to the removed edges.
  - However, they cannot guarantee that the layout can be always modified to comply with these edge deletions without enlarging the layout size.
- It is still in need to develop an algorithm that can simultaneously consider odd cycle removal and layout modification.

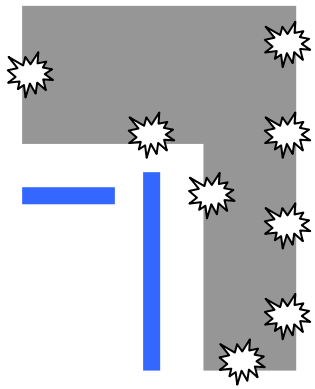


5. Hybrid OPC Modeling

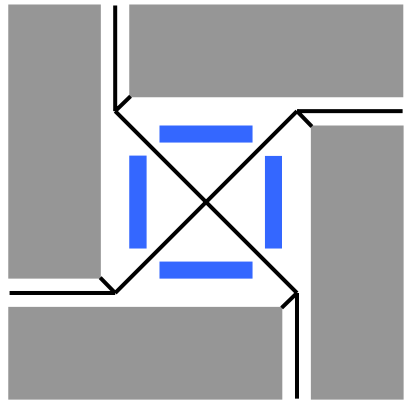
- There are two general types of OPC systems, rule-based OPC and model-based OPC.
  - A rule-based OPC determines how to apply OPC by given rules.
  - A model-based one used mathematical models of the fabrication process.
- There is a trade-off between accuracy and efficiency.
  - A rule-based OPC is usually more efficient but less accurate than a model-based OPC.
- A hybrid OPC balancing the two important factors is desired.
  - It can also play an important role to guide an OPC-aware router with sufficient accuracy and efficiency at the same time.

6. Two-Dimensional SRAF Optimization

- To prevent two-dimensional SRAF placement conflicts, existing works apply the Voronoi diagram or a model-based conflict resolution.



Model Evaluations

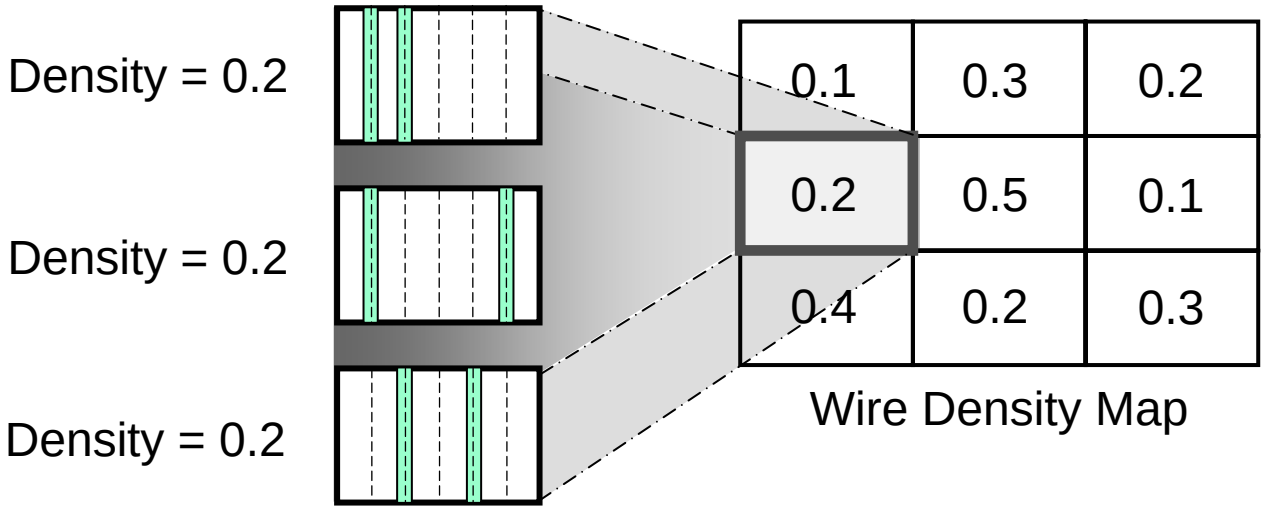


Voronoi Diagram

- There is still no well-formulated problem being proposed to deal with this two-dimensional conflict problem.
  - The challenges of the SRAF placement include the number, sizes, and positions of SRAFs.
  - The distances from SRAFs to the main shapes and those between SRAFs are also constrained.

7. Wire-Density Modeling

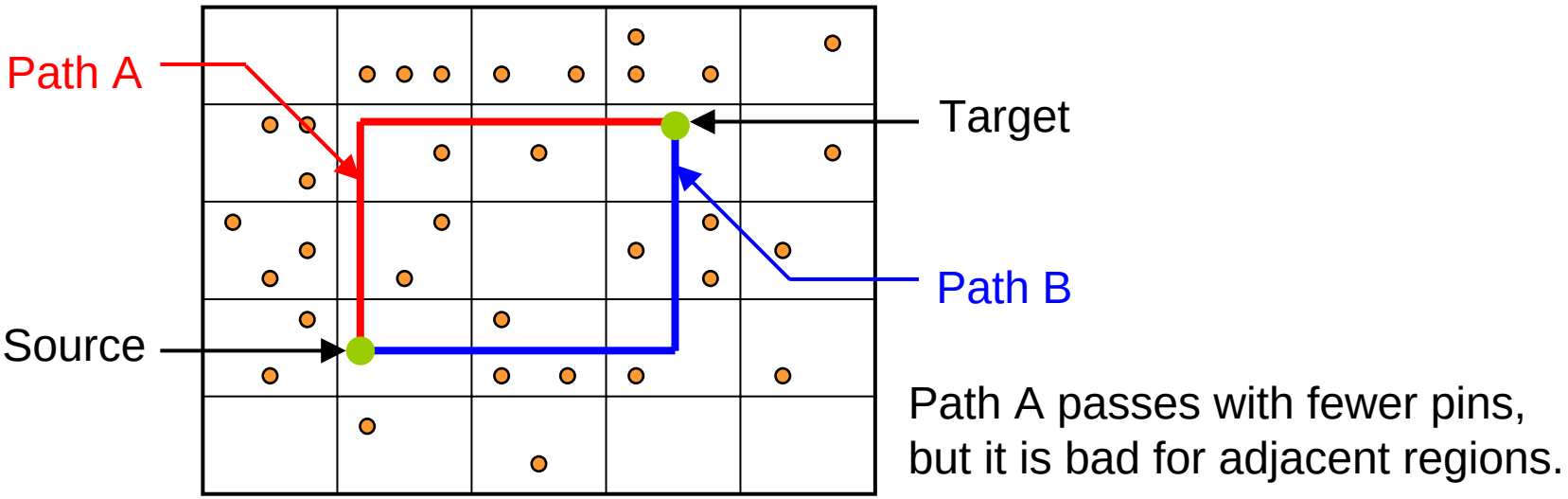
- For a better CMP process, existing approaches consider the wire density inside each global-routing tile.
  - Handling density only in a global-routing tile may incur large density variations among neighboring tiles.
  - As a result, the density variations between neighboring subregions are not controlled.



- The modeling of wire density should be reconsidered at a more global perspective.

8. Cost Metric of Wire Density

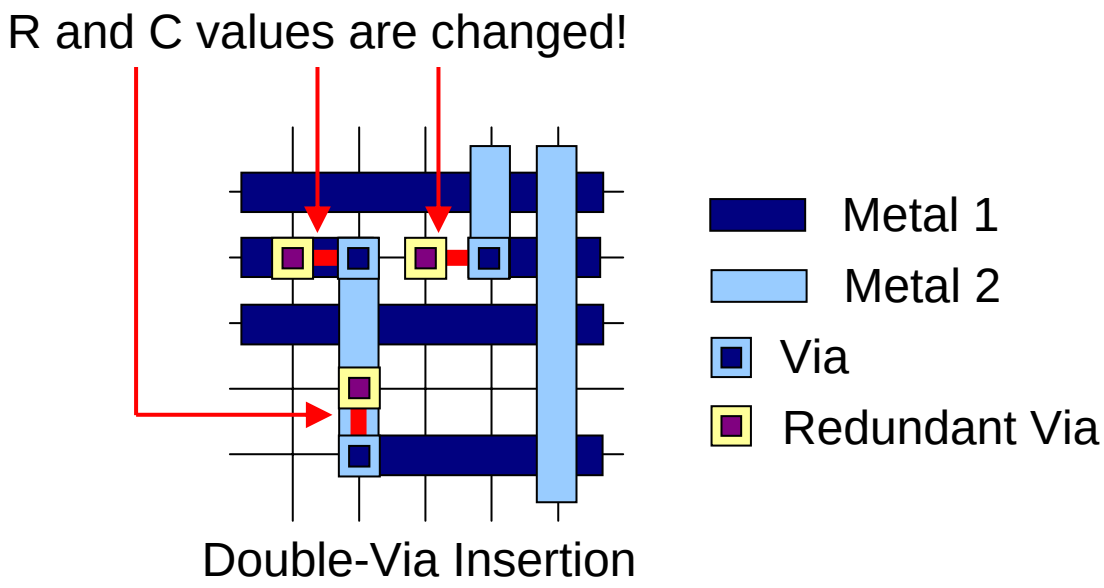
- A minimum pin-density routing is proposed to avoid global-routing paths from passing through over-dense areas.
  - Although the routing path passes a region with fewer pins, it may exacerbate the over-dense areas in its adjacent regions.



- Most existing works try to optimize the wire density for a given window for CMP control.
  - This is not a right metric and a common pitfall for CMP control.
  - It is more desirable to minimize the variation of wire density.

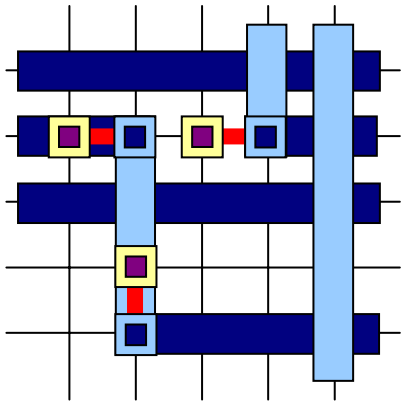
9. Timing-Aware Double-Via Insertion

- The addition of redundant vias could change the timing behavior of a design positively and negatively.
  - Some path delays may increase while some others may decrease.
  - Existing works cannot guarantee that the resulting design can still satisfy timing constraints after applying their approach.
- How to tackle the timing issue more accurately during double-via insertion is still worthy for further study.

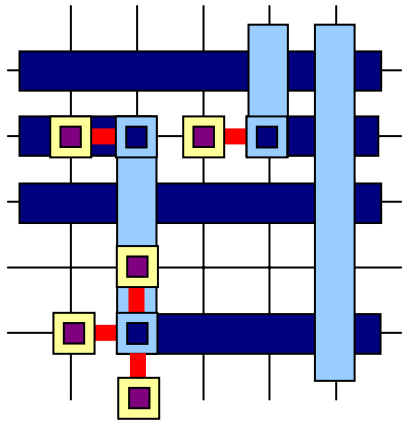


10. Multiple-Cut Via Insertion

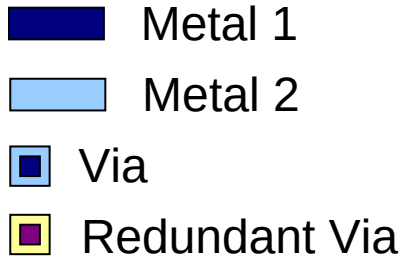
- For high-activity, high-current, and power nets, more than one redundant via is usually desired to be inserted.
  - How to efficiently and effectively insert multiple-cut vias for those nets is also an interesting problem.
  - The single vias located on the lower layers generally have smaller dimensions and hence have higher probability of becoming invalid.
  - The lower-layer vias should have higher priority for adding redundant vias than the others.



Double-Via Insertion

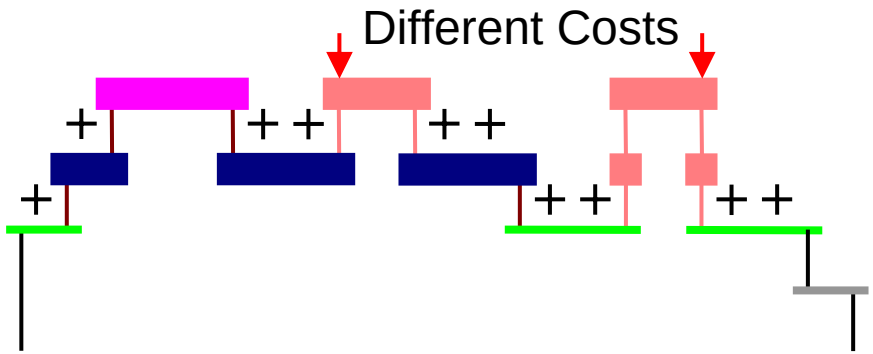


Multiple-Cut Via Insertion



11. Cost Variation of Jumper Insertion in Different Layers

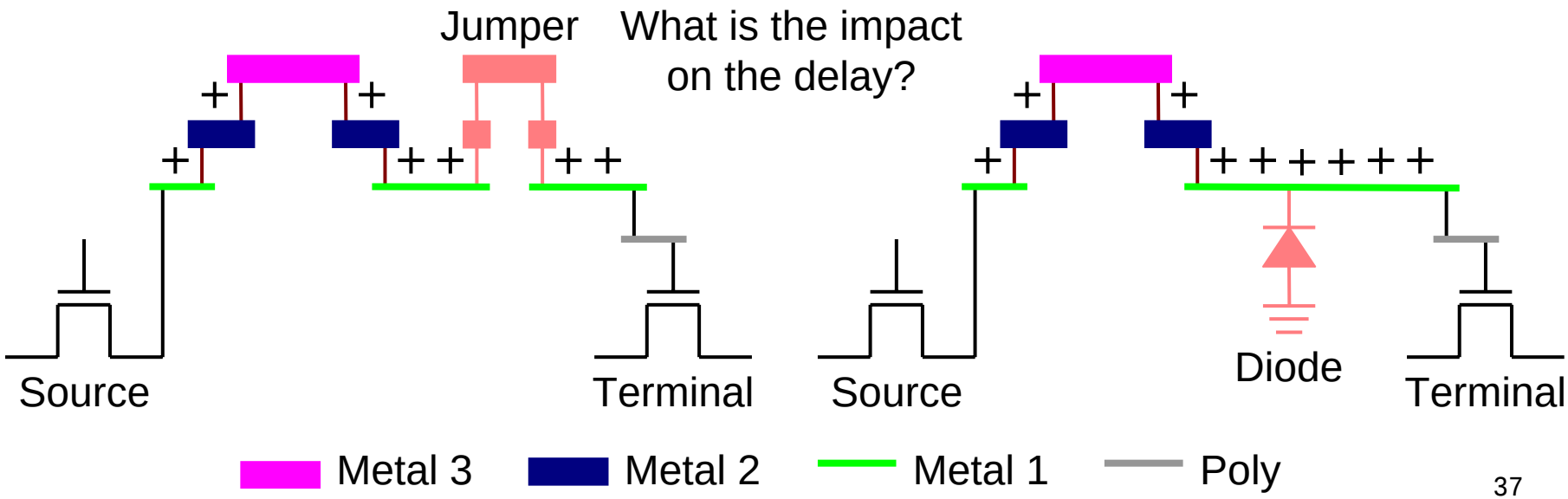
- Jumper insertion reroutes nets to the top-metal layer.
  - Previous works do not consider the cost difference in adding a jumper from different layers to the top-metal layer.
  - The lower jumpers consume vias that cross more metal layers and thus should be assigned larger costs than higher jumpers.



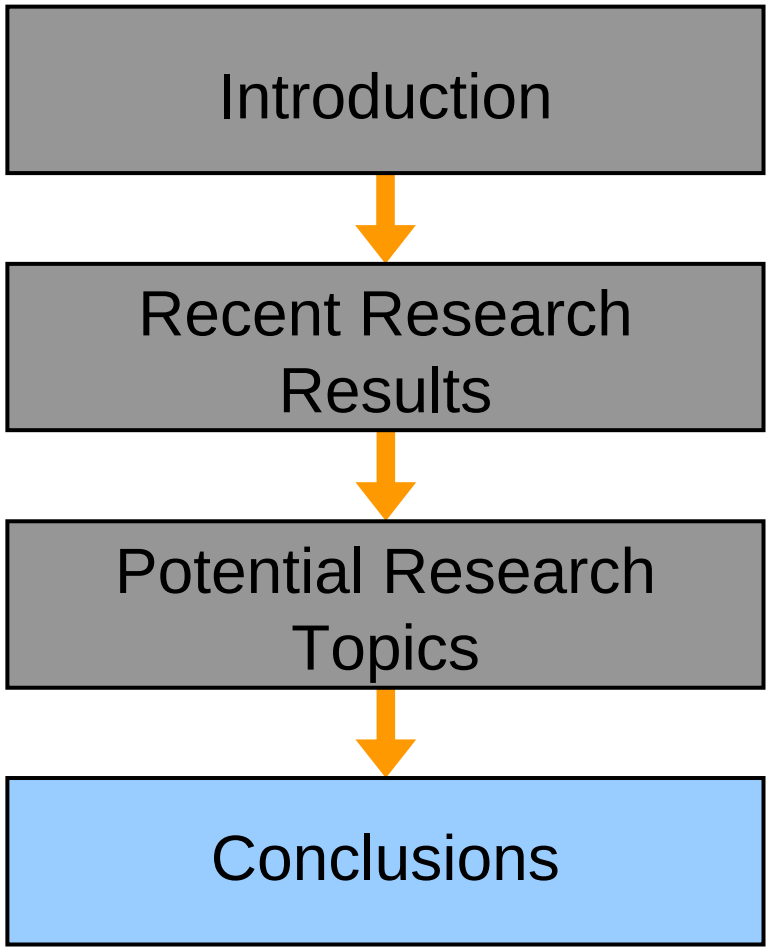
- For the formulated tree-cutting problem, the cost variation would incur two independent weights for each tree edge.
  - One is for the antenna charge, and the other is for the jumper cost.
  - The problem can be formulated as to optimize the total jumper cost such that the antenna rules are satisfied.

12. Correlation of Diode/Jumper Insertion for Antenna Effect

- There are different design costs between diode insertion and jumper insertion.
  - A previous work defines the cost function composed of the total wirelength of extension wires (for diodes) and the total number of jumpers to minimize the total delay.
  - If a more precise delay model is used to calculate the induced total delay, the cost function for the problem may be different.
- New algorithms is needed to solve this problem.



Outline


Introduction
Recent Research Results
Potential Research Topics
Conclusions

Conclusions

- With the imperfect manufacturing process, yield and reliability have become first-order cost metrics.
- Physical design plays an essential role to ensure the success of manufacturing and improve yield and reliability.
- Many existing works have shown the effectiveness of physical design for this requirement.
- There are still many opportunities for future research to further improve the manufacturability and reliability of the final designs.