LeAF: A Leakage- Aware Floorplanner

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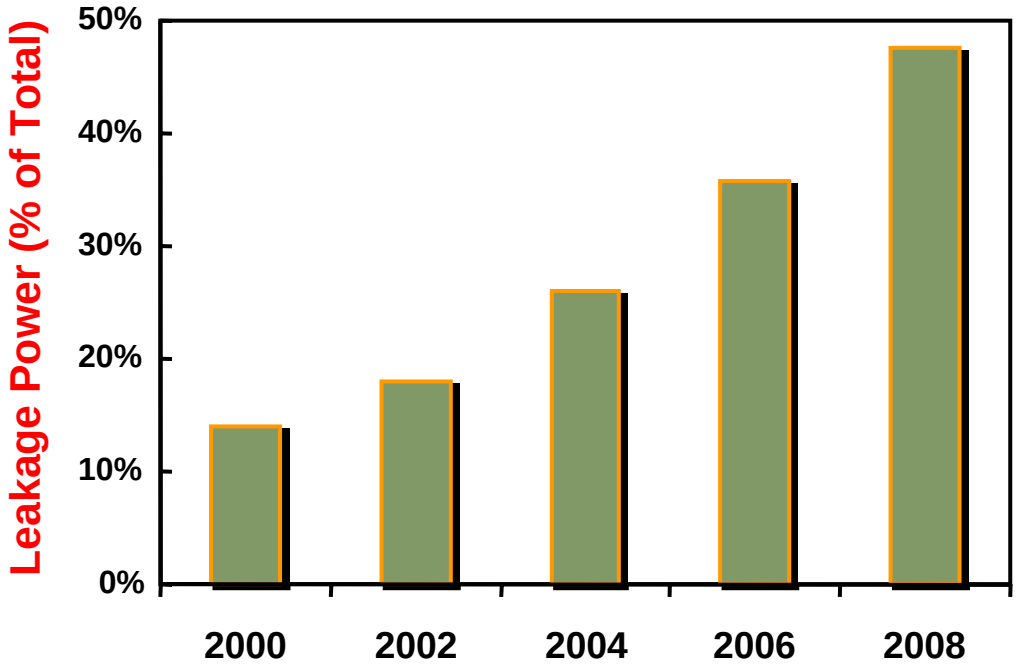
freescale semiconductor

Why worry about power? – Leakage Power

Year	2002	2005	2008	2011	2014
Power supply V_{dd} (V)	1.5	1.2	0.9	0.7	0.6
Threshold V_T (V)	0.4	0.4	0.35	0.3	0.25

As V_T is decreased to maintain noise margins and to meet frequency demands, the leakage current will increase leading to excessive battery draining.



…and phones leaky!

Source: Borkar, De Intel®

Leakage Power

- Leakage power is more than 50% of the total power in many chips.
- Major component of leakage power is sub-threshold current.
- Sub-threshold leakage current is sensitive to temperature.
- Leakage power of an industrial core at 65nm:

Core	Case (Voltage)	Leakage Power (% of Total Power)	
		85 ºC	105 ºC
400 MHz	Worst (0.9V)	20% →	46%
	Typical (1.0V)	17% →	40%
	Best (1.1V)	25% →	**53%**

- Leakage power more than doubles with a 20ºC increase in the temperature of the die.

Source: Freescale Semiconductor®

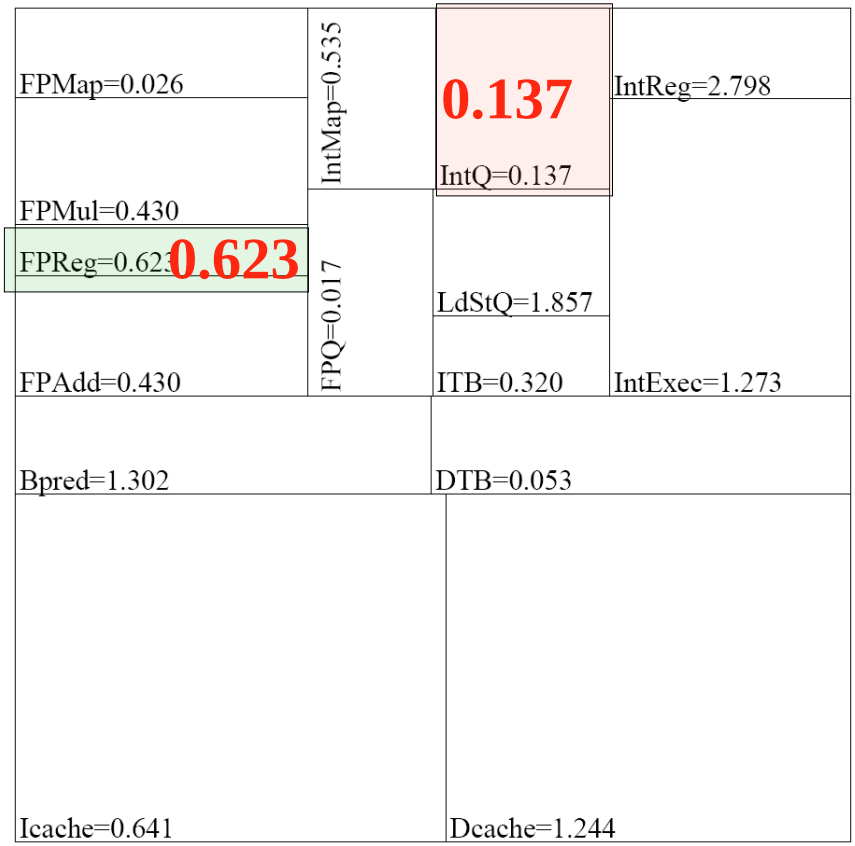
Thermal Characteristics of a Chip

- Power densities are increasing with smaller geometries leading to increased chip temperatures.
- Temperature difference across a SoC can be as high as 50ºC.
- The heat of a IP-block is not confined to itself and effects other blocks also:
  - Thermal Diffusion
  - Heat flows from high temperature block to low temperature blocks.
- Floorplan of SoC affects temperatures of the IP-blocks.

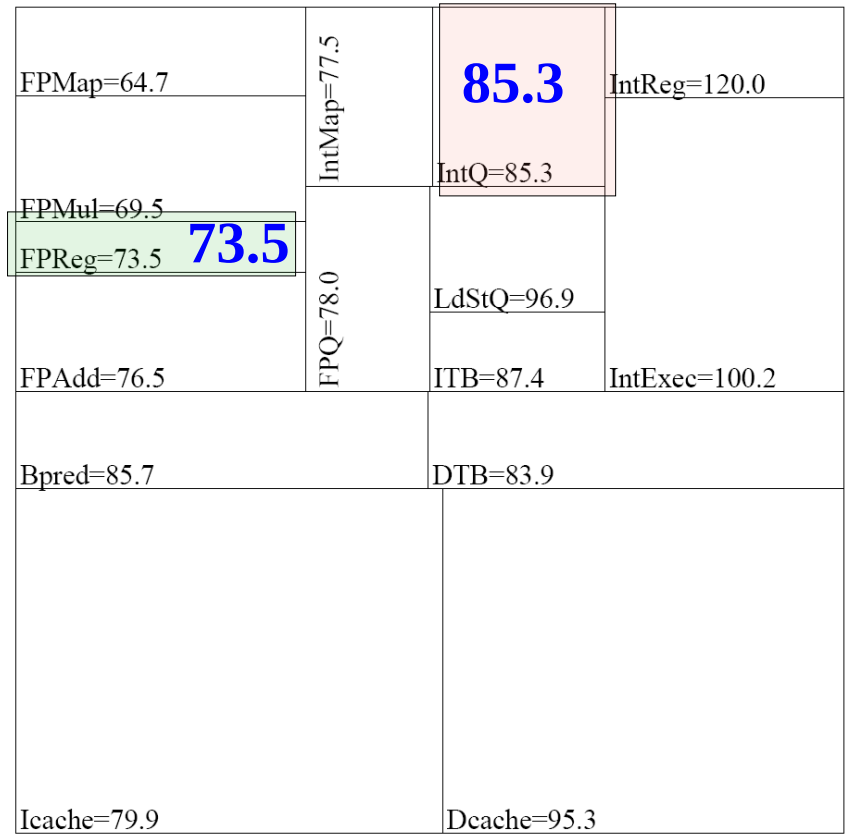
Thermal Diffusion

- Alpha 21364 Core with gcc benchmark

Power Densities



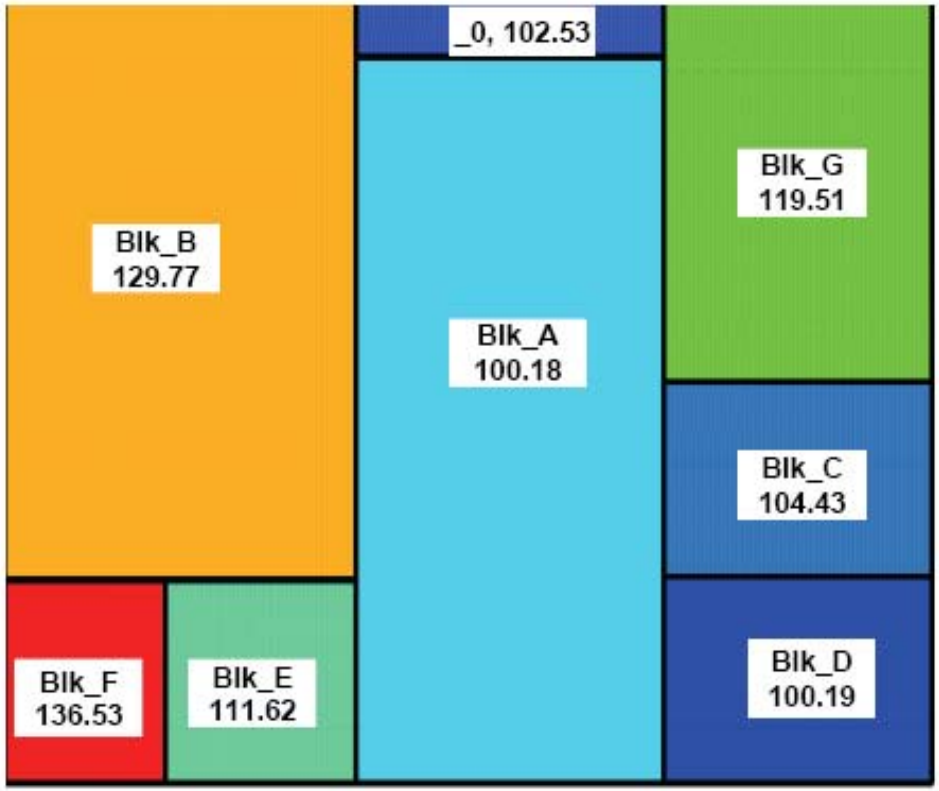
Temperatures

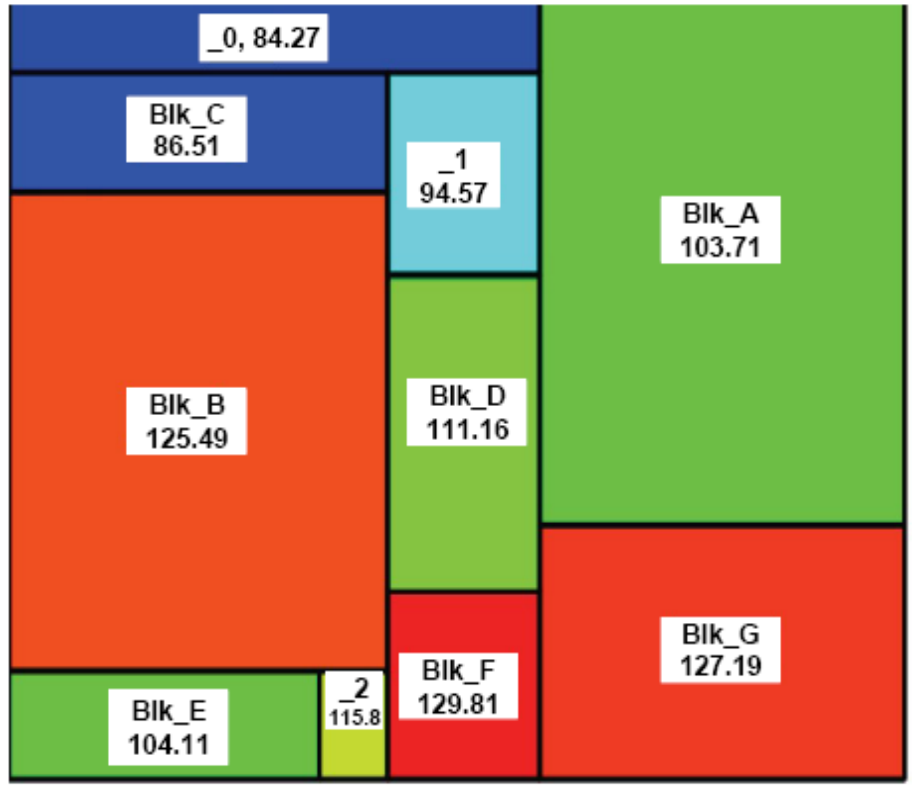


Power densities don't necessarily map to temperatures

[Moritz, Koren]

Temperature & Floorplans





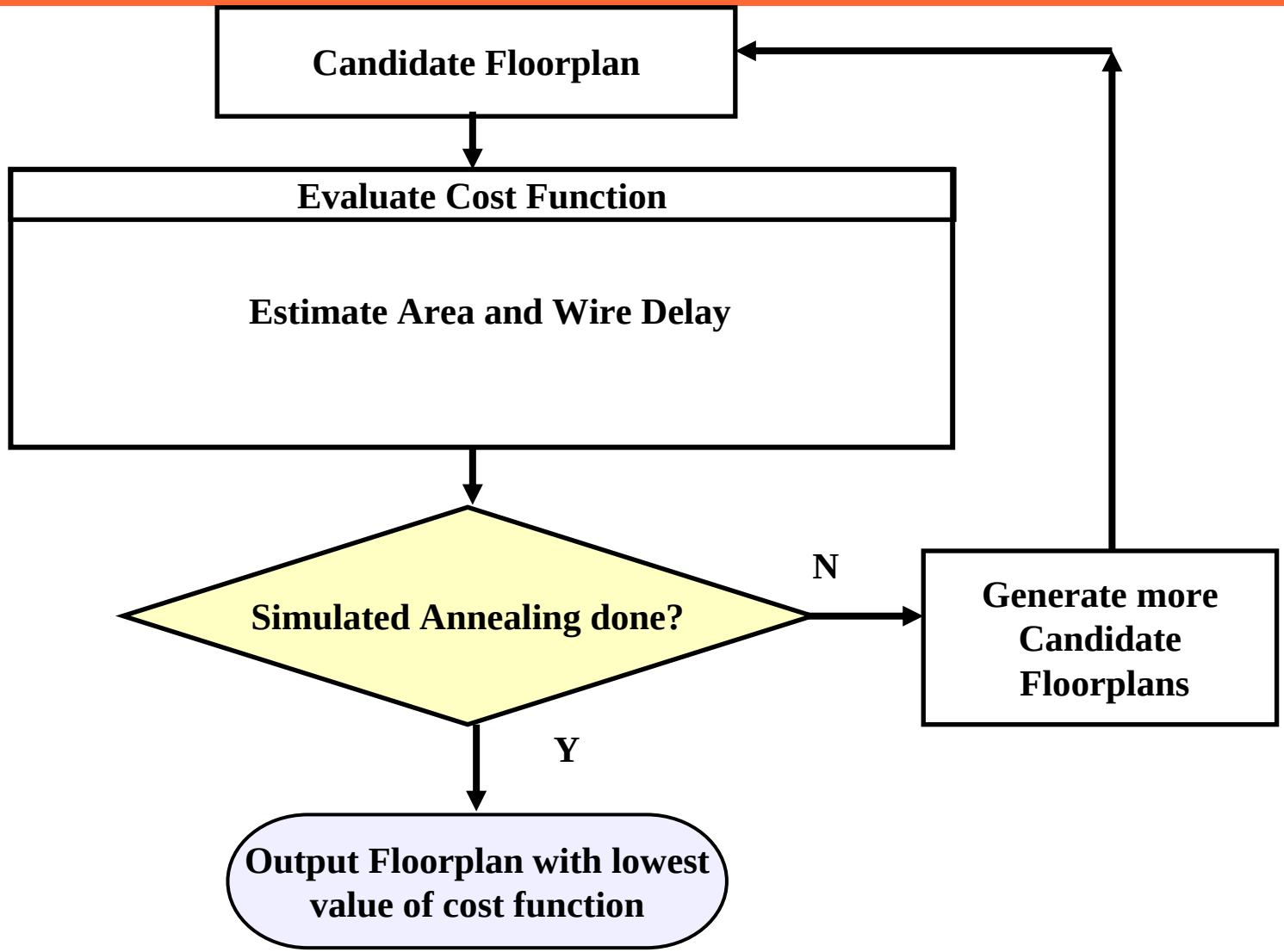
- Thermograms for 2 floorplans of the same SoC look different.
- Significant temperature gradients across the SoC (45°C in right floorplan).
- Leakage power (Temperature dependent) for the two floorplans is different by about 10%.

Problem Definition

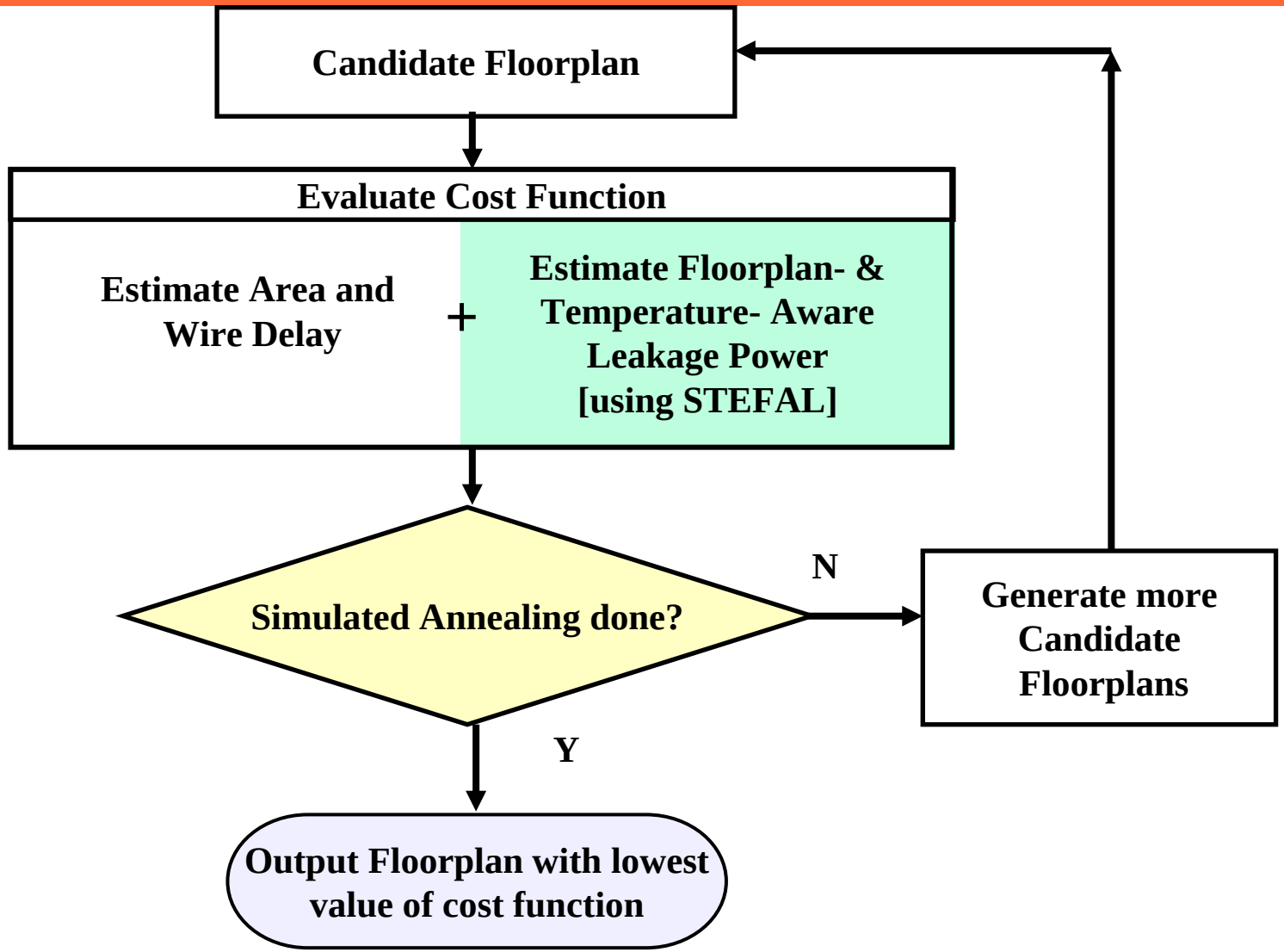
- **Given:**
  - Leakage power is highly dependent on temperature.
  - Different blocks in a SoC are at different temperatures. The effect of thermal diffusion is very significant.
  - There is an interdependency between SoC floorplan, temperature, and leakage power

- **How much is the impact of SoC floorplans on the leakage power?**
- **Can we optimize SoC floorplans for thermal-aware leakage power ?**

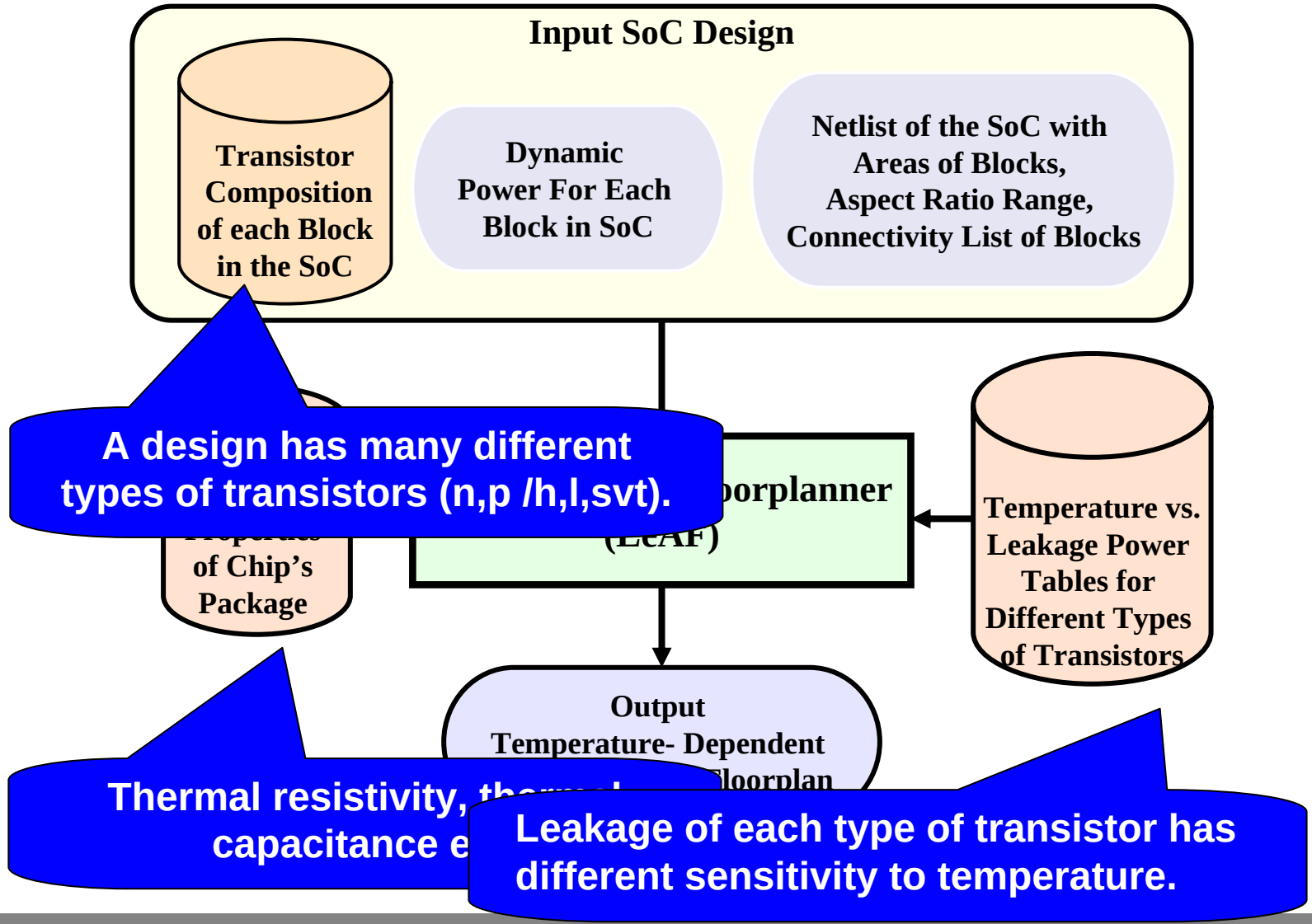
Traditional Floorplanning



Leakage Aware Floorplanning



Minimum changes in any existing floorplanner's optimization algorithm


Input SoC Design
Transistor Composition of each Block in the SoC
Dynamic Power For Each Block in SoC
Netlist of the SoC with Areas of Blocks, Aspect Ratio Range, Connectivity List of Blocks
A design has many different types of transistors (n,p /h,l,svt).
of Chip's Package
oorplanner
(LeAF)
Temperature vs. Leakage Power Tables for Different Types of Transistors
Output
Temperature- Dependent
loorplan
Thermal resistivity,
capacitance e
Leakage of each type of transistor has different sensitivity to temperature.

Cost Function

- All floorplanners' output is optimized for a Cost Function.
- Traditional floorplanner's Cost Function = *f*(Area, Wire Length)
- Cost Function of Leakage Aware Floorplanner = *f*(Area, Wire Length, Leakage Power)
- Leakage Aware Floorplanner additionally optimizes floorplans for temperature dependent leakage power which is estimated using STEFAL.
- Each parameter in the Cost Function has respective weights. Sum of all weights = 1.

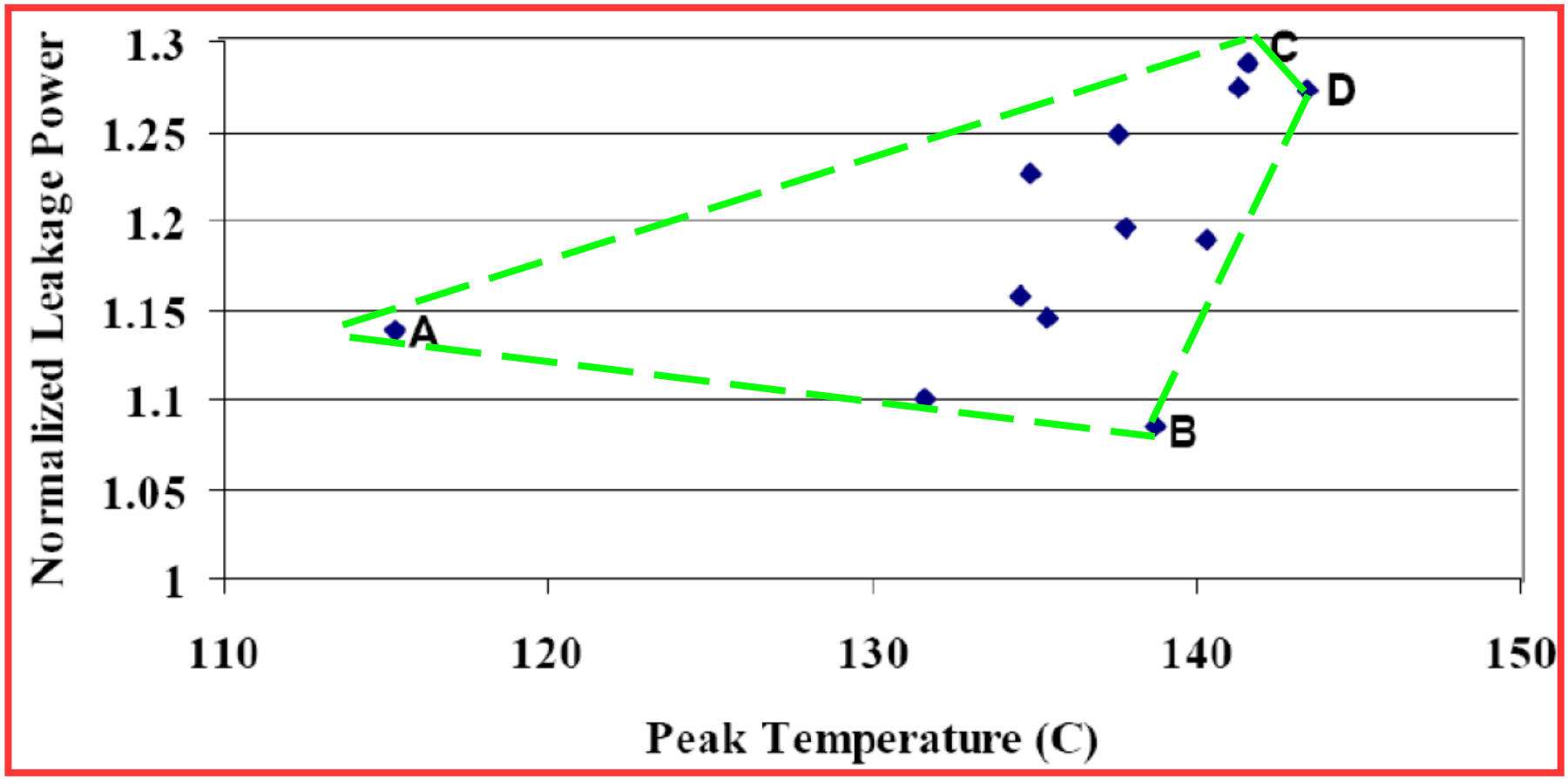
Thermal- vs. Leakage- Aware Floorplanning

- Related work focused on thermal-aware floorplanning:
  - Optimizes floorplans for peak temperature
    - > objective is to reduce the peak temperature of a SoC
  - Peak temperatures affect package design, reliability etc.
  - Reduction of peak temperatures ‘may or may not’ reduce the leakage power
  - It is different from leakage aware floorplanning.

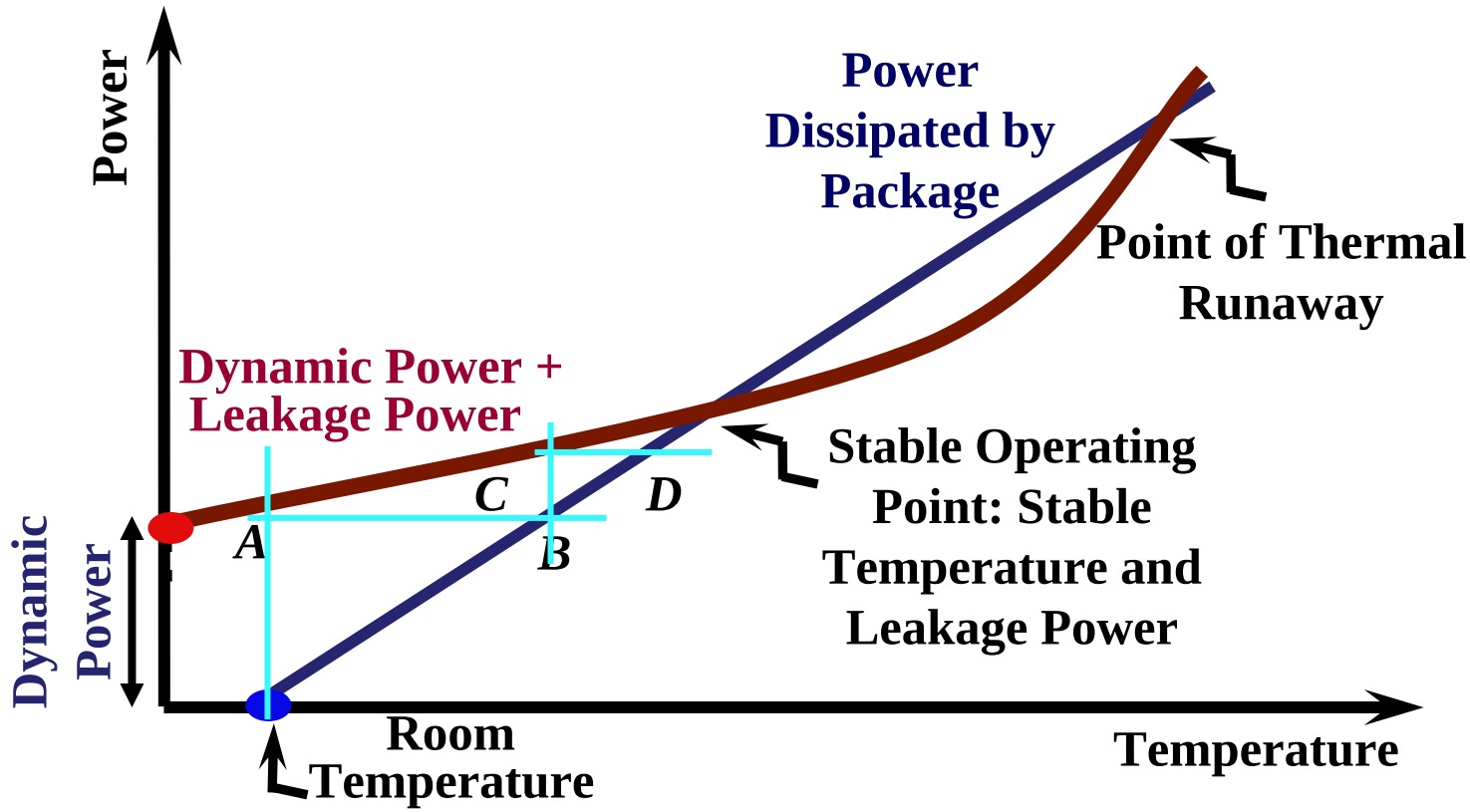
- Leakage-aware floorplanning:
  - Optimizes floorplans for leakage power
    - > objective is to reduce the leakage power of a SoC

Thermal- vs. Leakage- Aware Floorplanning

- Peak temperature and leakage of different floorplans
- No definite correlation between peak temperature and leakage power



Positive feedback between Leakage & Temperature

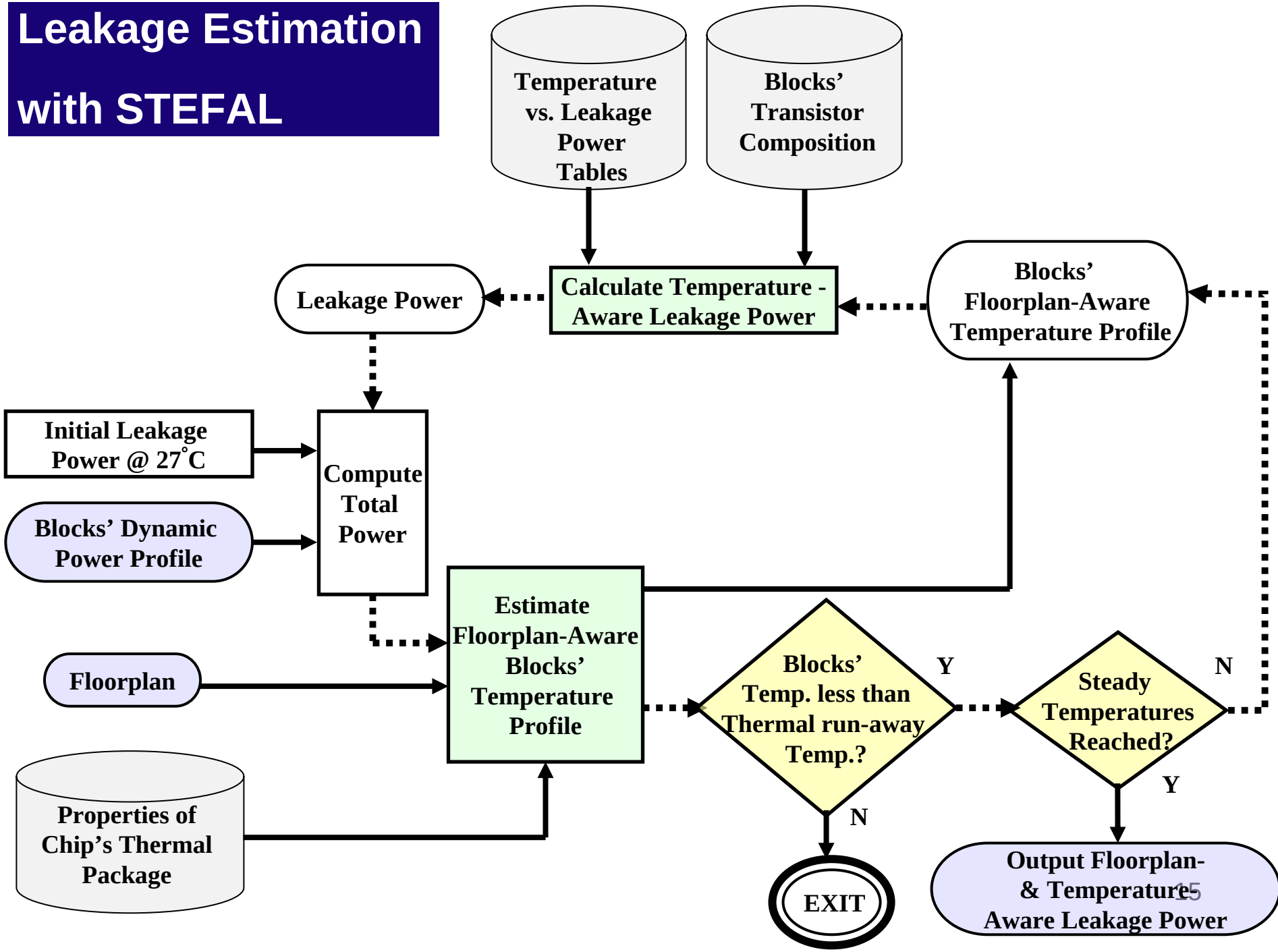


During temperature dependent leakage estimation, this positive feedback cannot be ignored.

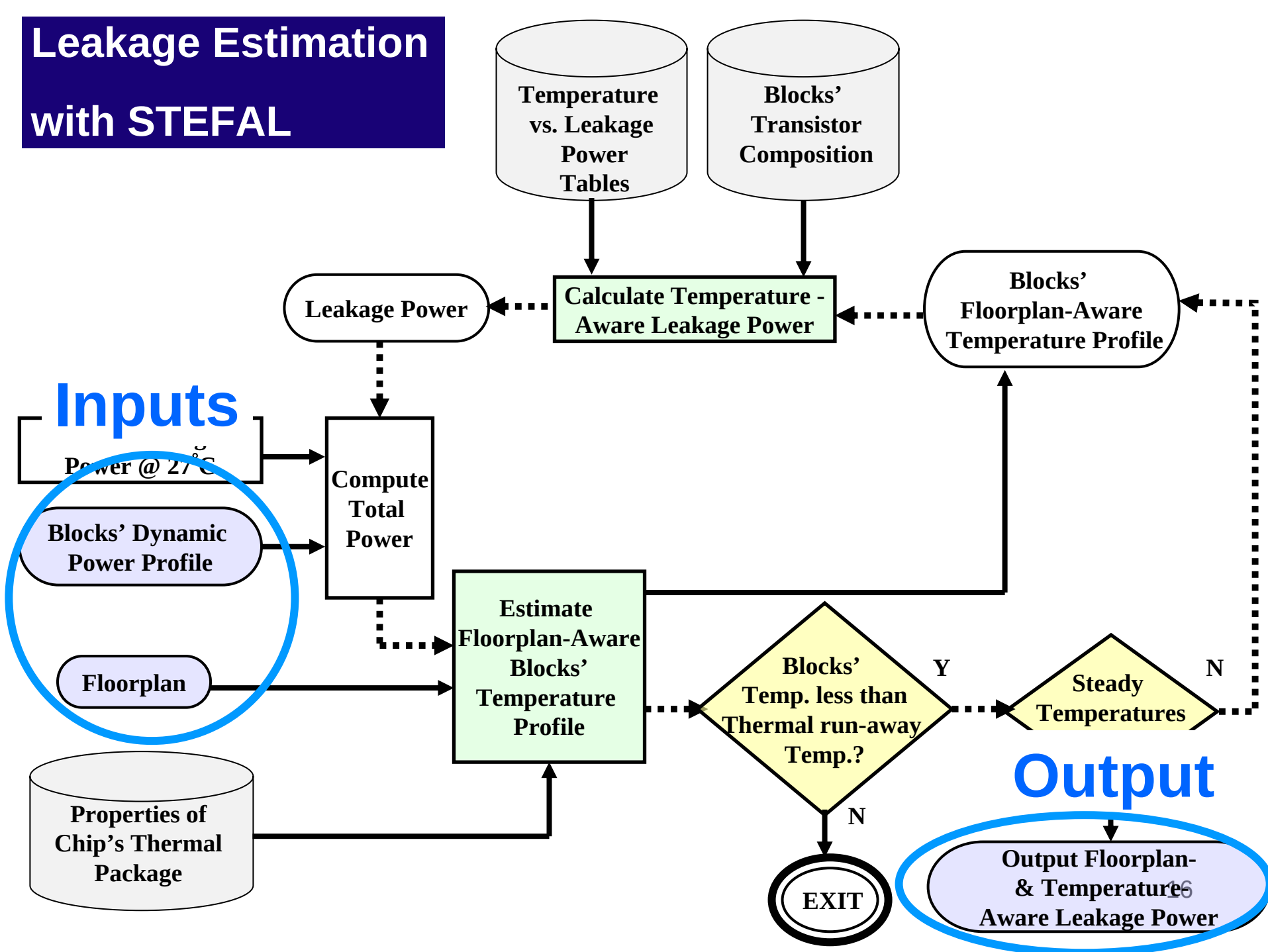
- **S**ystem Level **Te**mperature- and **F**loorplan- **A**ware **L**eakage Power Estimator

- Estimates the leakage power of a SoC:
  - Considers the candidate floorplan of the SoC
  - Considers the actual temperature profile of the SoC
  - Considers positive feedback between leakage and temperature

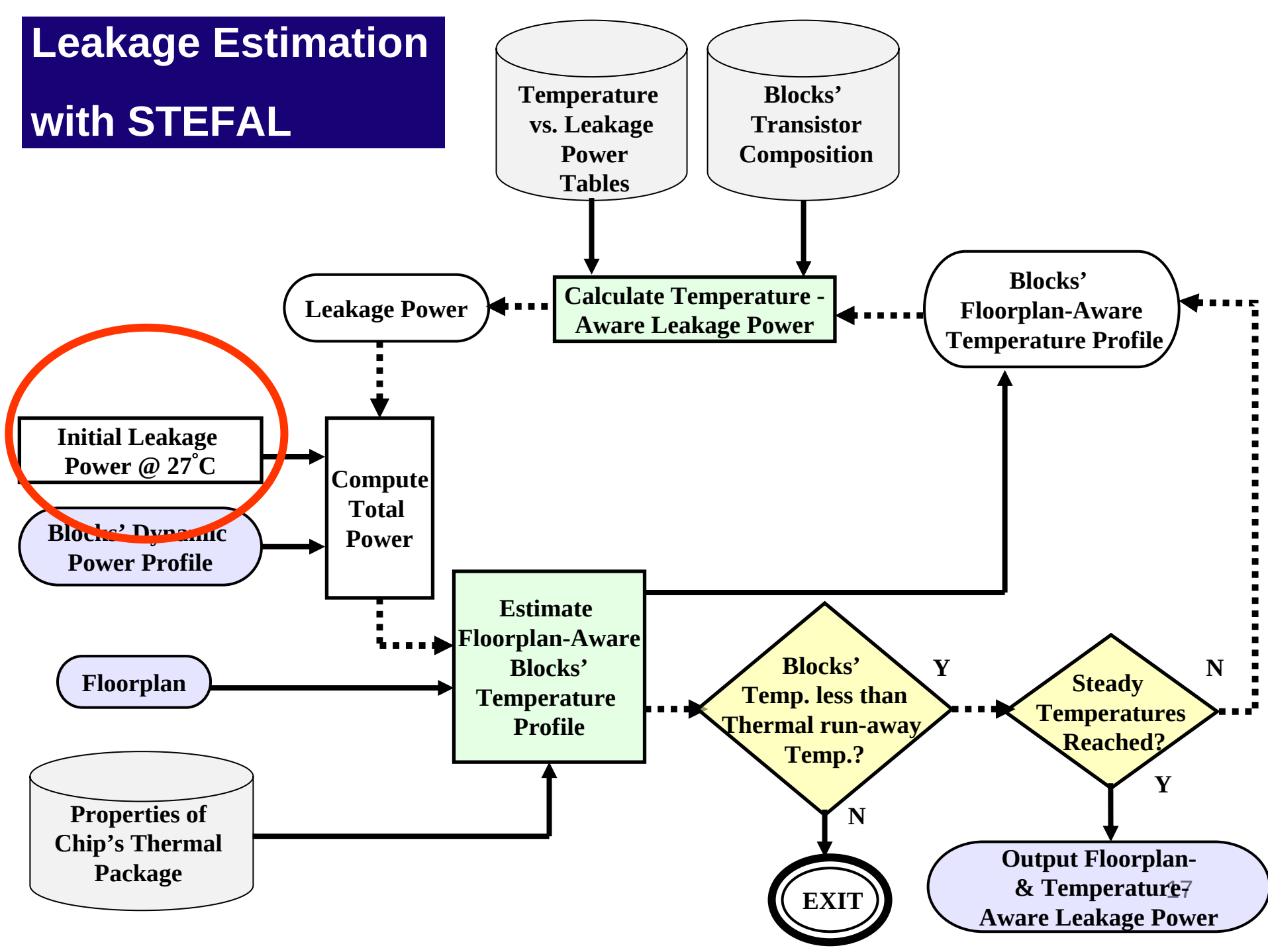
Leakage Estimation with STEFAL



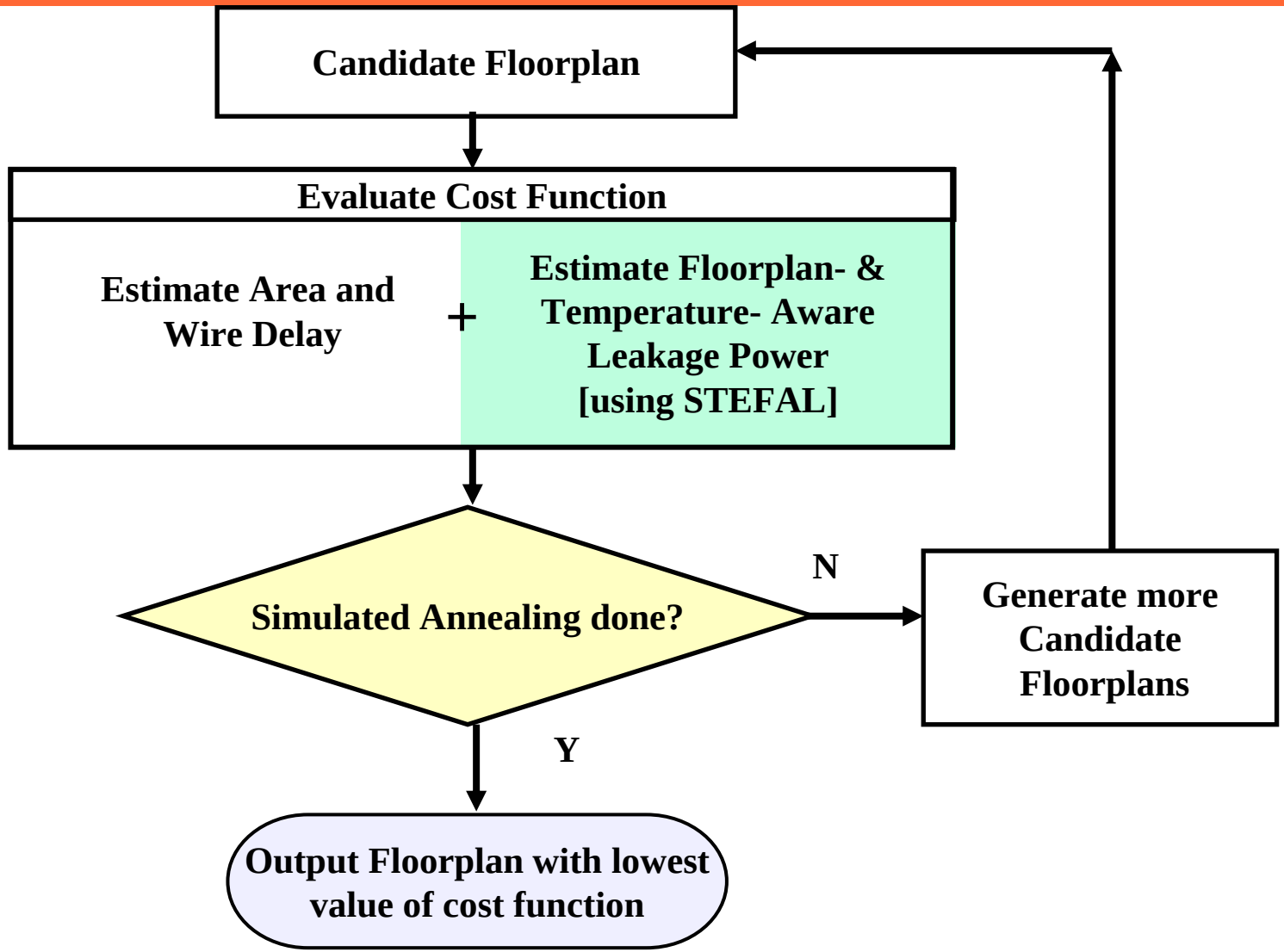
Leakage Estimation with STEFAL



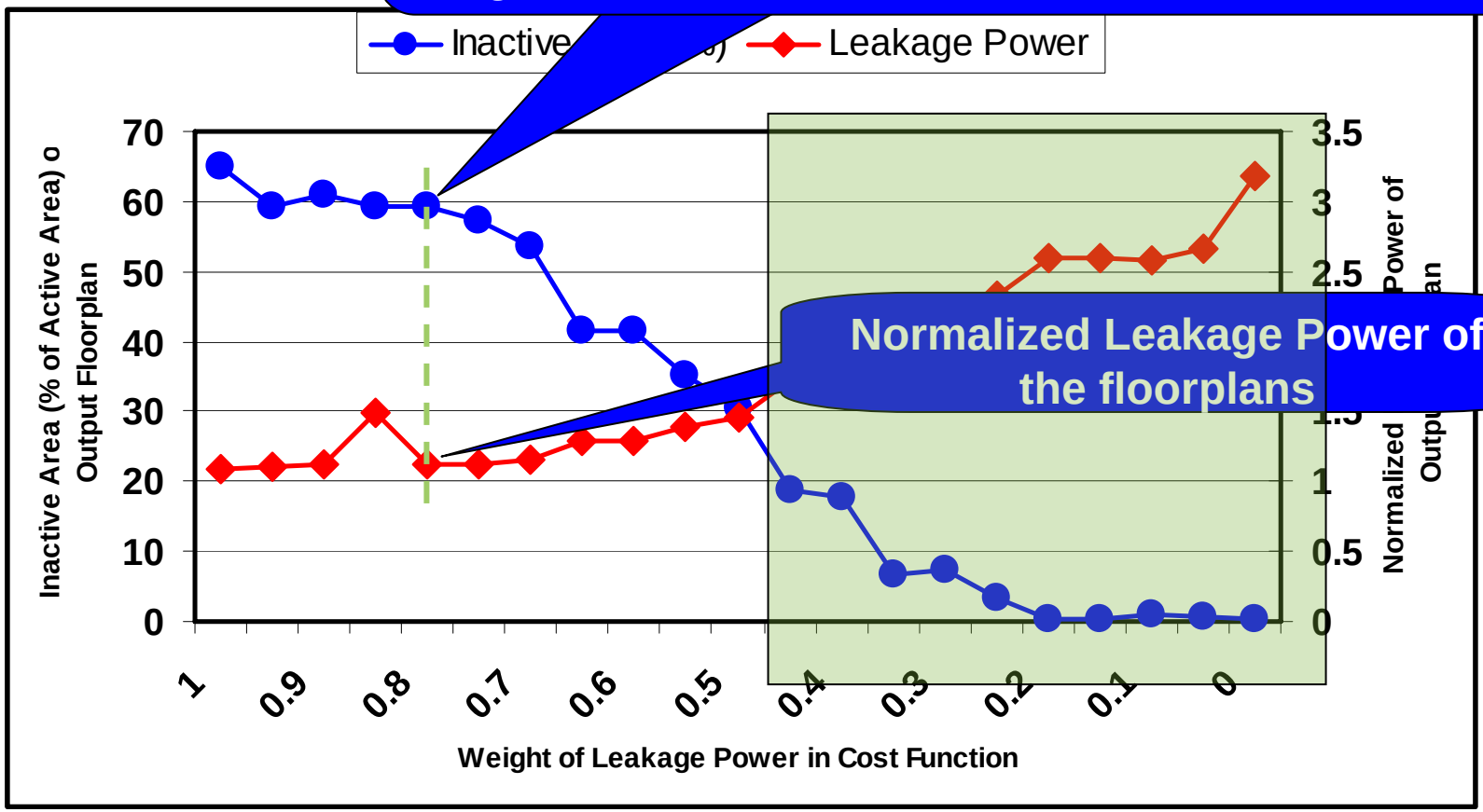
Leakage Estimation with STEFAL



Leakage Aware Floorplanning



- Leakage power variation: 190%!
- Even floorplans with 20% Inactive Area show a variation of 84% !
- All the floorplans shown in the results meet wire length constraints.



Effect of the Positive Feedback Loop

- Run STEFAL on a floorplan and report leakage power numbers for each iteration.

Iteration Number of STEFAL	Output Leakage Power
1	X
2	X + 19.8%
3	X + 24.9%
4	X + 26.3%
5	X + 26.7%
6	X + 26.9%
7	**X + 26.9%**

- Emphasizes the importance of considering the positive feedback loop to reach steady state temperatures.

Conclusion

- Temperature sensitivity of leakage power cannot be ignored.
- Thermal diffusion has very significant impact on the block temperatures.
- Different floorplans have different temperature profiles → different floorplans have different leakage power
- SoC floorplans need to be optimized for leakage power.
- Design cost of leakage aware floorplanning is minimal.
- Leakage aware floorplanning has only 4% runtime overhead compared to traditional floorplanning.