3B-4
Power and Memory Bandwidth Reduction of an H.264/AVC HDTV Decoder LSI with Elastic Pipeline Architecture

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Outline

- Background
- Required cycles in H.264 video decoding
- Elastic pipeline
- Simulation result
- Summary

Research background

Portable media player

Cell phone

Video recorder

Video camera

Video player

H.264 is

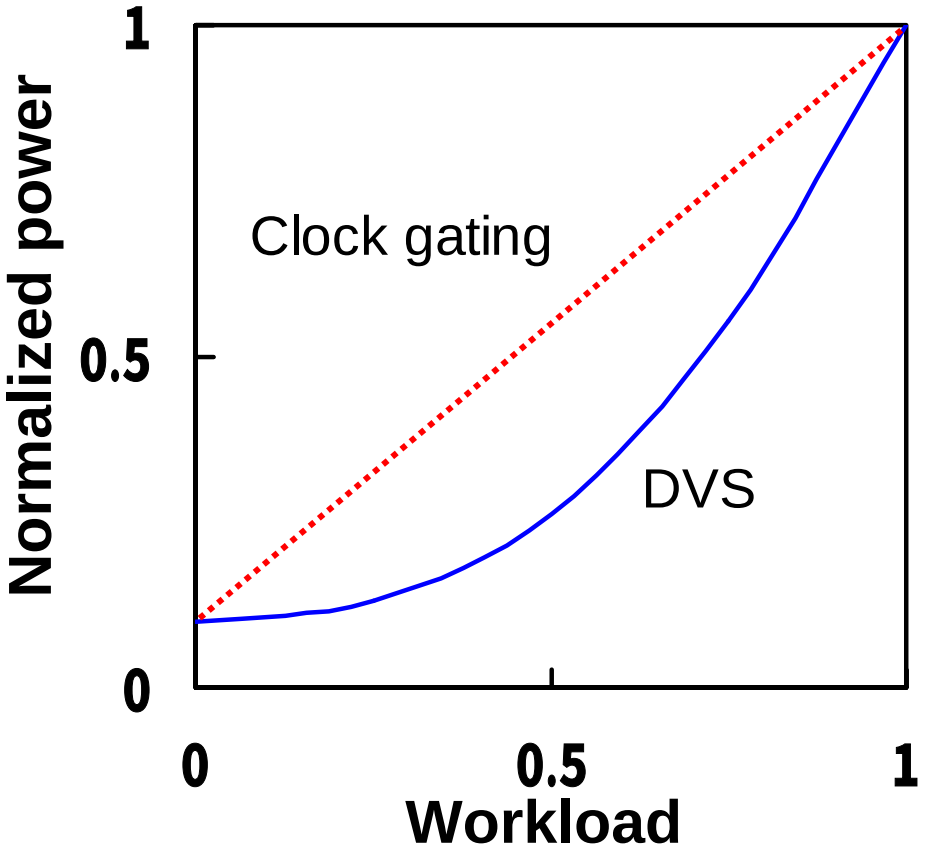
- **newest video coding standard,**
- **twice as effective as MPEG2,**
- **adopted in various services and products.**

But H.264 is

- **several times power consuming.**

Low power H.264 video decoder LSI is required.

DVS (Dynamic Voltage Scaling)



f_{max}: a maximum operating frequency
V_{dd}: supply voltage
k: constants
α: velocity saturation index
V_{th}: threshold voltage
a: activation ratio
C: total capacitance
I_0: leak current at $V_{gs}=V_{th}$
S: subthreshold slope
f: operating frequency

$$f_{max} = \frac{(V_{dd} - V_{th})^{\alpha}}{kV_{dd}}$$

$$P = a \cdot C \cdot f \cdot V_{dd}^{2} + V_{dd} \cdot I_0 \cdot 10^{\frac{V_{gs} - V_{th}}{S}}$$

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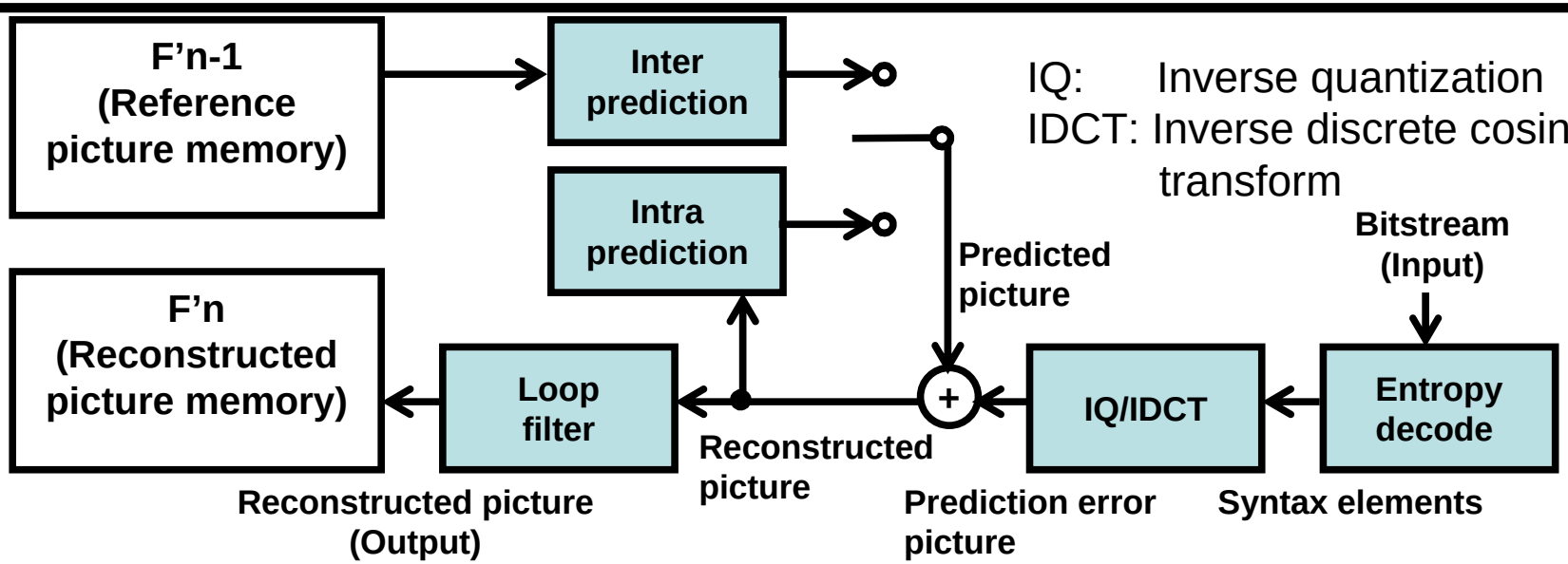
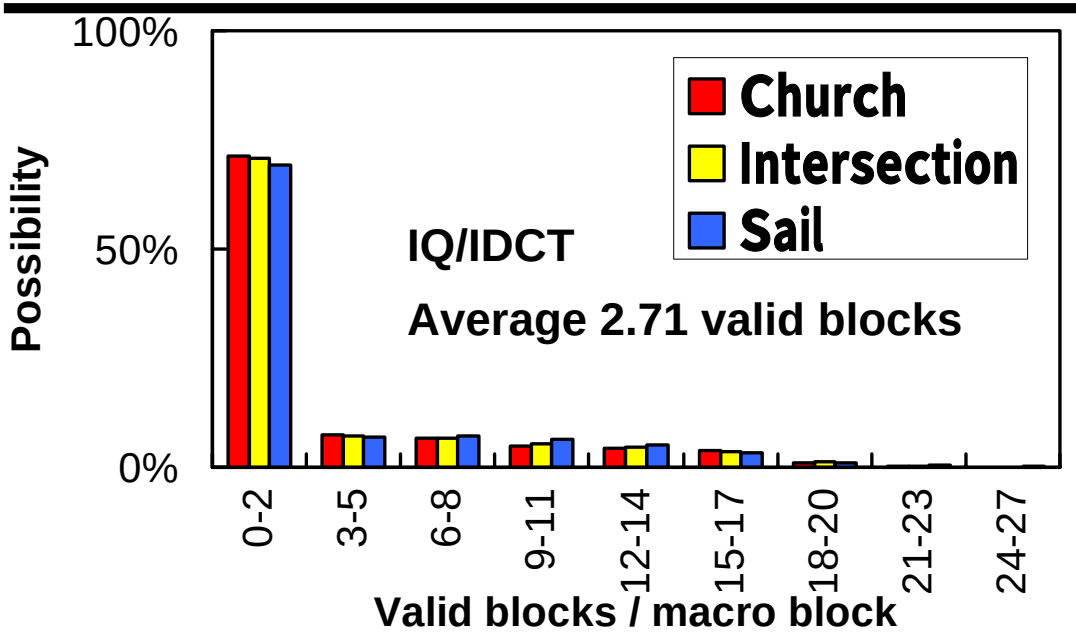
Cycle variation in H.264 decoding

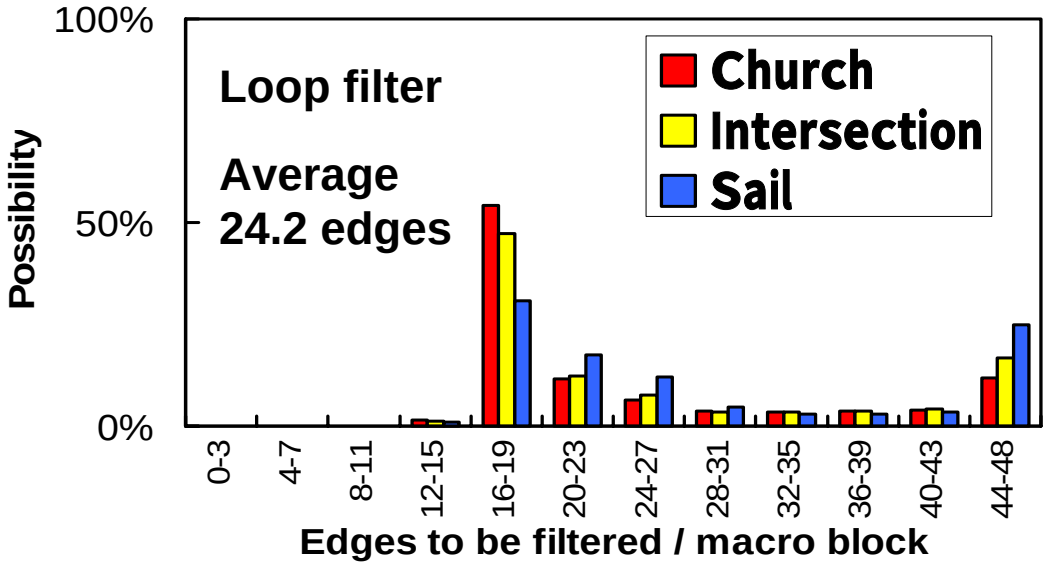


Process	Content of processing	Factor of variation of required comp. power
Entropy decode	Transforms an input bit stream to syntax elements	# of syntax elements
IQ/IDCT	Matrix operation	# of valid blocks
Intra prediction	Numerical calculation	Intra prediction mode
Inter prediction	FIR filter	# of motion vectors, precision of motion vectors
Loop filter	FIR filter	Intra/Inter mode, MB partition mode, pixel value

Computation power required for H.264 decoding is fluctuate.

Required cycles in an macro block





Simulation conditions

Frame rate	30frames/s
Resolution	1920×1024
Bitrate	10Mbits/s
# of Reference picture	2
Motion estimation algorithm	UMHexagon search
Search range	±64 x ±64
Entropy decoder	CABAC

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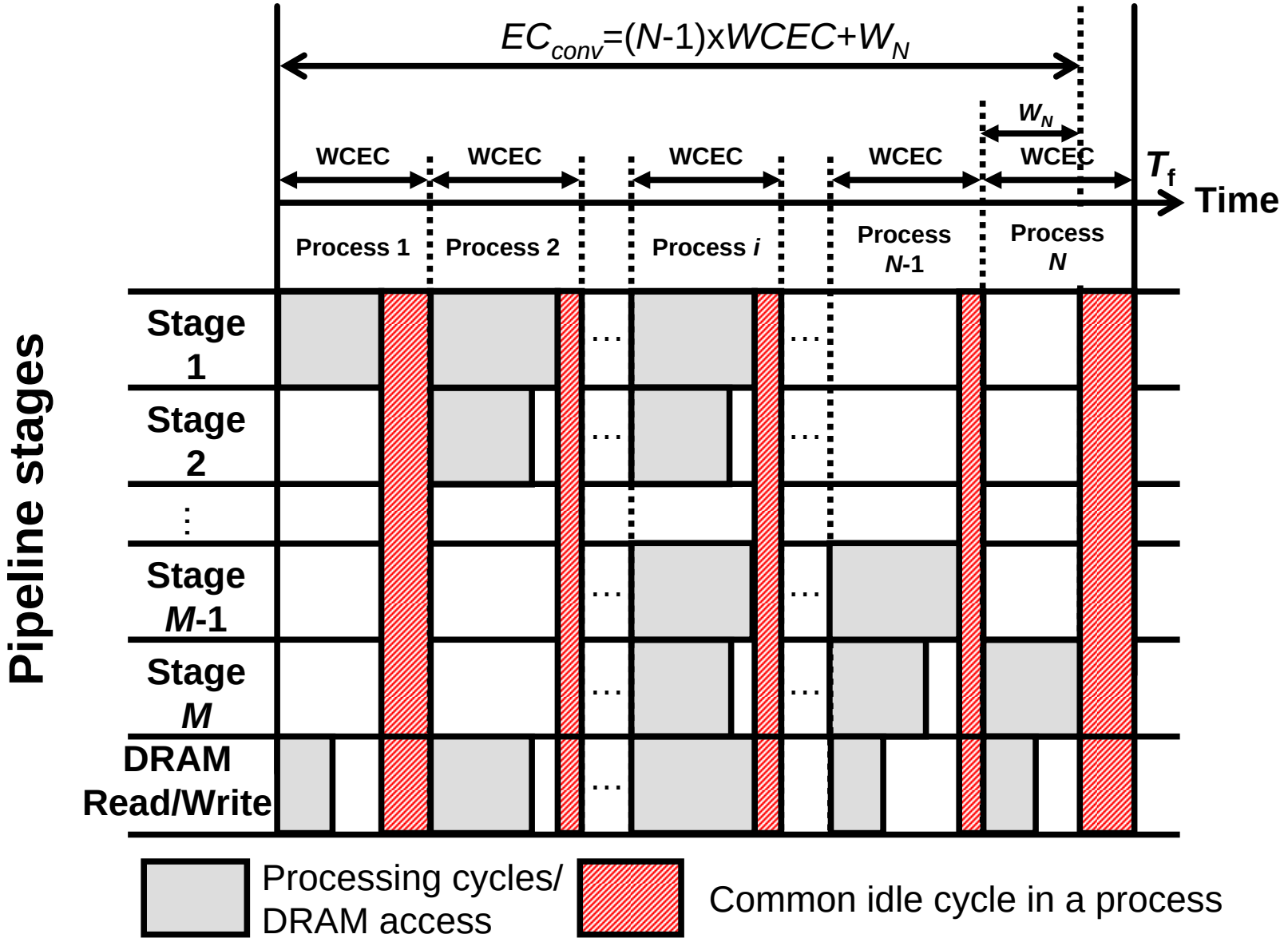
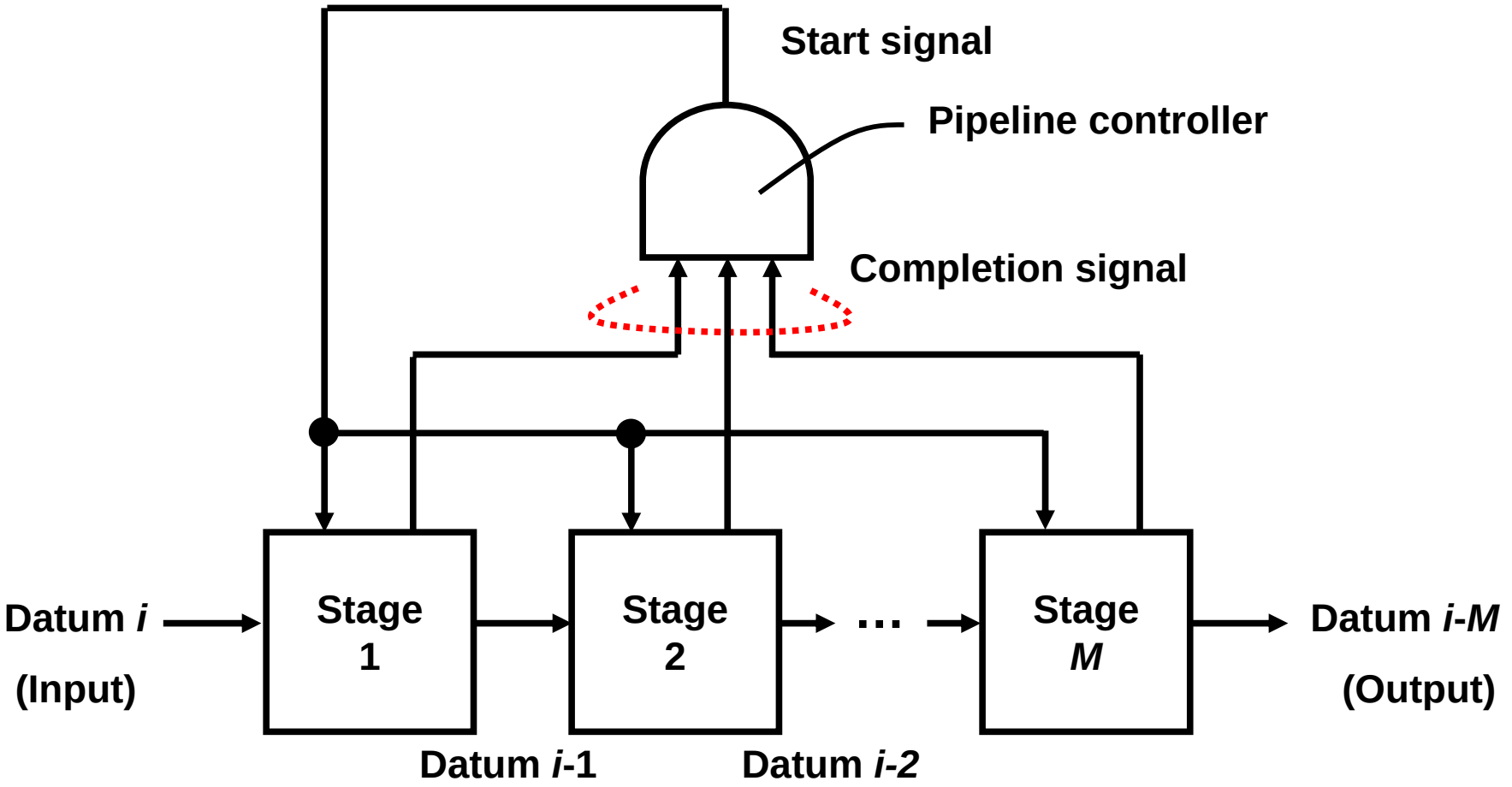
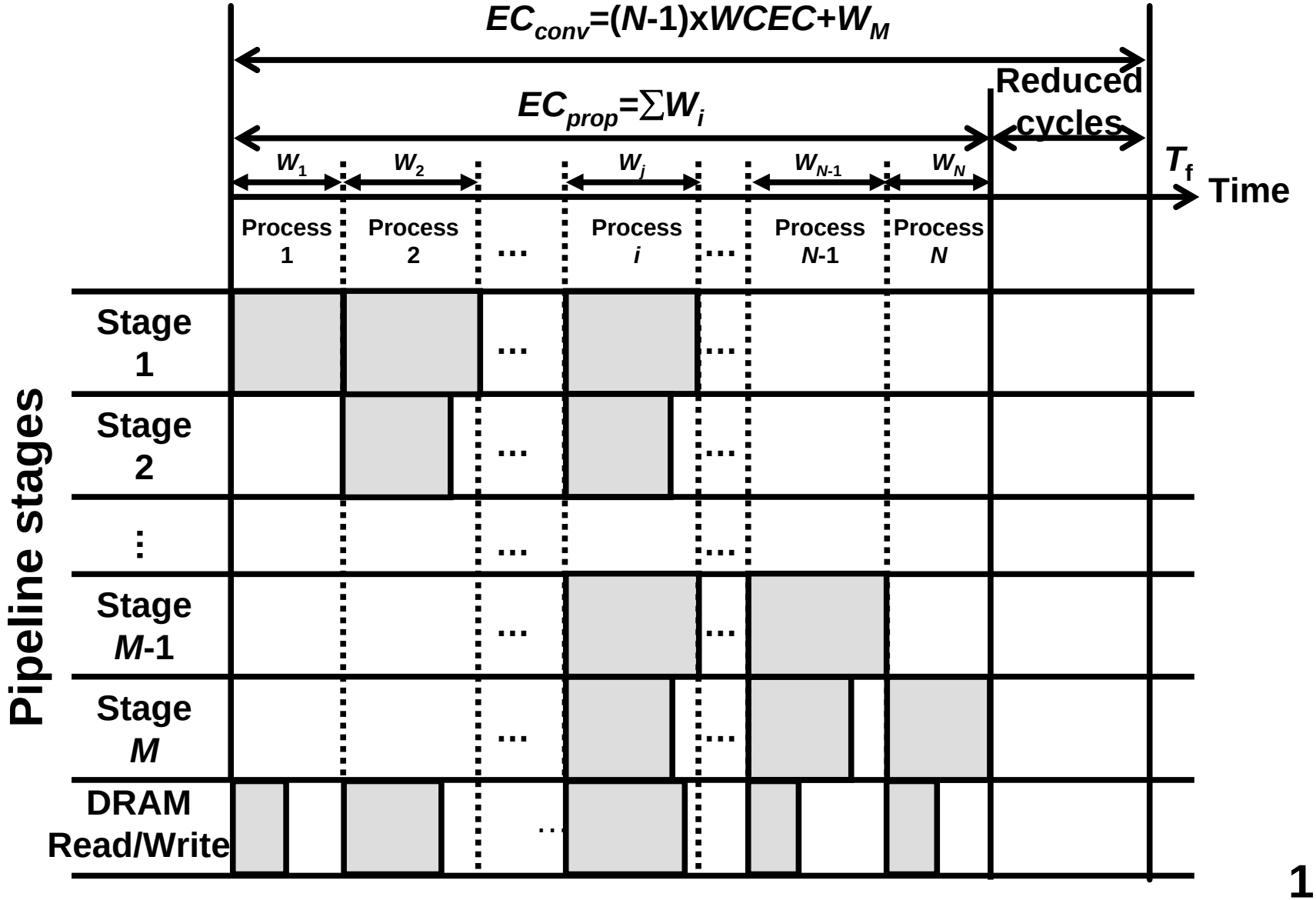
Conventional pipeline



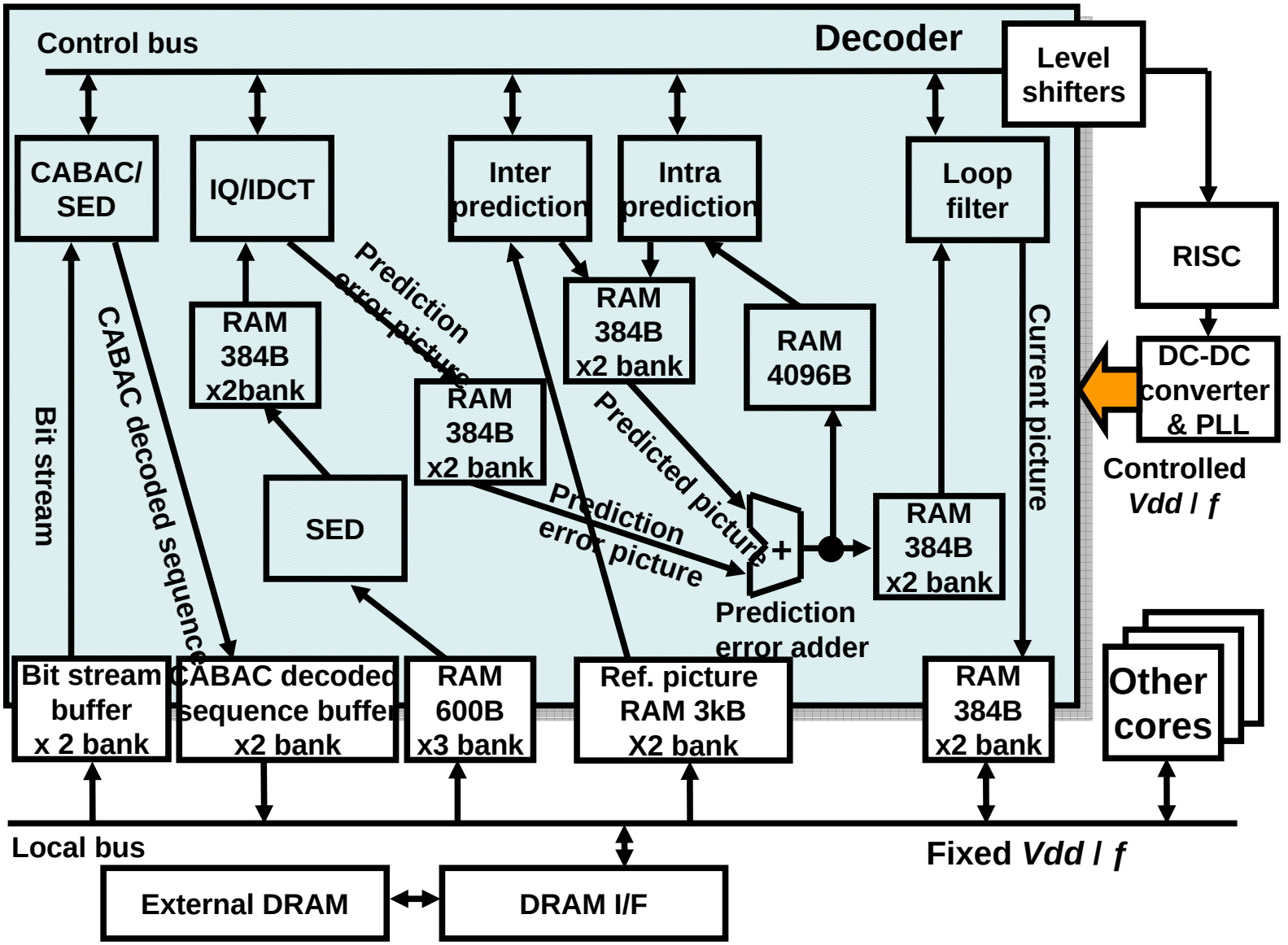
Elastic pipeline (1/2)



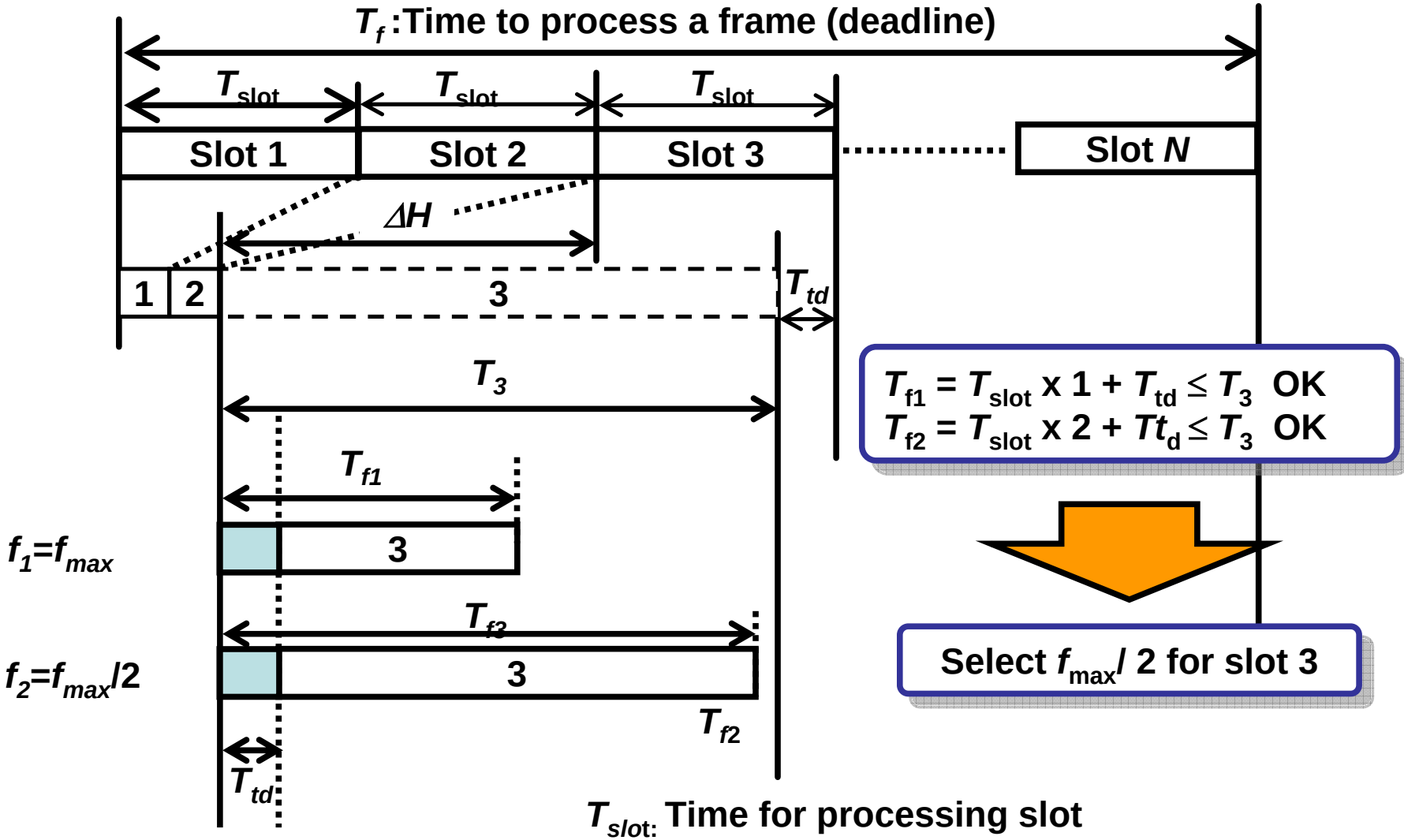
Elastic pipeline (2/2)



Block diagram of H.264 decoder core in a SoC



DVS algorithm



T_{slot}: Time for processing slot

T_{td}: Time for voltage/frequency transition

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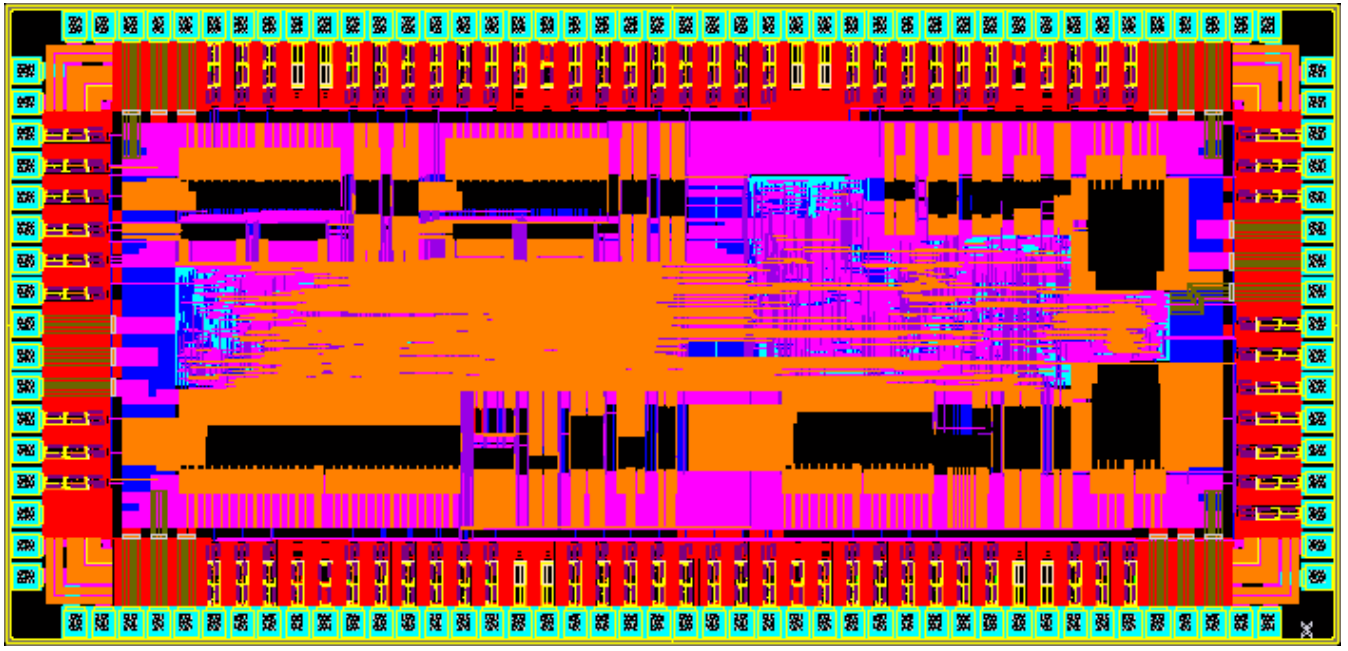
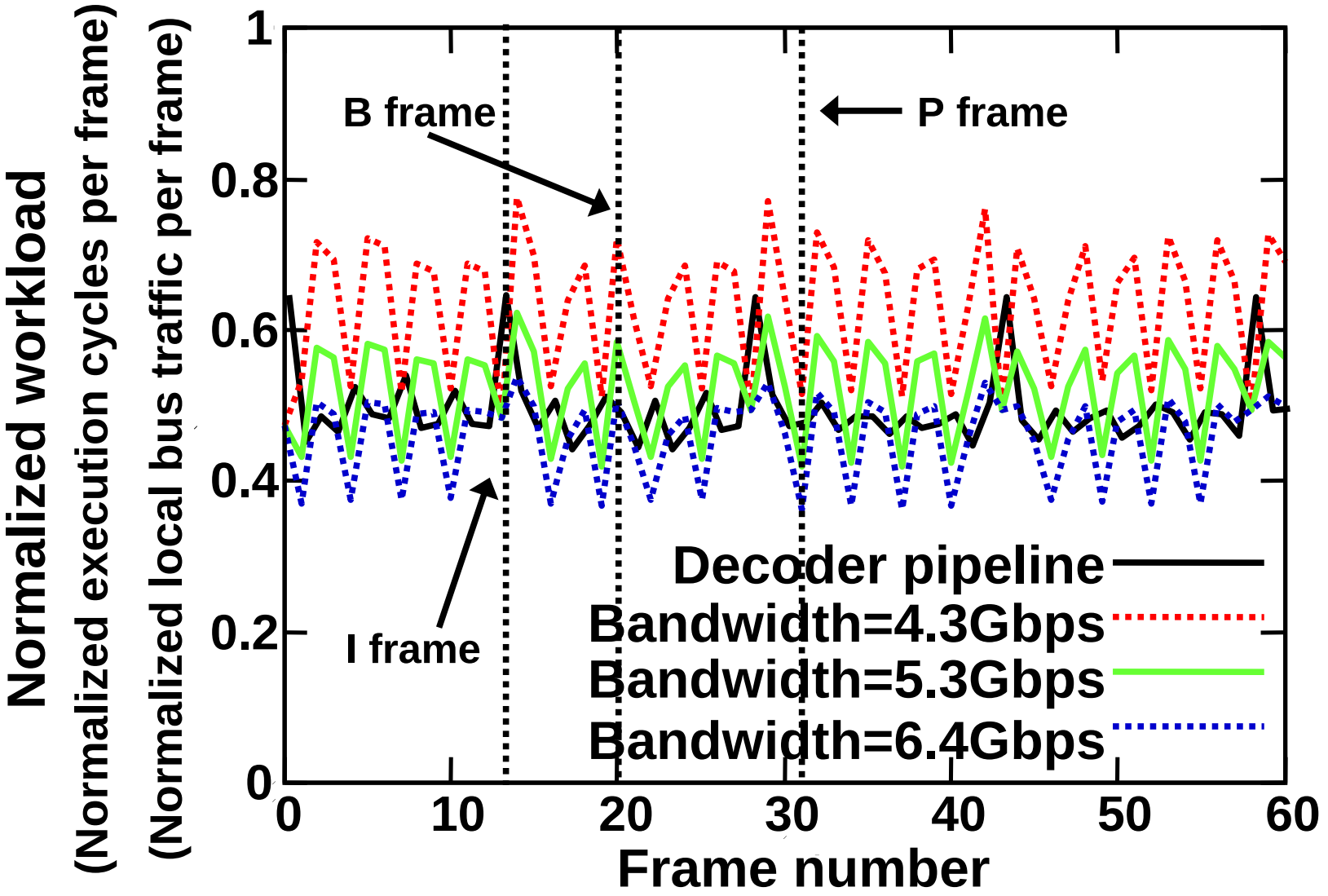
Design for H.264 decoder core



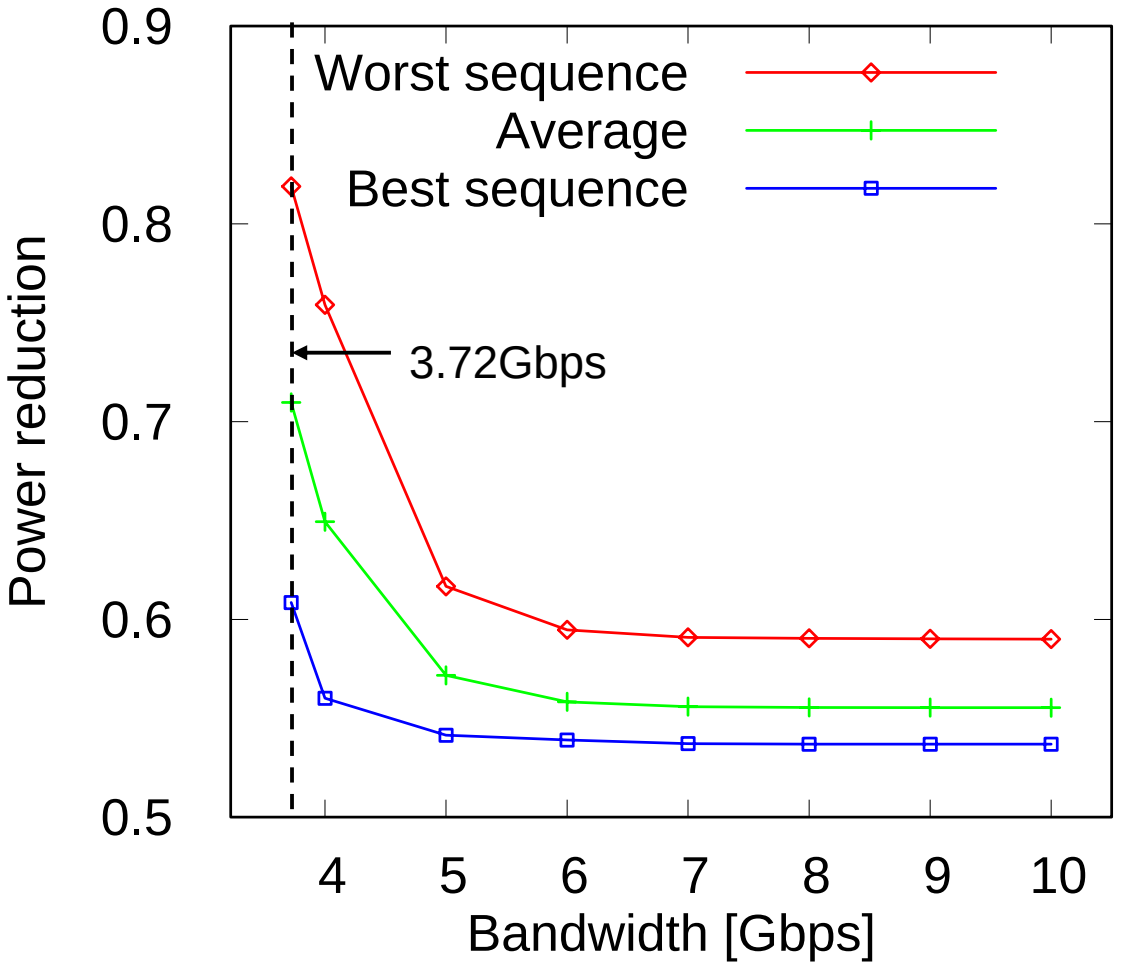
Process technology:	90nm 6-metal
Core area:	1.4x4.0mm
Gate count:	60k
# of transistors:	2.5M
Supply voltage:	1.0V
Operating frequency:	108MHz
Function:	H.264 Main Profile Level 4 w/o CAVLC, weighted prediction and field MB

Cycle reduction



Power reduction

Result of 148 frames × 6 video sequences



- Elastic pipeline can reduce the bandwidth to 3.72Gbps, while the conventional pipeline requires 9.76Gbps.
- Power reduction is saturated over 6.4Gbps.

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- Elastic pipeline for DVS
- Applicable to hard-wired logic
- Bandwidth reduction from 9.62Gbps to 3.72Gbps or 44% power reduction of H.264 HDTV video decoder core

Acknowledgment

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