

Synthesis of Reversible Sequential Elements

Speaker : *Kuang-Jung Chang*

Author : *Min-Lun Chuang*

Chun-Yao Wang

Dept. of Computer Science
National Tsing Hua University, Taiwan

Outline

- Introduction
- Background
- Previous work
- Novel reversible sequential elements
- Results
- Conclusions

Motivations

- Reversible circuits have applications in low power design
 - Landauer Principle $E = k T \ln 2$
 - Moore's Law
- Nanotechnology, low power CMOS, optical computing, quantum computer
 - Every future technology have to use reversible gates in order to reduce power consumption
- Reversible logic synthesis on combinational logic
- This work presents reversible flip-flops and latches used in designing reversible sequential circuits

Outline

- Introduction
- Background
- Previous work
- Novel reversible sequential elements
- Results
- Conclusions

Reversible Computing

- If we know the output, we can derive the input of the function. This kind of computation is called “reversible”

if $C=0 \rightarrow A=?, B=?$



The AND Gate

- $f:(x_1, x_2, \dots, x_n) \rightarrow (y_1, y_2, \dots, y_m)$ is called reversible
iff: f is a bijection function
- A bijection function means the function is 1-1 and onto

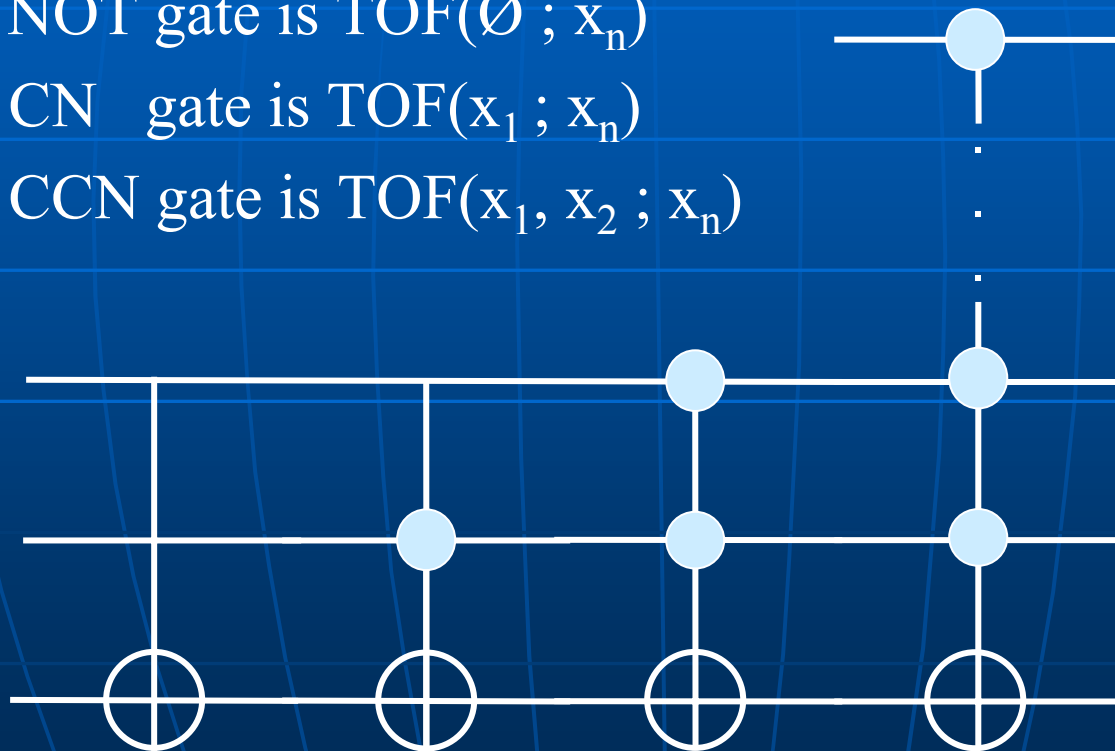
Generalized Toffoli Gate

- $\text{TOF}(C;t)$, where C is the set of control variable, $\{x_1, x_2, x_3, \dots\}$, t is the set of target variable $\{x_n\}$ and $C \cap t = \{\emptyset\}$

ex: NOT gate is $\text{TOF}(\emptyset ; x_n)$

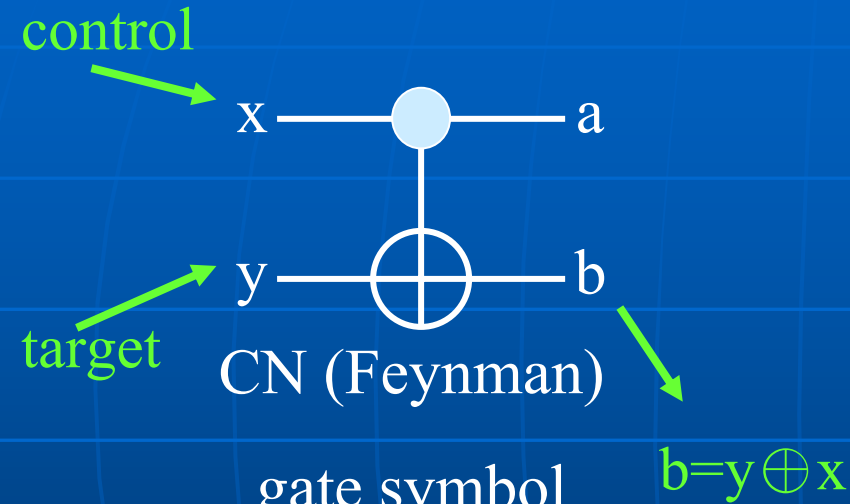
CN gate is $\text{TOF}(x_1 ; x_n)$

CCN gate is $\text{TOF}(x_1, x_2 ; x_n)$



The CN Gate & CCN gate

■ Controlled NOT

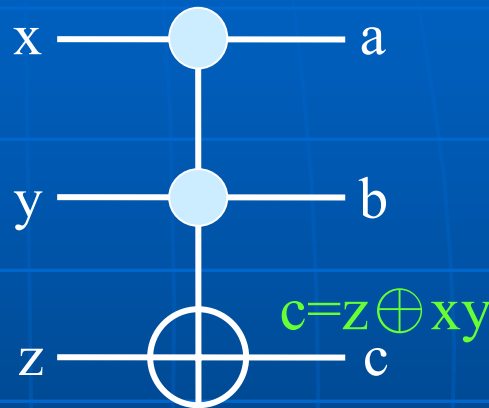


gate symbol

x	y	a	b
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Truth Table for the CN Gate

■ Controlled Controlled NOT gate



CCN (Toffoli)

gate symbol

x	y	z	a	b	c
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Truth Table for the CCN Gate

Irreversible Function Implementation

x	y	xy
0	0	0
0	1	0
1	0	0
1	1	1

$$f(x,y)=xy$$



x	y	z	x	y	$xy \oplus z$
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

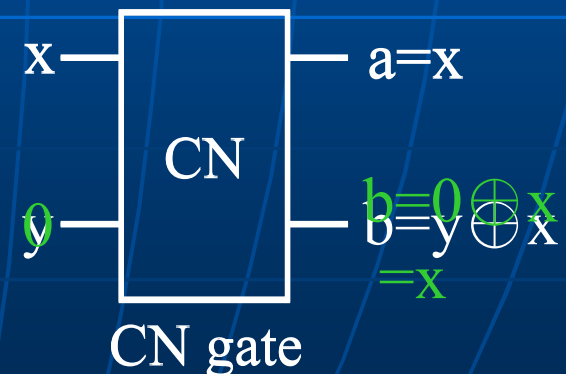
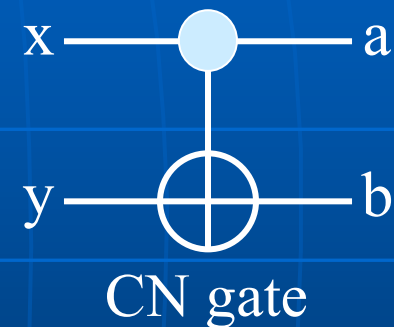
$$f(x,y,z)=xy \oplus z$$

Garbage

Garbage is the outputs added to make an n -input m -output function reversible.

Restriction

- Fanout count of a signal net must equal one
 - Fanout structure is not reversible
 - If two copies of one signal are needed, a duplication is necessary



Reversible Circuits Synthesis Objective

- Minimize the number of gates
 - Gate count gives a simple estimate of the implementation cost of the reversible circuit
- Minimize the number of garbage outputs
 - Minimizing the number of garbage outputs leads to minimizing area and power

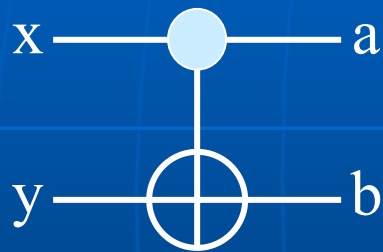
Outline

- Introduction
- Background
- Previous work
 - A Beginning in the Reversible Logic Synthesis of Sequential Circuits [17]
- Novel reversible sequential elements
- Results
- Conclusions

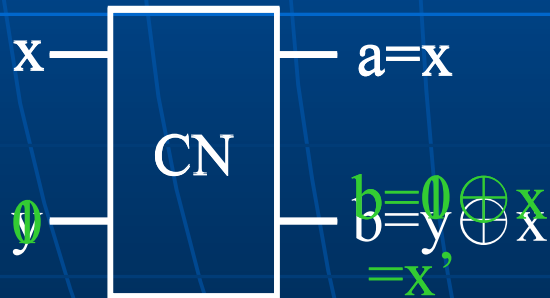
Basic Gate

■ Controlled NOT gate

NOT & fanout



CN gate symbol

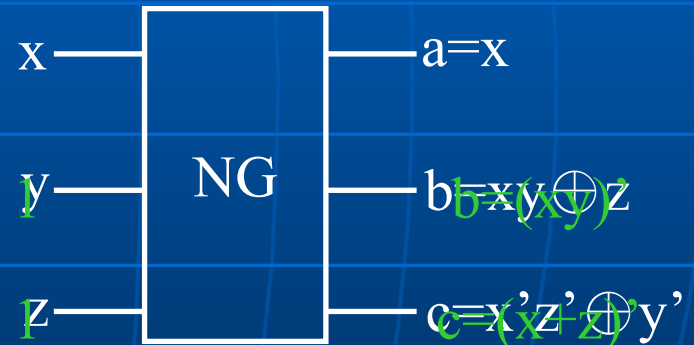


CN gate

■ New gate (NG)

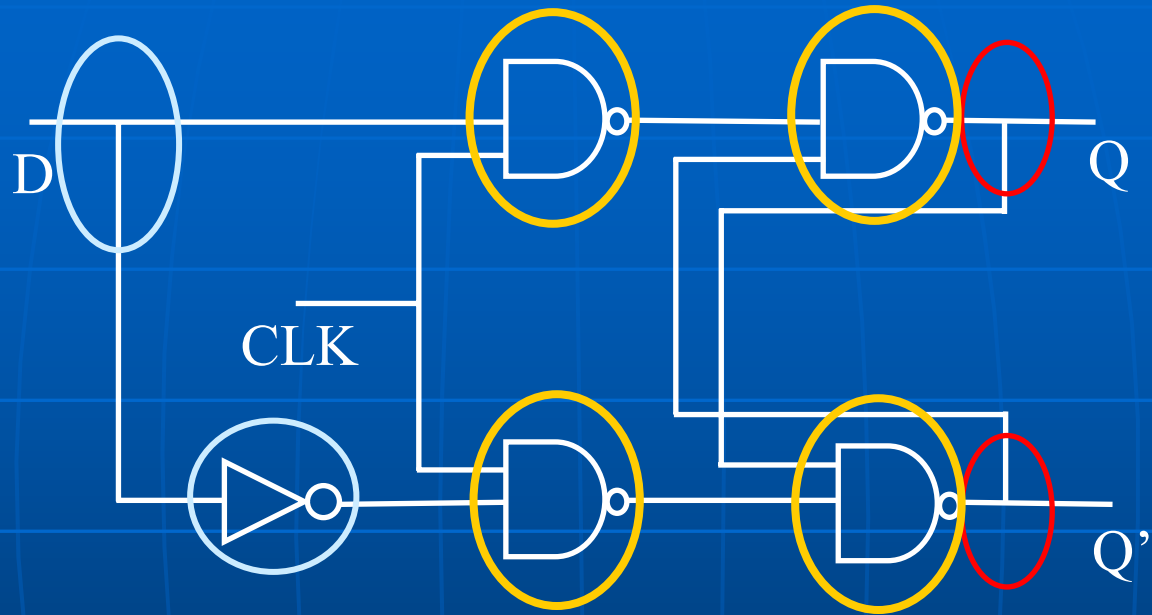
- more complex and powerful

NAND & NOR



New gate symbol

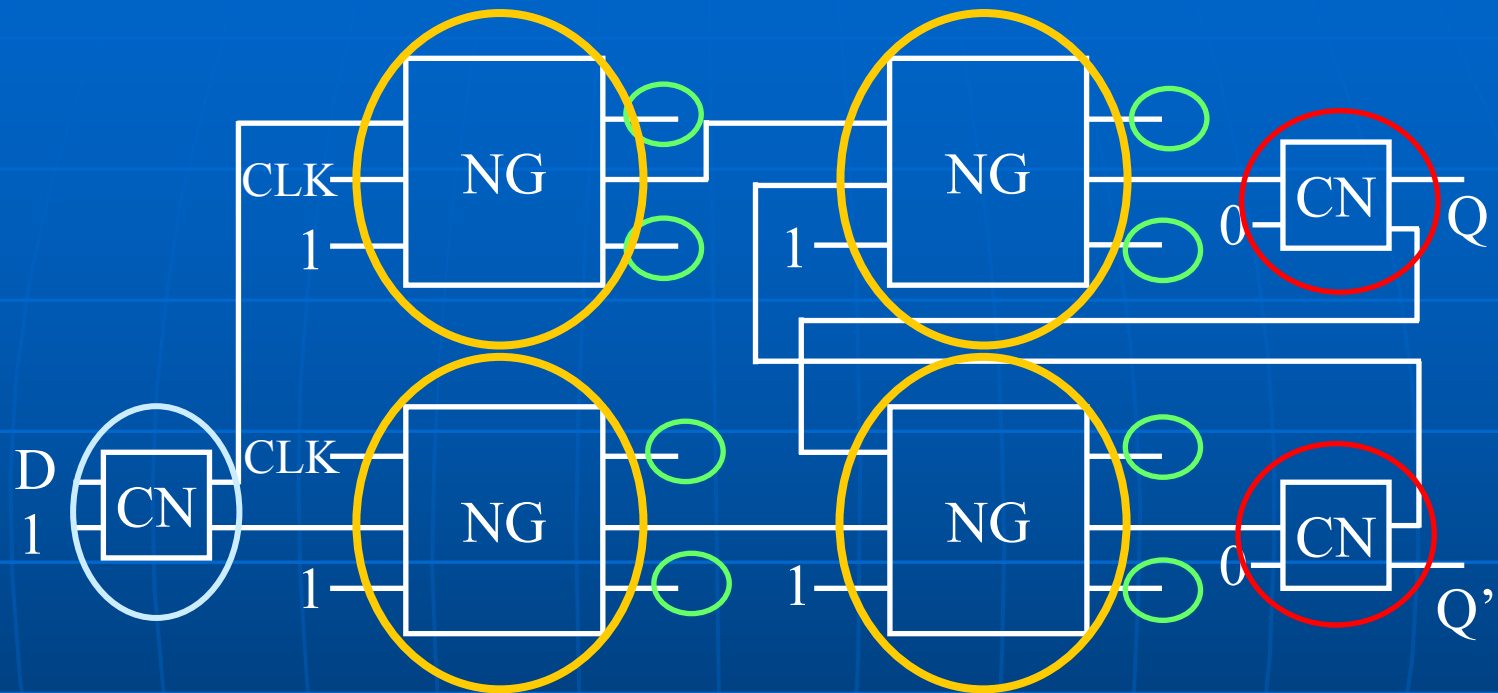
D Latch



CLK	D	Q_{n+1}
0	0	Q_n
0	1	Q_n
1	0	0
1	1	1

D latch truth table

Reversible D Latch



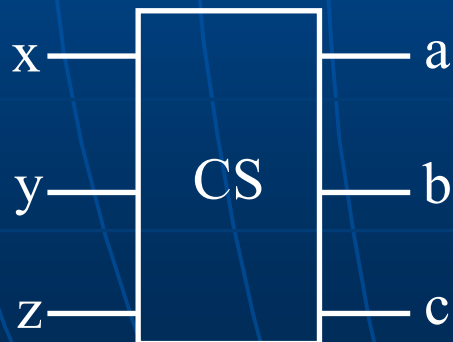
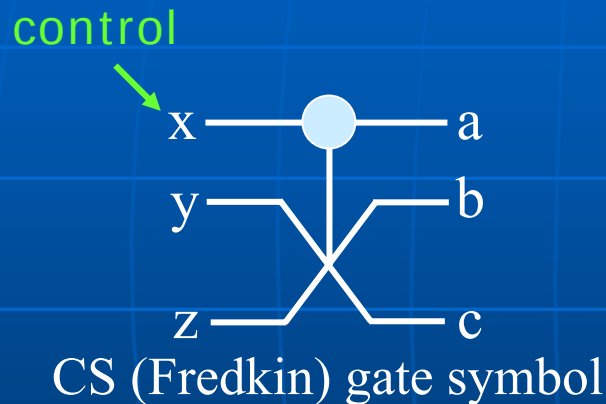
	Garbage outputs	Gate counts
[17]	8	7

Outline

- Introduction
- Background
- Previous work
 - A New Look at Reversible Memory Elements [15]
- Novel reversible sequential elements
- Results
- Conclusions

Basic Gate

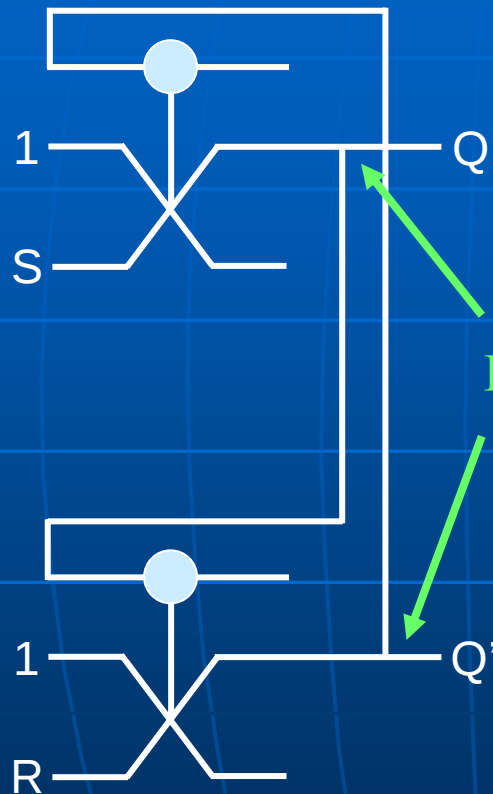
- Controlled Swap gate (CS): Controlled Swap gate is also called Fredkin gate



x	y	z	a	b	c
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

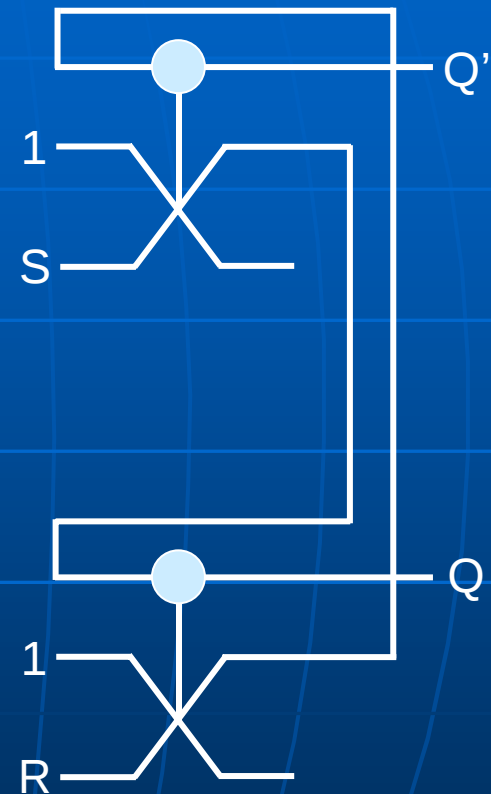
Truth Table for the CS gate

Reversible RS Latch



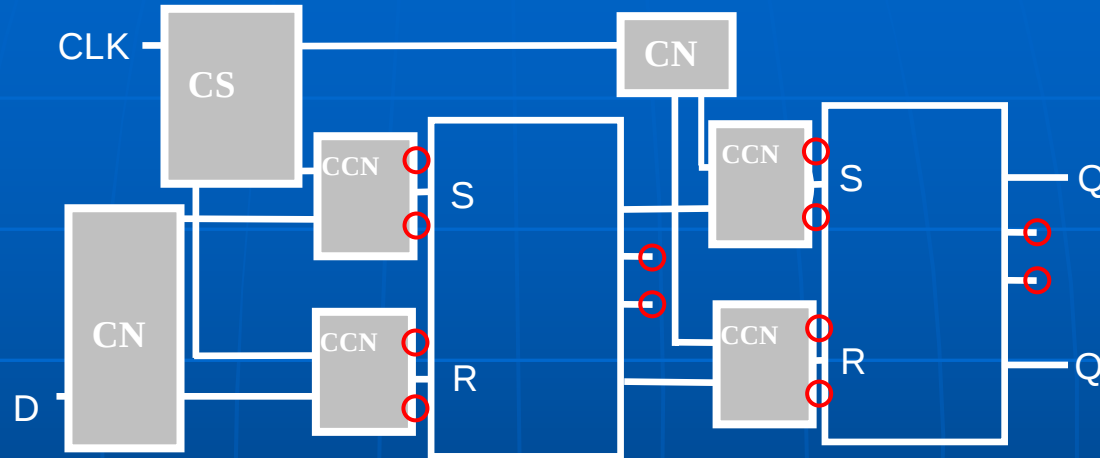
The reversible RS latch
proposed by Picton

Figure



The reversible RS latch
proposed by Rice [15]

D Flip-Flop



D flip-flop	Garbage outputs	Gate counts
[15]	12	11

Outline

- Introduction
- Background
- Previous work
- Novel reversible sequential elements
- Results
- Conclusions

Truth Table Extension Synthesis Method

- Add garbage outputs to make the truth table reversible

CLK	J	K	Q_{n+1}
0	0	0	Q_n
0	0	1	Q_n
0	1	0	Q_n
0	1	1	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Q_n'

JK latch truth table

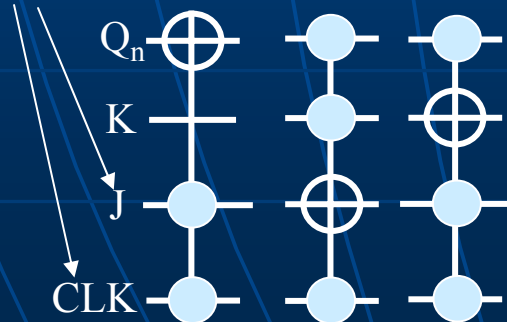


extend

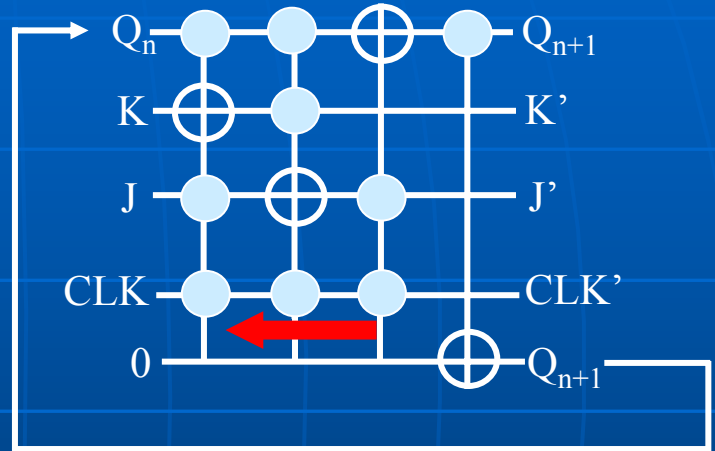
CLK	CLK	K	Q_n	Q_n'	Q_{n+1}'	K'	Q_{n+1}
0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	1
0	0	1	0	0	0	1	0
0	0	1	1	1	1	1	1
0	1	0	0	0	0	0	0
0	1	0	1	1	0	0	1
0	1	1	0	0	1	1	0
0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	1	1	1	1	0
1	1	0	0	0	0	0	1
1	1	0	1	1	1	0	1
1	1	1	0	0	1	1	1
1	1	1	1	1	1	0	0

Synthesis Procedure [9]

in	out	S1	S2	S3
0000	0000	0000	0000	0000
0001	0001	0001	0001	0001
0010	0010	0010	0010	0010
0011	0011	0011	0011	0011
0100	0100	0100	0100	0100
0101	0101	0101	0101	0101
0110	0110	0110	0110	0110
0111	0111	0111	0111	0111
1000	1000	1000	1000	1000
1001	1001	1001	1001	1001
1010	1010	1010	1010	1010
1011	1110	1111	1011	1011
1100	1101	1100	1100	1100
1101	1011	1011	1111	1101
1110	1111	1110	1110	1110
1111	1100	1101	1101	1111



D. M. Miller , “A transformation based algorithm for reversible logic synthesis,”
DAC 2003



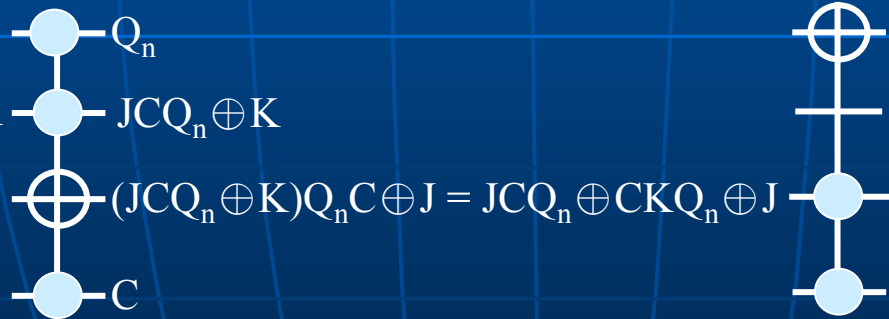
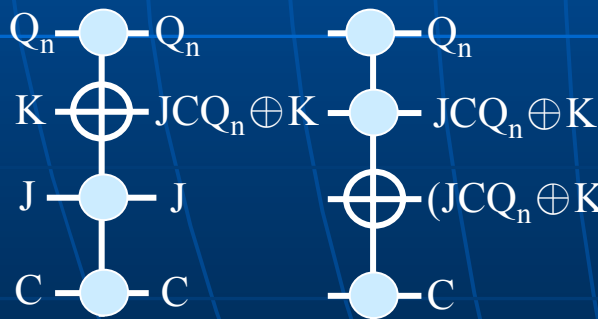
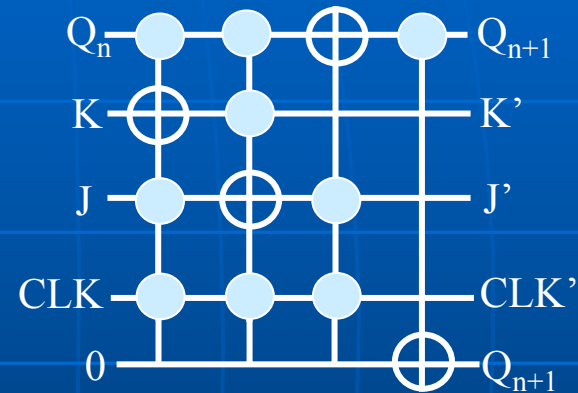
	Garbage outputs	Gate counts
Our design	3	4
Existing one	12	10

Function Verification

Obtained by JK latch truth table

$$C' = C$$

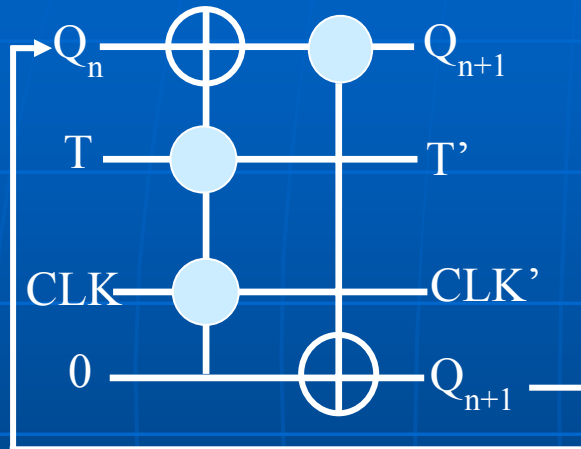
$$Q_{n+1} = JC \oplus Q_n \oplus Q_n CK \oplus Q_n CJ$$



$$\begin{aligned} Q_{n+1} &= (JCQ_n \oplus CKQ_n \oplus J)C \oplus Q_n \\ &= JC \oplus Q_n \oplus Q_n CK \oplus Q_n CJ \end{aligned}$$

Reversible T Latch & D Latch

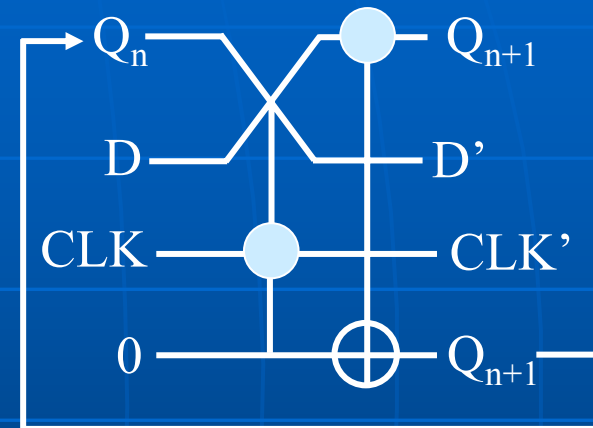
■ T Latch



Evaluation of T latch

	Garbage outputs	Gate counts
Our design	2	2
Existing one	12	10

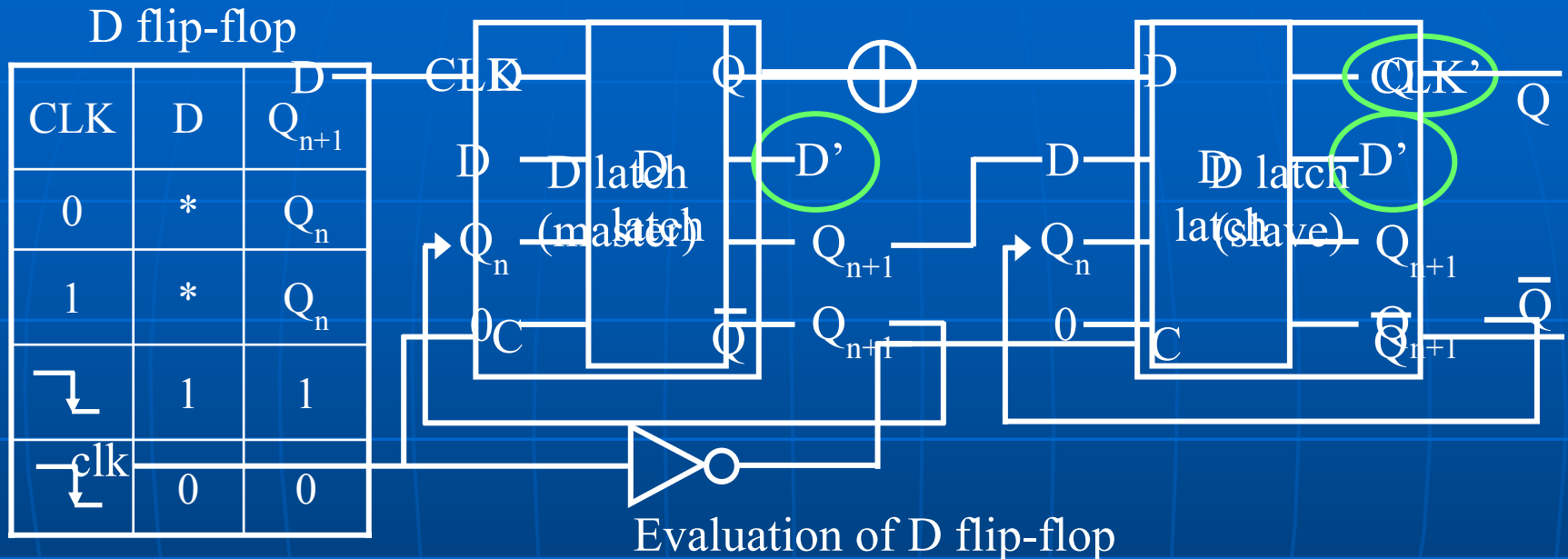
■ D Latch



Evaluation of D latch

	Garbage outputs	Gate counts
Our design	2	2
Existing one	8	7

Reversible D Flip-Flop

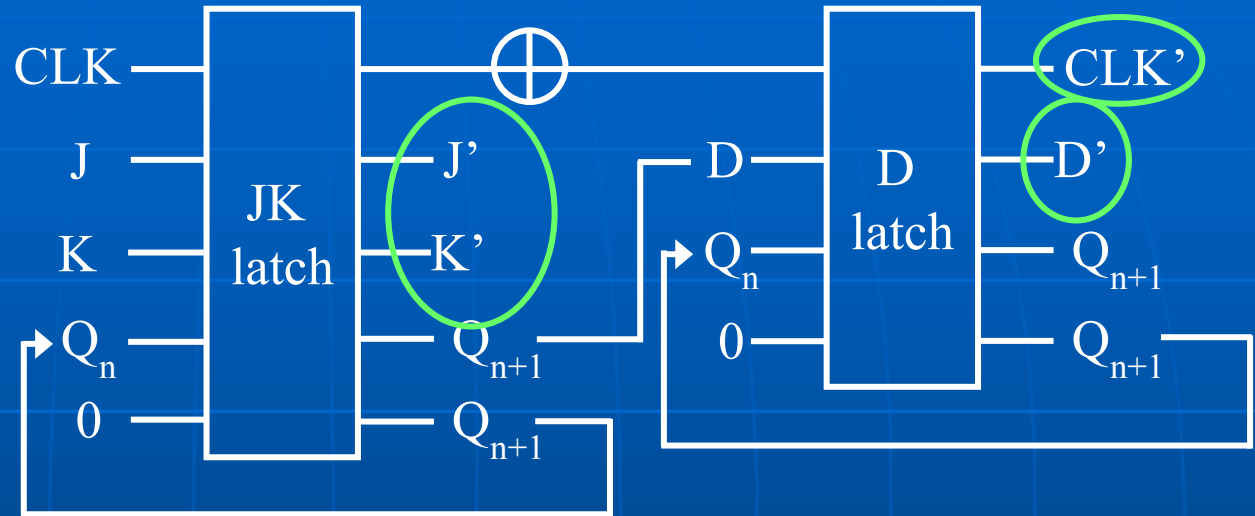


	Garbage bits	Gate counts
Our design	3	5
Existing one	12	11

Reversible JK Flip-Flop

JK flip-flop

CLK	J	K	Q_{n+1}
0	*	*	Q_n
1	*	*	Q_n
$\downarrow$	0	0	Q_n
$\downarrow$	0	1	0
$\downarrow$	1	0	1
$\downarrow$	1	1	Q_n'



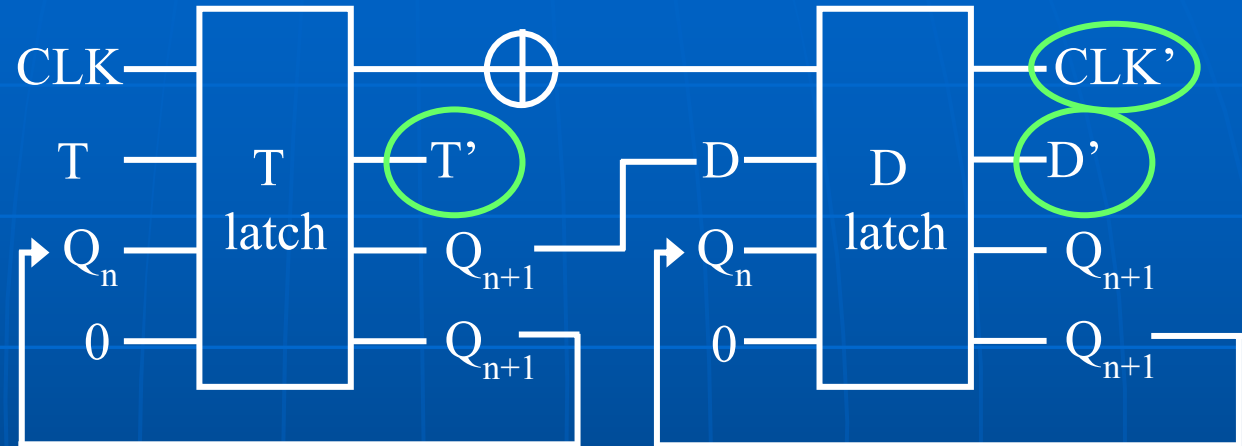
Evaluation of JK flip-flop

	Garbage bits	Gate counts
Our design	4	7
Existing one	21	18

Reversible T Flip-Flop

T flip-flop

CLK	T	Q_{n+1}
0	*	Q_n
1	*	Q_n
	1	Q_n'
	0	Q_n



Evaluation of T flip-flop

	Garbage bits	Gate counts
Our design	3	5
Existing one	14	13

Outline

- Introduction
- Background
- Previous work
- Novel reversible sequential elements
- Results
- Conclusions

Results

	No. of garbage outputs			No. of gates		
	Ours	2005	Ratio(%)	Ours	2005	Ratio(%)
D-latch	2	8	25.0	2	7	28.6
JK-latch	3	12	25.0	4	10	40.0
T-latch	2	12	16.6	2	10	20.0
D flip-flop	3	—	—	5	—	—
JK flip-flop	4	21	19.0	7	18	38.9
T flip_flop	3	—	—	5	—	—
Average	—	—	21.4	—	—	31.9

H. Thapliyal and M. B. Srinivas, “A beginning in the reversible logic synthesis of sequential circuits,” in Proc. of MAPLD, 2005.

Results

	No. of garbage outputs			No. of gates		
	Ours	2006	Ratio(%)	Ours	2006	Ratio(%)
D flip-flop	3	12	25.0	5	11	45.5
JK flip-flop	4	14	28.6	7	12	58.3
T flip_flop	3	14	21.4	5	13	38.5
Average	—	—	25.0	—	—	47.4

Outline

- Introduction
- Background
- Previous work
- Novel reversible sequential elements
- Results
- Conclusions

Conclusions

- We propose novel designs of reversible latches and flip-flops
- The implementation costs of our new designs are more competitive

Thank You