A New Methodology for Interconnect Parasitic Extraction Considering Photo-Lithography Effects

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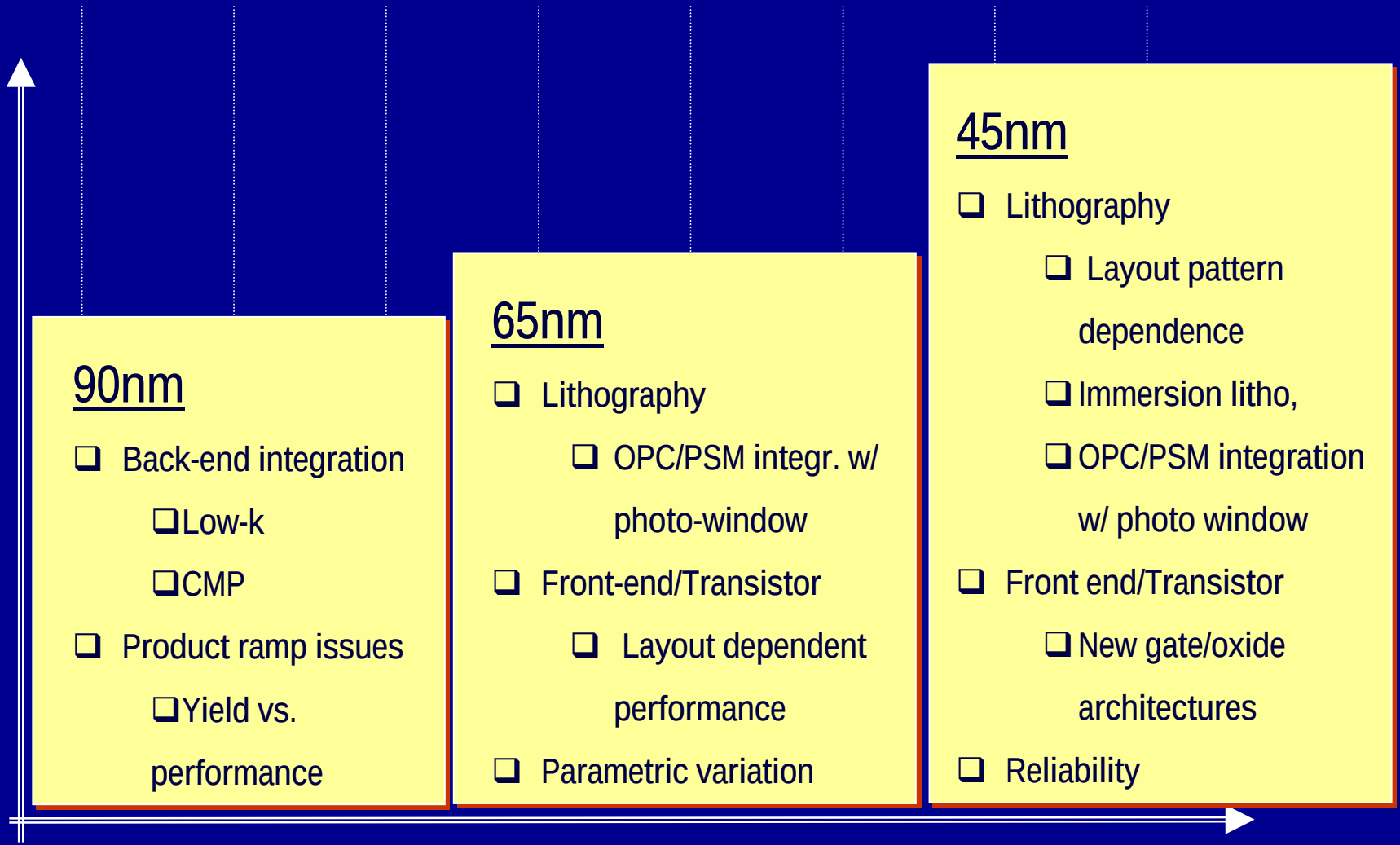
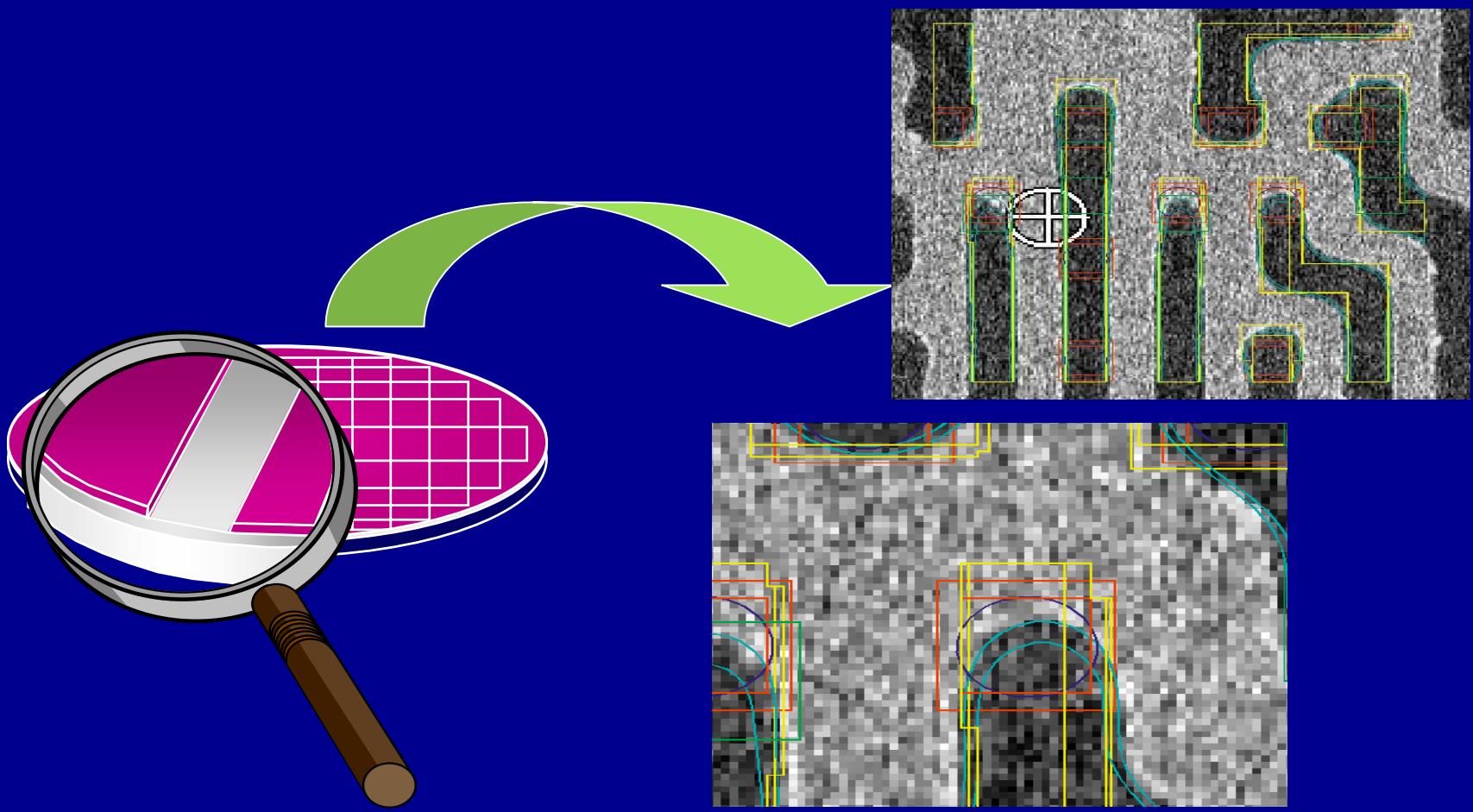
Outline

- **Introduction**
- New Methodology
- Lithography Simulation
- Discretization
- Shape Correction
- Conclusion

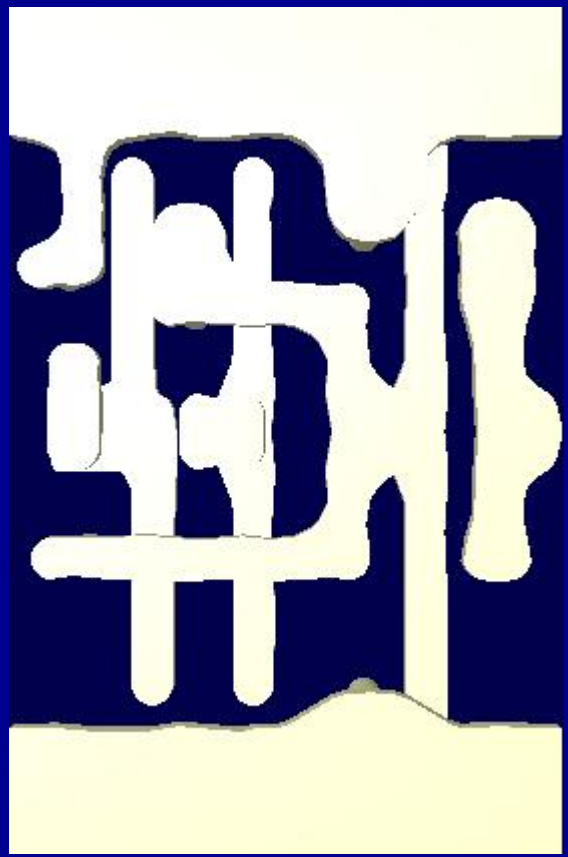
Technology Roadmap Challenges



Layout Geometry vs Fabricated



Typical NAND Gate



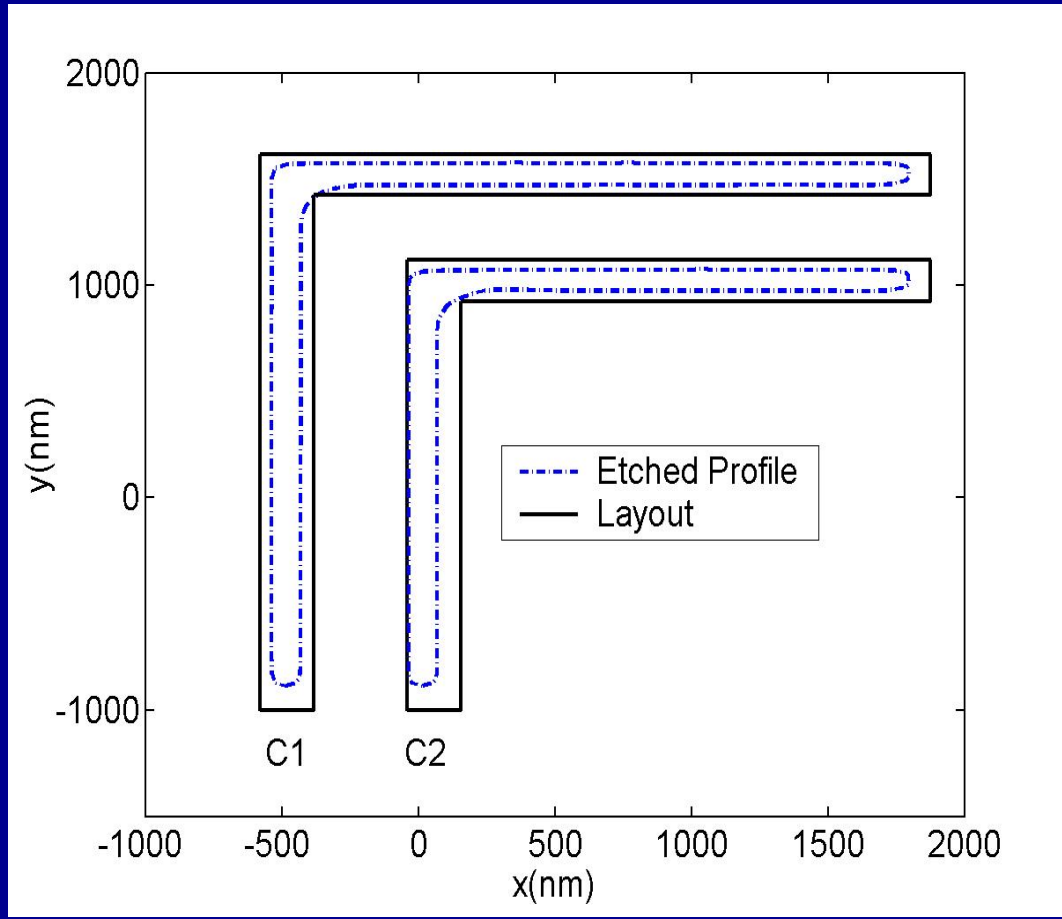
Severe distortion happens not only on ploy, but also on several metal layers

Layout Parasitic Extraction (LPE)

- From layout, extract parasitic Resistance (R), Capacitance (C), and Inductance (L)
- An important step in timing verification and signal integrity analysis
- RCL values depend on detailed geometry, and thus affected by OPC/litho/etch/CMP/…

Example Simple Structure

- Two elbows
- Best OPC added
- Litho/etch simulation performed by PROLITH



Top view

Significant Error in R and C

Capacitance (aF)	OPC / Litho / Etched	Layout	Error if assume layout
C_{11}	110.8	123.9	+11.8 %
C_{22}	93.9	105.9	+12.8 %
C_{12}, C_{21}	57.9	67.7	+16.9 %

Resistance (ohm)	OPC / Litho / Etched	Layout	Error if assume layout
R_{11}	0.288	0.225	–21.8 %
R_{22}	0.230	0.182	–20.8 %

Negligible Error in L

Inductance (pH)	OPC/Litho/ Etched	Layout	Error if assume layout
L_{11}	2.94	3.00	+2.0 %
L_{22}	2.16	2.20	+1.8 %
L_{12}, L_{21}	1.15	1.17	+1.7 %

Observation

- Due to OPC/litho/etch effect, assuming layout geometry in extraction can cause significant error in R and C
- Such large error is sufficient to cause problem in timing verification and signal integrity analysis
- It is time Layout Parasitic Extraction (LPE) tools consider OPC/litho/etch effect

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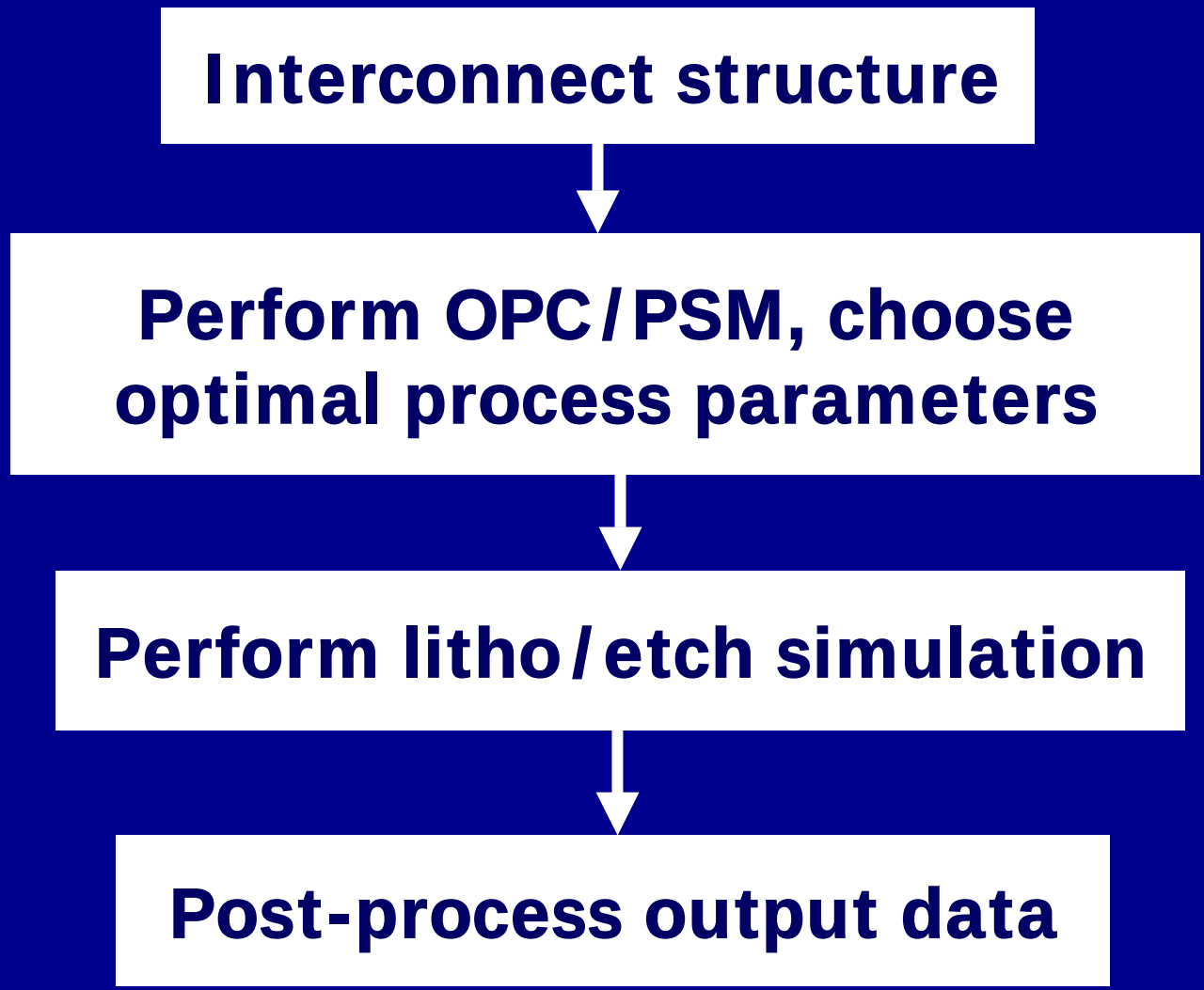
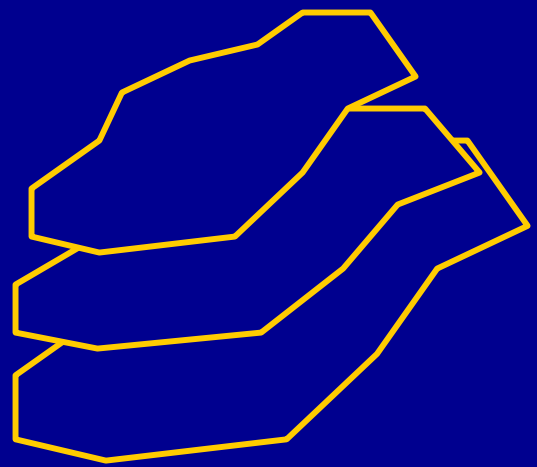
Litho/etch Simulation Flow



Litho Simulation Output

X	Y	Z
100.0	1200.0	0
101.0	1250.0	0
...		
100.5	1195.5	-3
102.0	1220.0	-3
...		
99.0	1120.5	-6
...		

Output specifies contour at different elevation:



Litho Simulation Limitation

- Highly process dependent
- Very slow, even for simple structures
- Multiple runs of full-chip litho/etch simulation impossible
- Large output data volume

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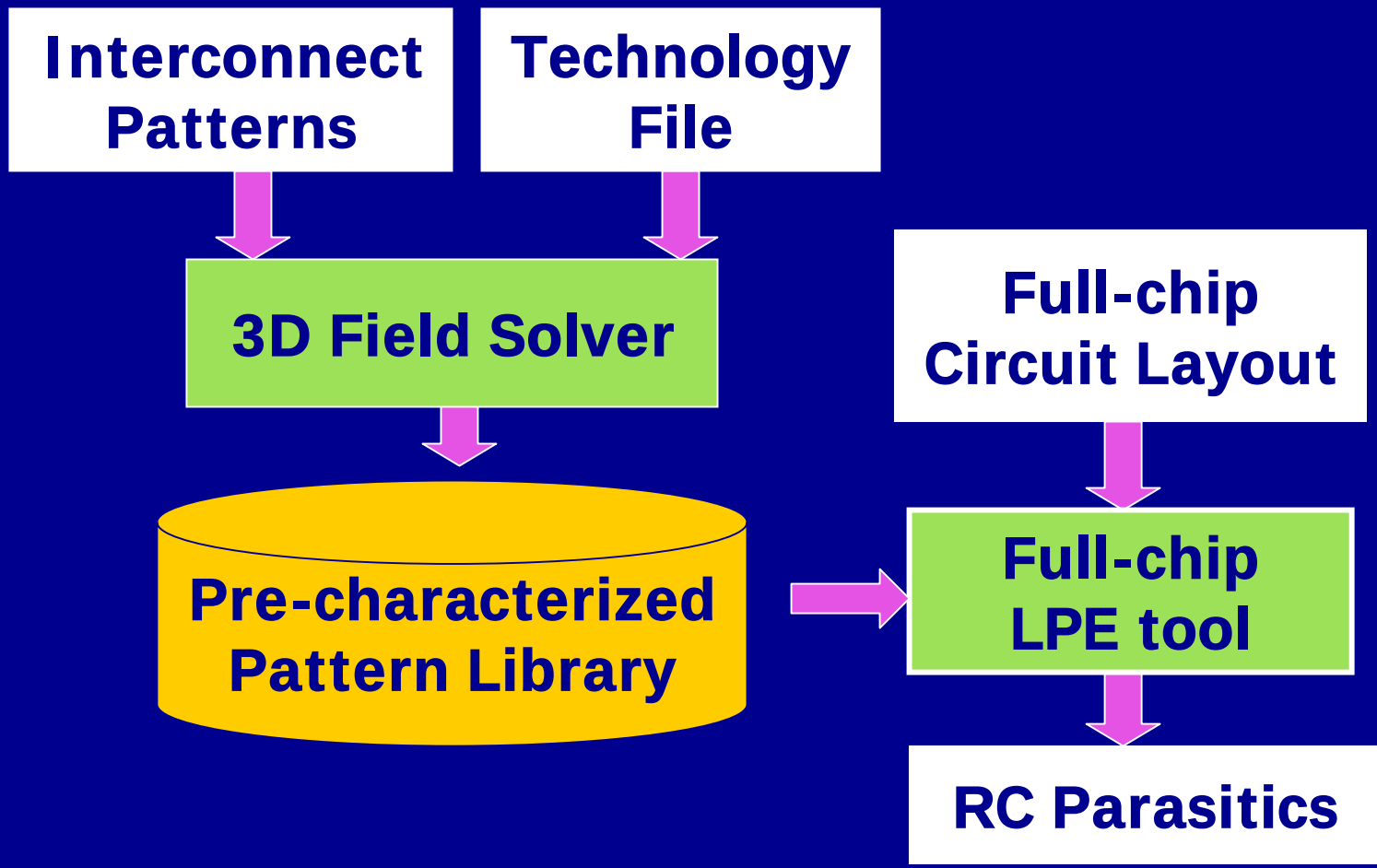
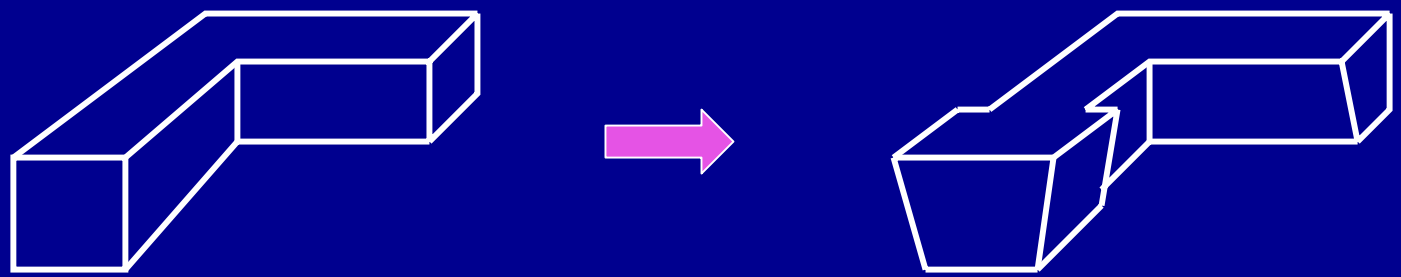
Traditional Full-Chip LPE Flow



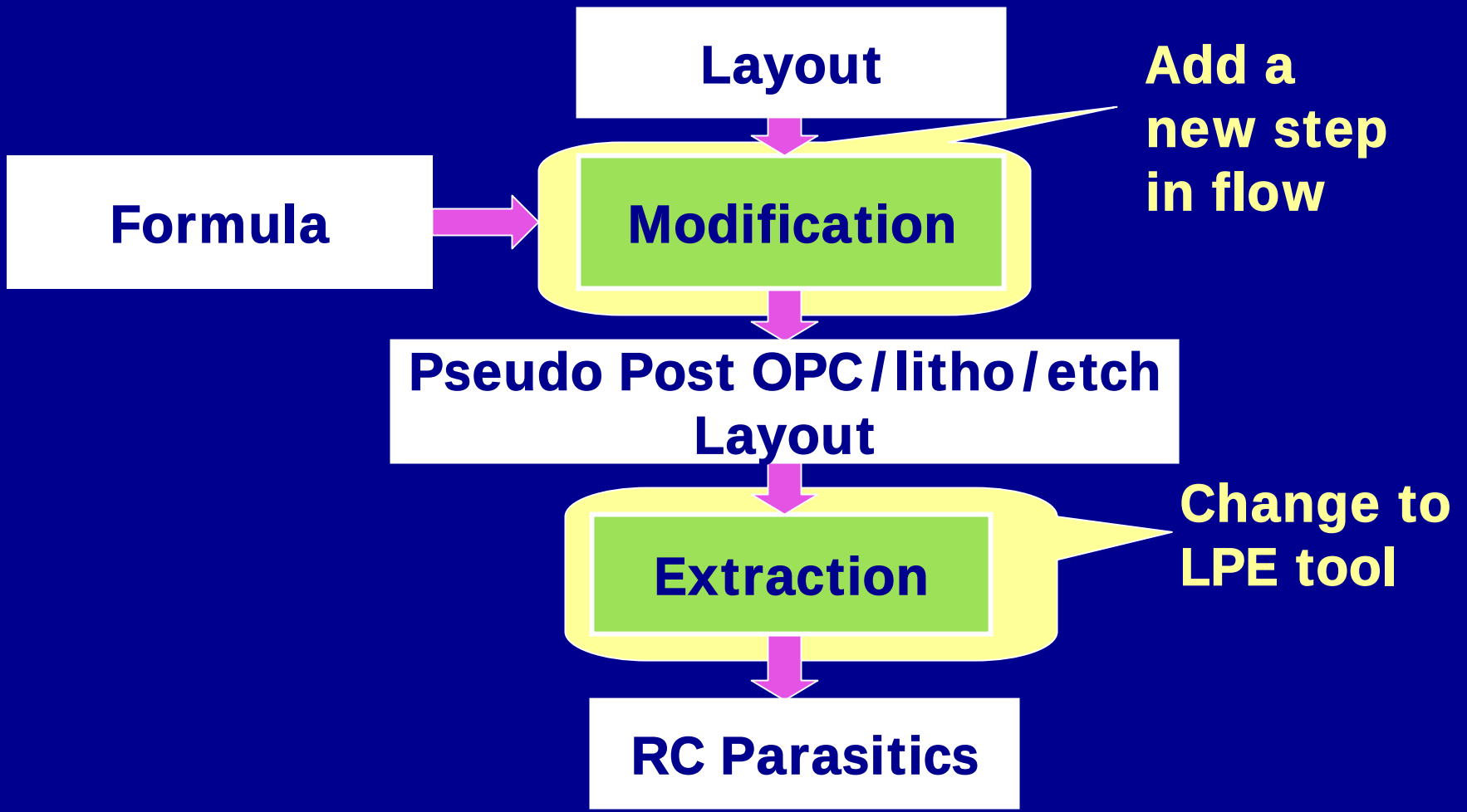
Formula-Based Approach

- Use a formula to predict the OPC/litho/etch effect
  - Width expanded = F(layer)
  - OPC width = F(spacing, width)
  - Sidewall shape = F(Z)

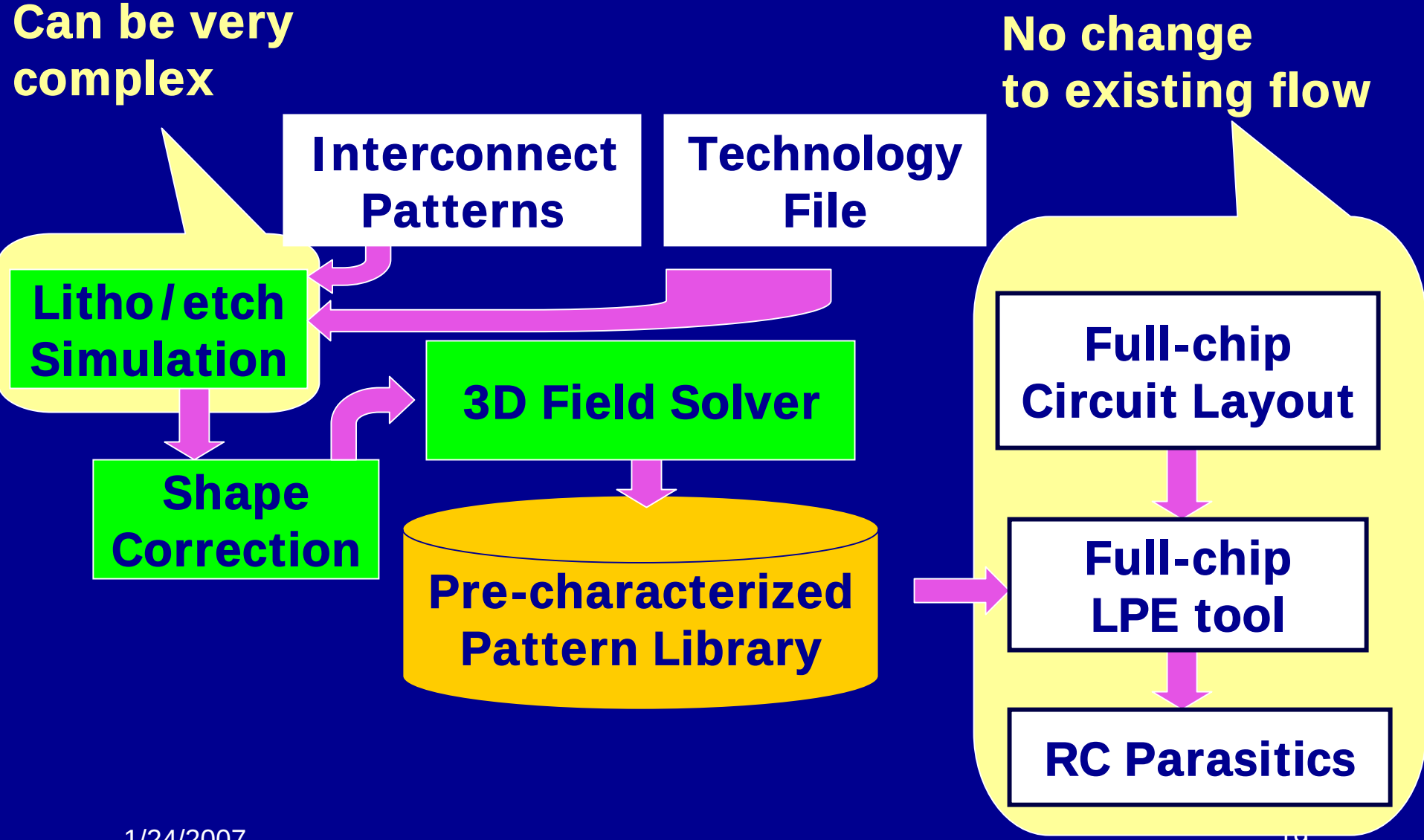


- Formula could be complex or inaccurate

Formula-Based Approach Flow



Peoposed LPE Flow



Features of New Methodology

- Minimum change to existing flow
  - Only change is to characterization step
  - No change to LPE tools
  - No increase in LPE run time
- Allows complex OPC/litho/etch simulation
  - Independent of rest flow
  - Performed only for selected patterns
  - Performed only once for each technology
- New requirements
  - 3D field solvers for non-rectangular conductors
  - Shape correction for speed up
  - May need more patterns due to non-local litho effect

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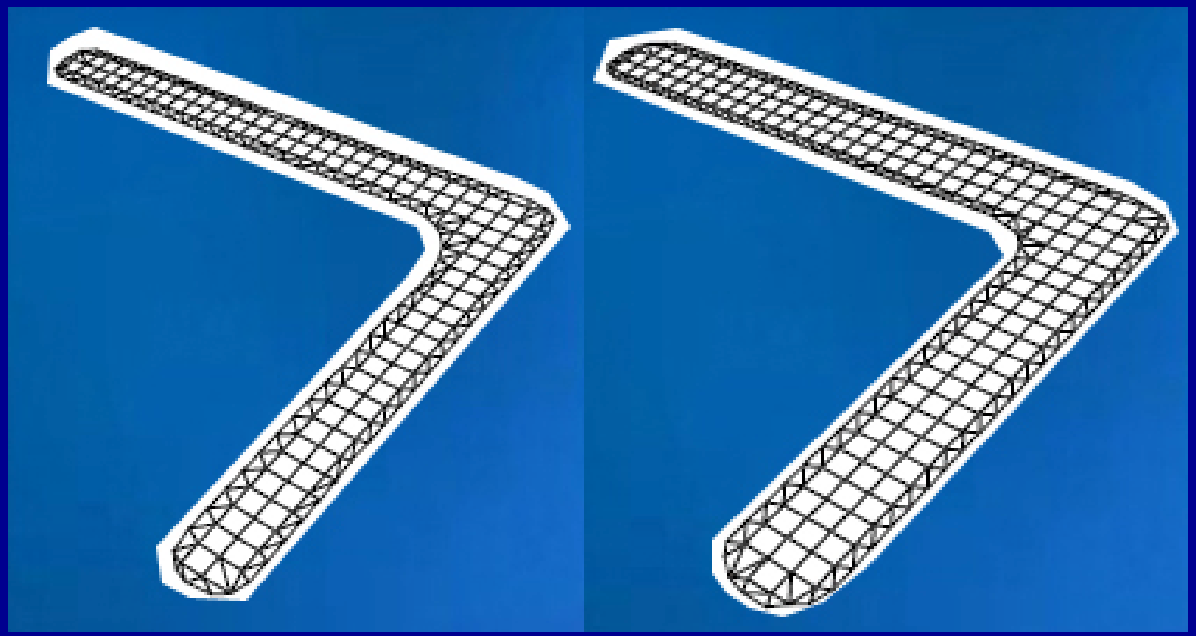
Requirement for 3D Field Solver

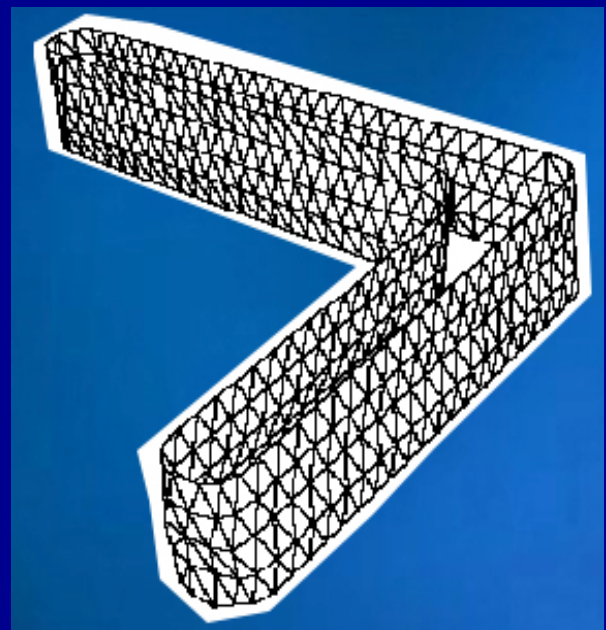
- Need 3D field solvers capable of solving non-rectangular conductors
- Boundary Element Method (BEM) algorithms can solve rectangular or non-rectangular conductors in the same amount of time
  - Conductor surfaces are discretized into triangles and rectangles
  - Whether the conductor is rectangular or non-rectangular makes little difference
  - FastCap is used to demonstrate the concept

Surface Discretization

- Discretization two types of surfaces



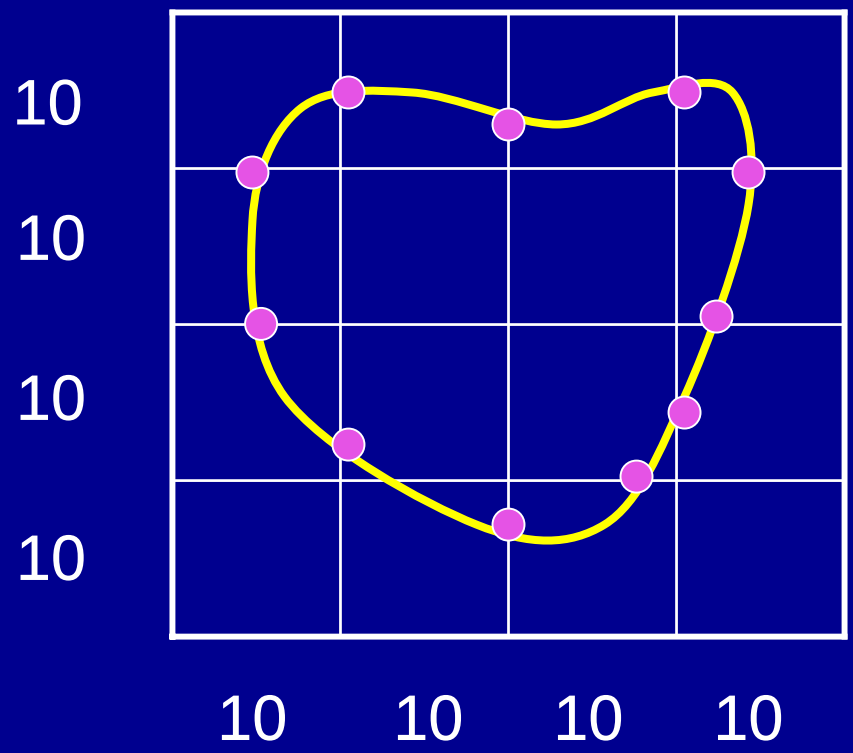
Top and bottom



Side wall

Discretize Top/Bottom Surfaces

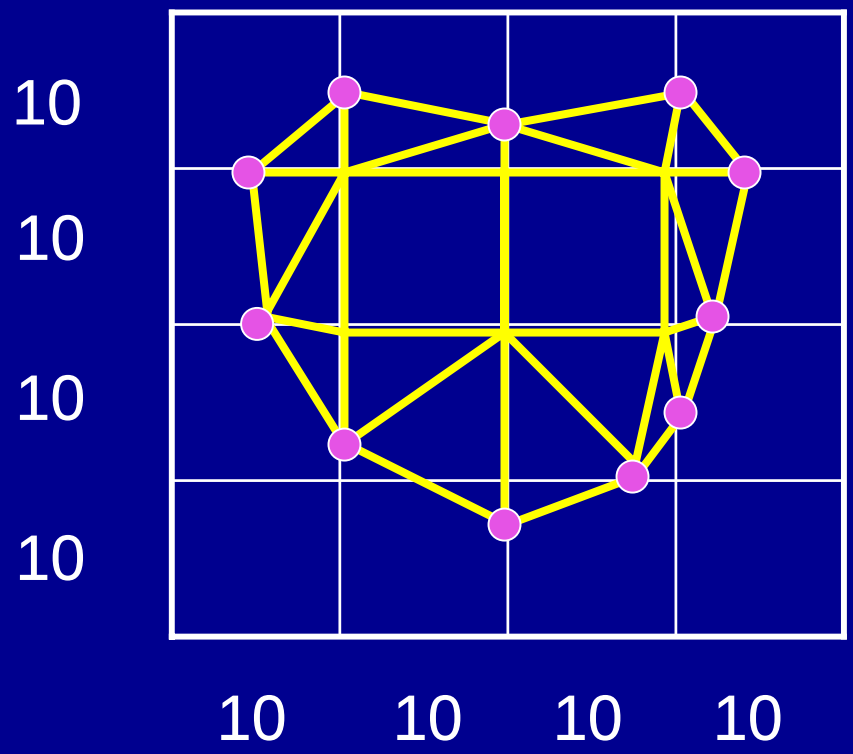
- Litho simulation tools allow the user to specify increment of x and y in output:



INC of X = 10
INC of Y = 10

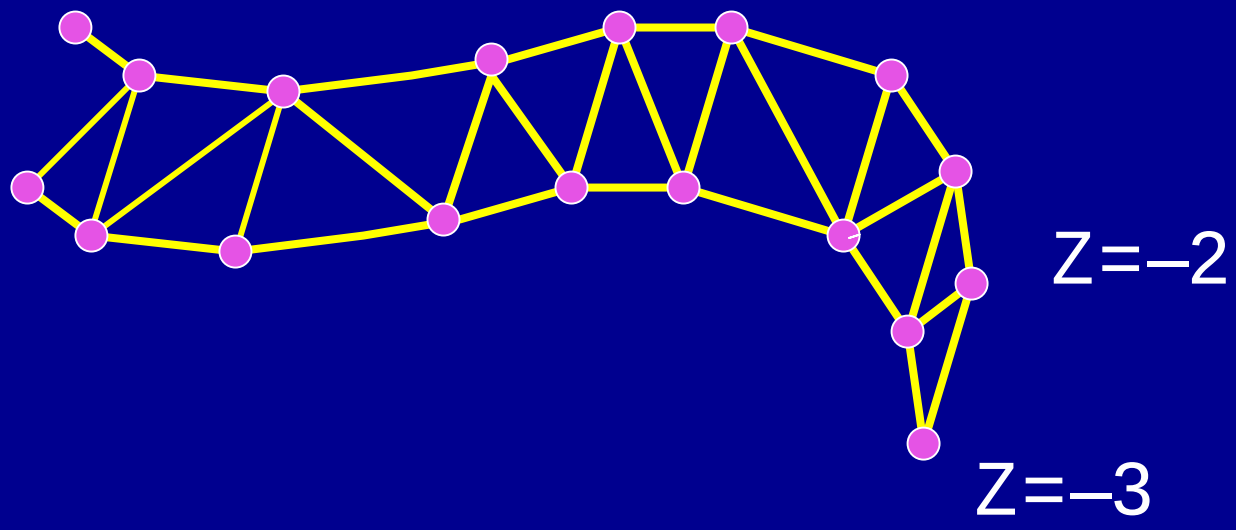
Grid Helps Discretization

- Inside regions are divided into squares
- Boundary regions are divided into triangles

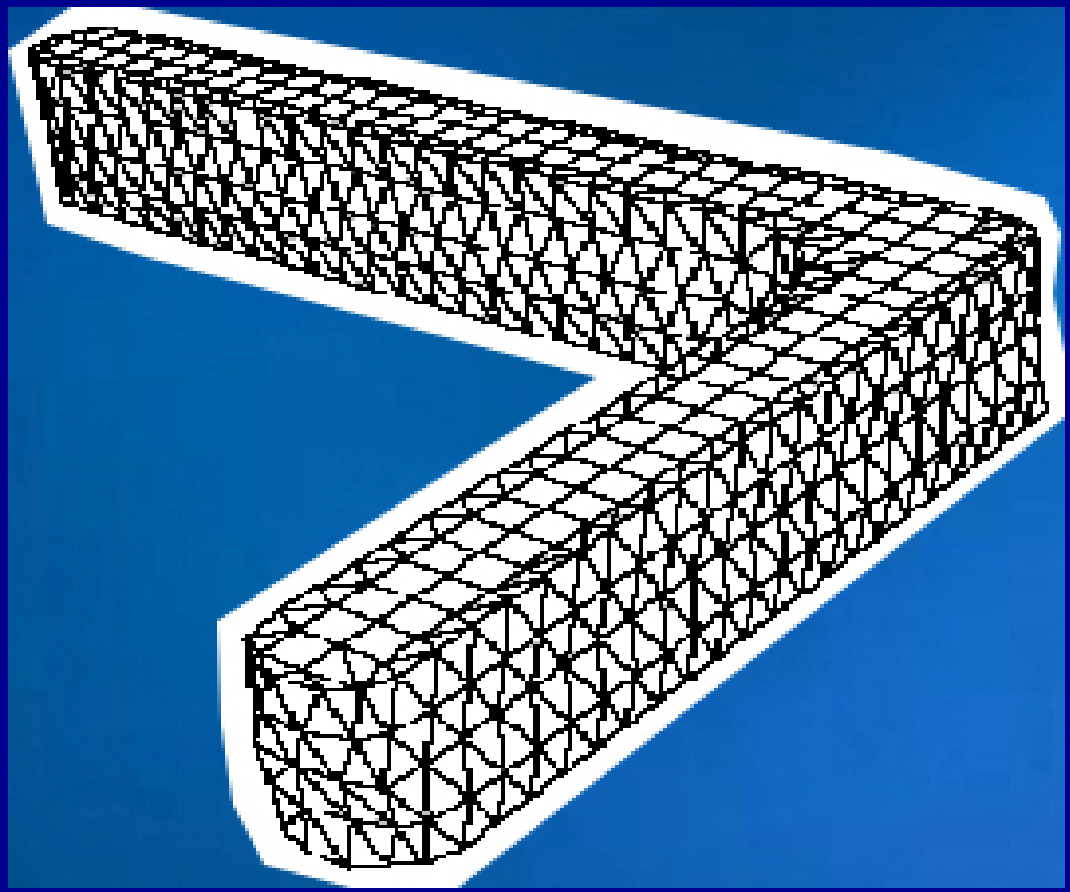


Discretization Side Wall

- Sidewall consists of curves at various elevations
- Triangulate between two adjacent elevations
- Each point is connected to its nearest neighbor



Final Result



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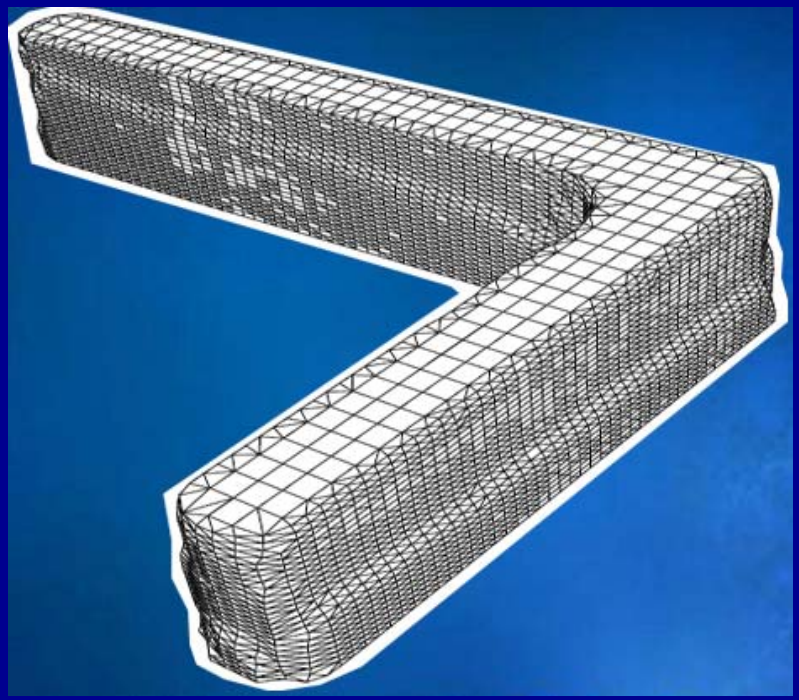
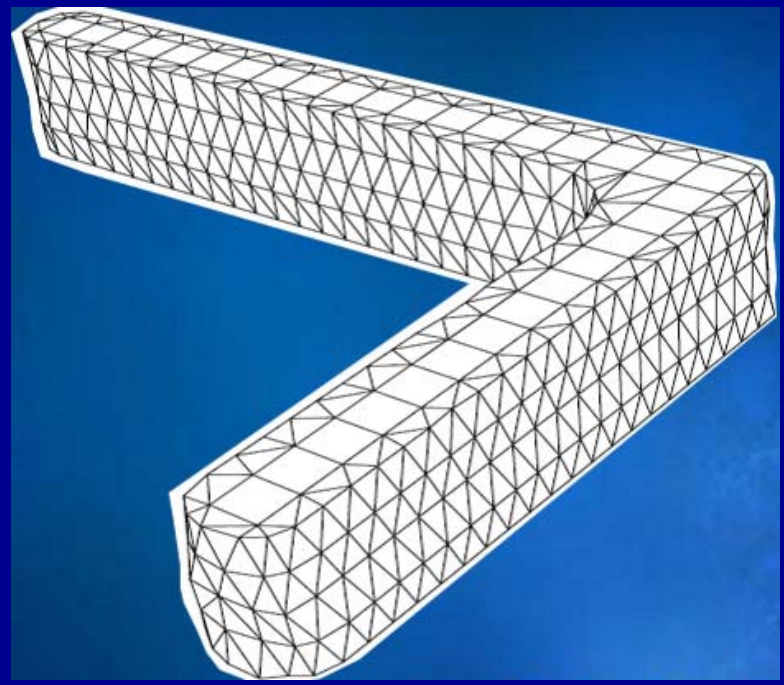
Why Shape Correction

- Surface discretization could produce too many panels, causing long run time for 3D filed solver
- Need to reduce the number of panels without sacrificing accuracy

Shape Correction Example



Original surface
30 elevations



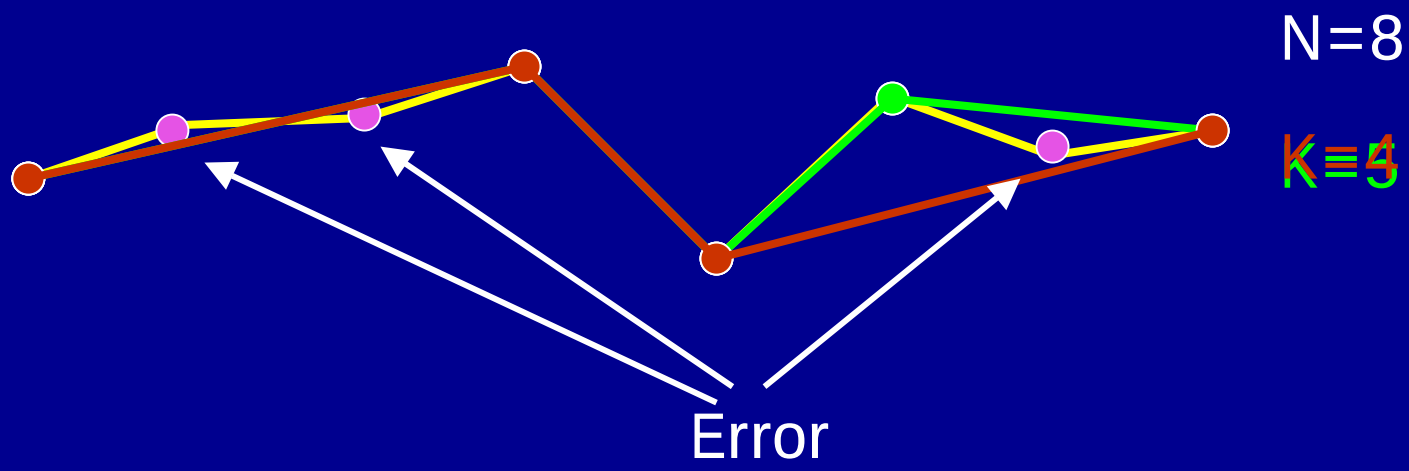
Corrected shape
5 elevations
10X faster, 1% error

Shape Correction Algorithm

- Problem formulation:
  - Given n contours $T(Z_1)$, $T(Z_2)$, …, $T(Z_n)$ for elevations Z_1, Z_2, …, Z_n respectively
  - Pick k contours such that the sum of error in shape is minimum
- We propose an optimal algorithm based on dynamic programming
- Near optimal yet faster algorithms for future research

Basic Idea in 2D

- Given a curve of N points, approximate it using a curve of K points, K < N
- Define error as the sum of difference between two curves
- Which K points to pick that minimizes error?



Dynamic Programming

- Let E(a, b; j) be the minimum error for approximating the curve from a to b using j points
- Since errors in different segments of the approximation are additive, we have

  $E(a, b; j) = \min \{E(a, c; 2) + E(c, b; j-1)\}$

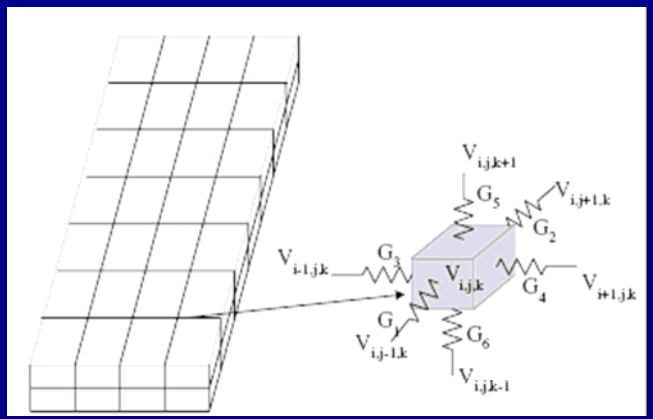
  where min is over all point c between a and b
- E(1, n; k) can be computed in $O(n^3)$ time using dynamic programming

Error and CPU Time

ERROR	OPC / litho / etch shape	5 elevation	3 elevation	2 elevation
Single elbow	-	1.45 %	1.73 %	2.30 %
Single bus	-	0.32 %	0.72 %	1.39 %
Parallel bus	-	1.31 %	4.80 %	7.92 %
1x1 bus	-	0.55 %	1.25 %	1.94 %
2x2 bus	-	1.14 %	3.68 %	5.74 %
Total Time (s)	1404.4	148.4	91.2	72.5
Memory (MB)	932.3	121.8	75.4	53.8

Resistance Extraction

- Traditional algorithms use formula
  - R = L/W * sheet resistance
- FDM (Finite Difference Method)
  - Handle non-regular shapes
  - Solves a sparse linear system



$$I = (G_1 + G_2 + G_3 + G_4 + G_5 + G_6) V_{i,j,k}$$
$$- G_1 V_{i,j-1,k} - G_2 V_{i,j+1,k} - G_3 V_{i-1,j,k}$$
$$- G_4 V_{i+1,j,k} - G_5 V_{i,j,k+1} - G_6 V_{i,j,k-1}.$$

$$G_i = \sigma A_i / L_i,$$

Conclusion

- New methodology to deal with OPC/litho/etch effect in interconnect parasitic extraction
  - Minimum change to existing design flow
  - Minimum increase in extraction time
- New algorithms for discretization and shape approximation
  - Top/bottom surface discretization
  - Side-wall triangulation
  - Shape approximation
- New methodology and algorithms reduce extraction error from 20% to under 5%.