Simple and Accurate Models for Capacitance Increment due to Metal Fill Insertion

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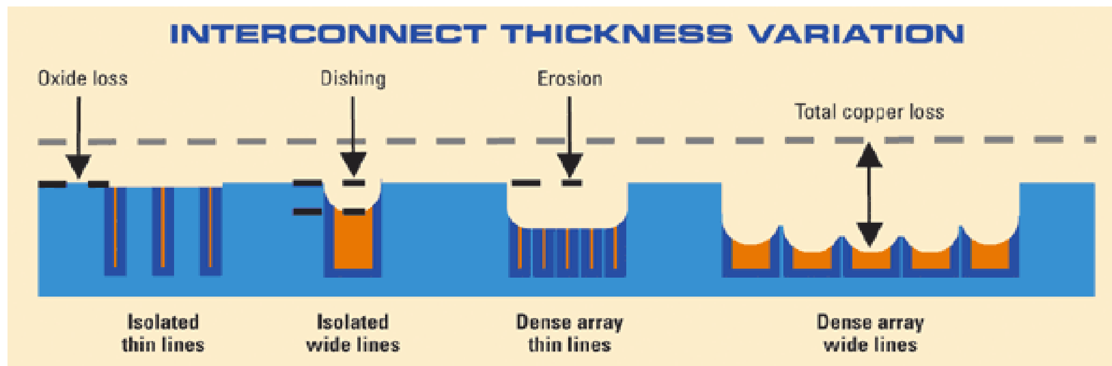
Outline

- **Introduction & Motivation**
- Analysis of Metal Fill and Guidelines
- Capacitance Increment Models
  - Intra-layer Metal Fills
  - Inter-layer Metal Fills
- Model Verifications
- Conclusion and Future Works

CMP(Chemical-Mechanical Polishing)

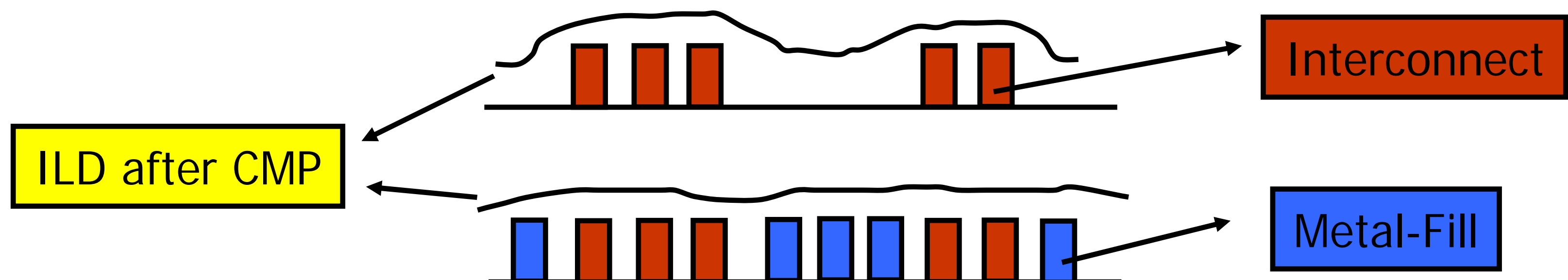
- CMP technique is essential for oxide planarization in current VLSI manufacturing process
  - But, erosion and dishing problems
  - Lack of planarity → problems in lithography(DOF) and etching
  - Can be applied for several structures; Bare silicon, STI for active layer, Metallization, and ILD layers for interconnects
- The CMP-induced problem has become more important
  - Multilevel interconnects; CMP-induced ILD thickness variation is accumulative
  - Aggressive scaling for feature size of devices (L, W)
  - Higher need for performance
  - Die and wafer size are getting larger (e.g., wafer 200mm → 300mm)



(Source Praesagus)

Dummy Metal Fill

- Metal-Fill insertion and CMP
  - Electrically inactive(grounded or floating) and not for optical assistance (e.g. SBs)
  - Minimize local density variation
  - Minimize variation of ILD thickness after CMP
- Creates new problems
  - Increase interconnect capacitance
    - Delay, coupling/crosstalk noise, and power consumption
  - Design verification and mask data preparation issues
  - Accuracy of parasitics extraction of full-chip w/o dummy
    - Dummy usually inserted at tape-out stage and before OPC process



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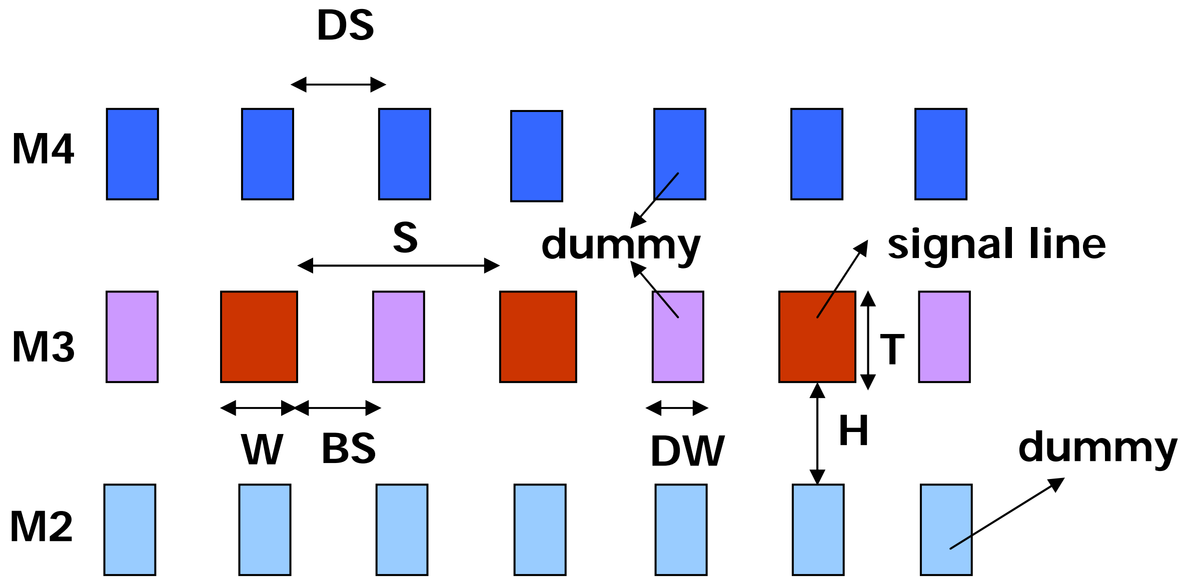
Analysis of Metal Fill and Guidelines

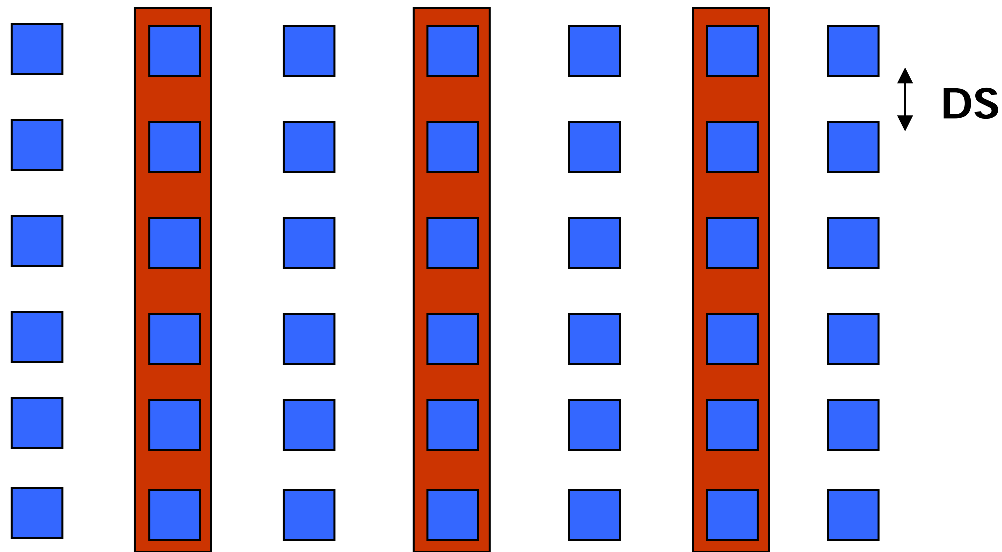
- Electrical Property
  - Grounded vs. Floating
- Location
  - Intra-layer vs. Inter-layer
- Buffer Space
- Signal Width and Space
- Dummy Fill Density
- Dummy Shape and Dimension

Simulation Setups

- Use *QuickCap* as a 'Golden tool'
  - *'float'* command for floating dummy metals
  - Accuracy 1%; ex) quickcap –d1% -m30
  - Extract cap. (*Ctot, Cg, Cc*) between w/o and w/ metal-fills
- All technology parameters from ITRS 130nm technology node
- 3 metal layers (M2, M3, M4)
  - M3 for signal lines
  - Intra/inter-layer metal fills analysis
- 3 signal lines of 10um long and extract *Ctot* (*Cc* and *Cg*) of the middle line

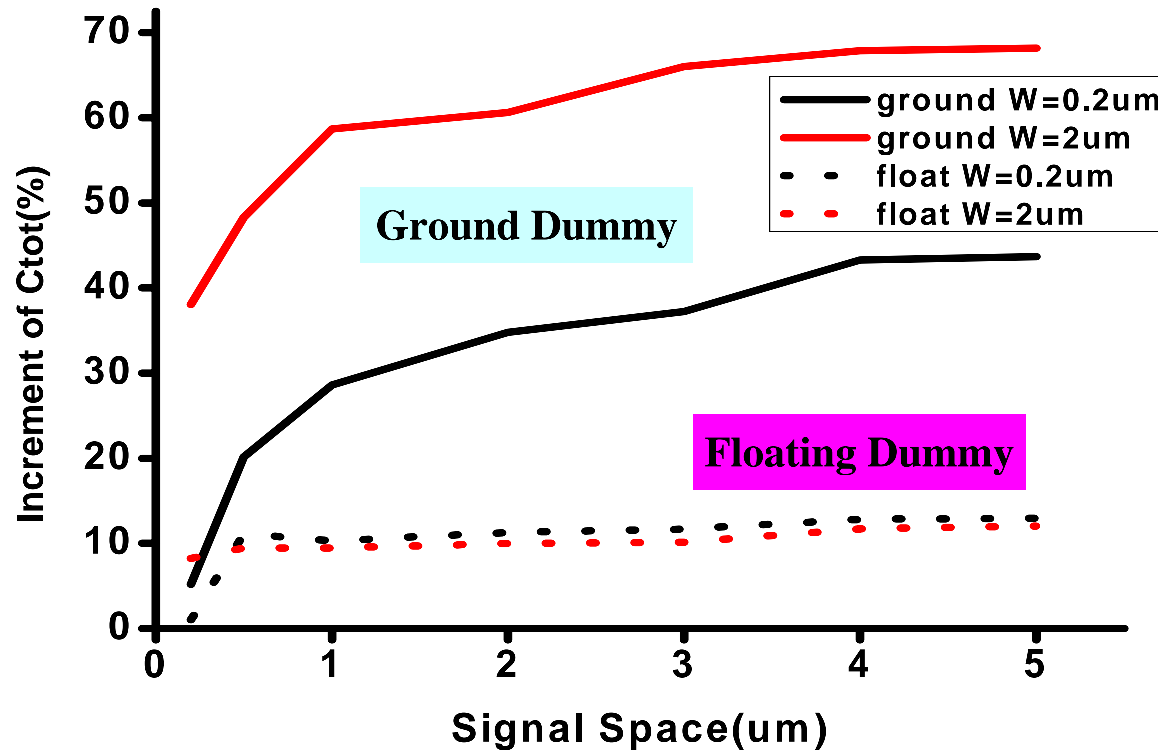


Side view



Top view

Grounded vs. Floating



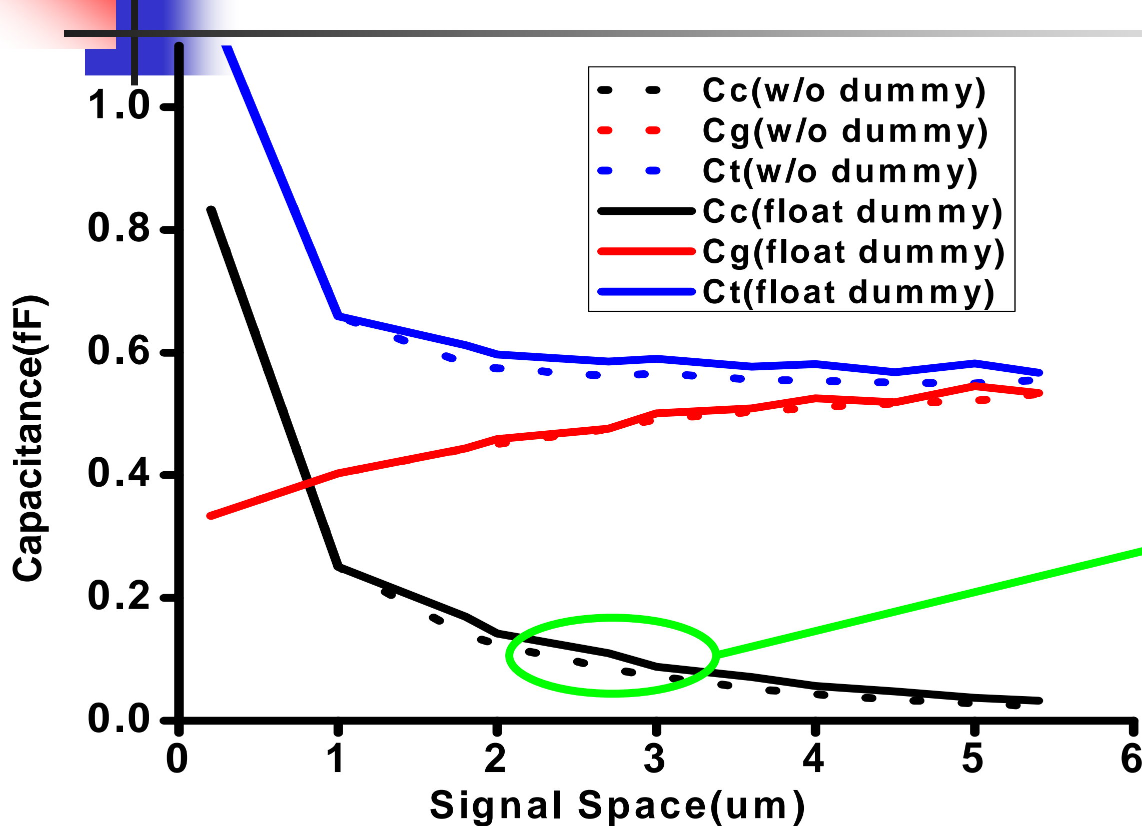
Grounded dummy is not used much due to higher impact on capacitance and routing difficulties (DW=BS=0.6um, 60% density)

- Grounded Dummy (~ 70%)
  - Wider signals have more impact
  - Signal space dependency (saturates when the space is enough to insert dummy)
- Floating Dummy (~12%)
  - No big dependency on signal width or space

Grounded vs. Floating

- Grounded
  - Affect delay (e.g., *Ctot*)
  - Easy to estimate → traditional layout-extraction tool can be used
  - Routing problem → prefer long lines
- Floating
  - Affect coupling and crosstalk (e.g., *Cc*)
  - Hard to estimate → metal-fill generated automatically during tape-out
  - Additional coupling paths → prefer segmented metals

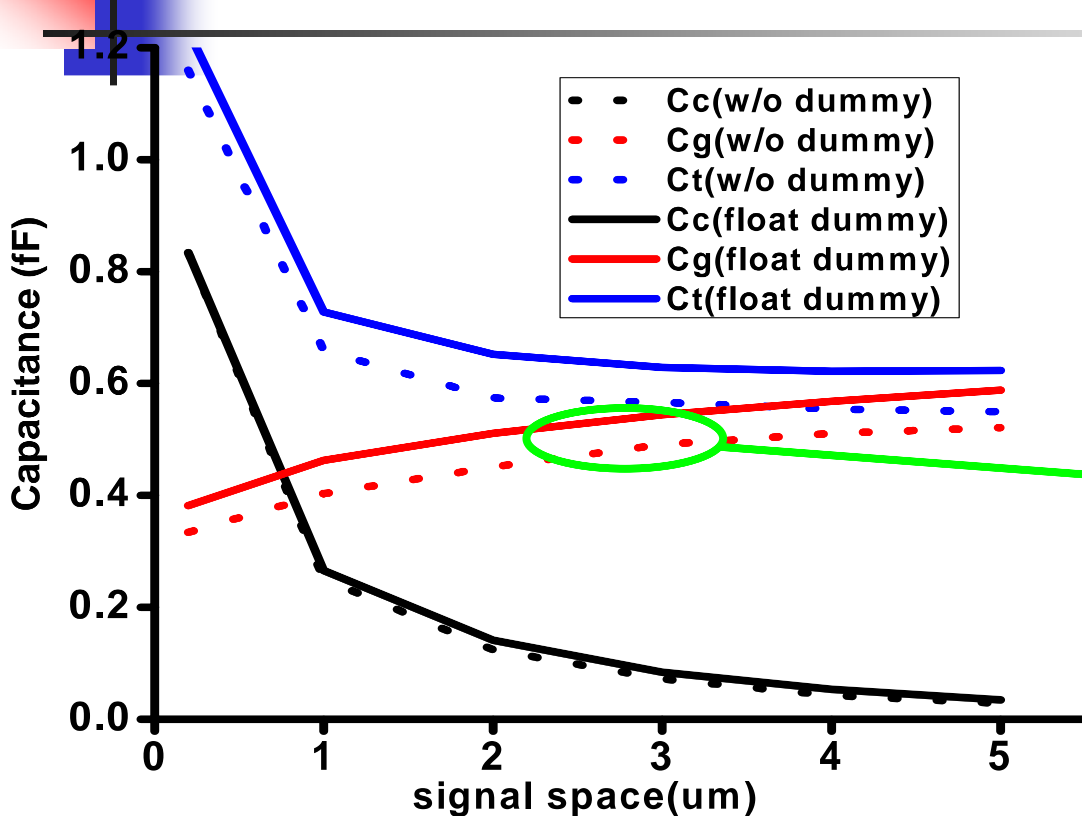
Intra-layer dummy



Space (um)	Cap. Increment(%)		
	Cc	Cg	Ct
0.2	**0.00%**	**0.00%**	**0.00%**
1	**0.00%**	**0.00%**	**0.00%**
2	**14.03%**	**0.87%**	**4.77%**
3	**21.67%**	**0.81%**	**4.25%**
4	**30.99%**	**0.40%**	**5.38%**
5	**29.25%**	**0.75%**	**4.35%**

- Negligible impact on the *Cg*
- Big impact on the *Cc*, but small portion in *Ctot* (< 1/10 of *Cg*)
- Buffer space and density (i.e., dummy space, dummy size) are important factors

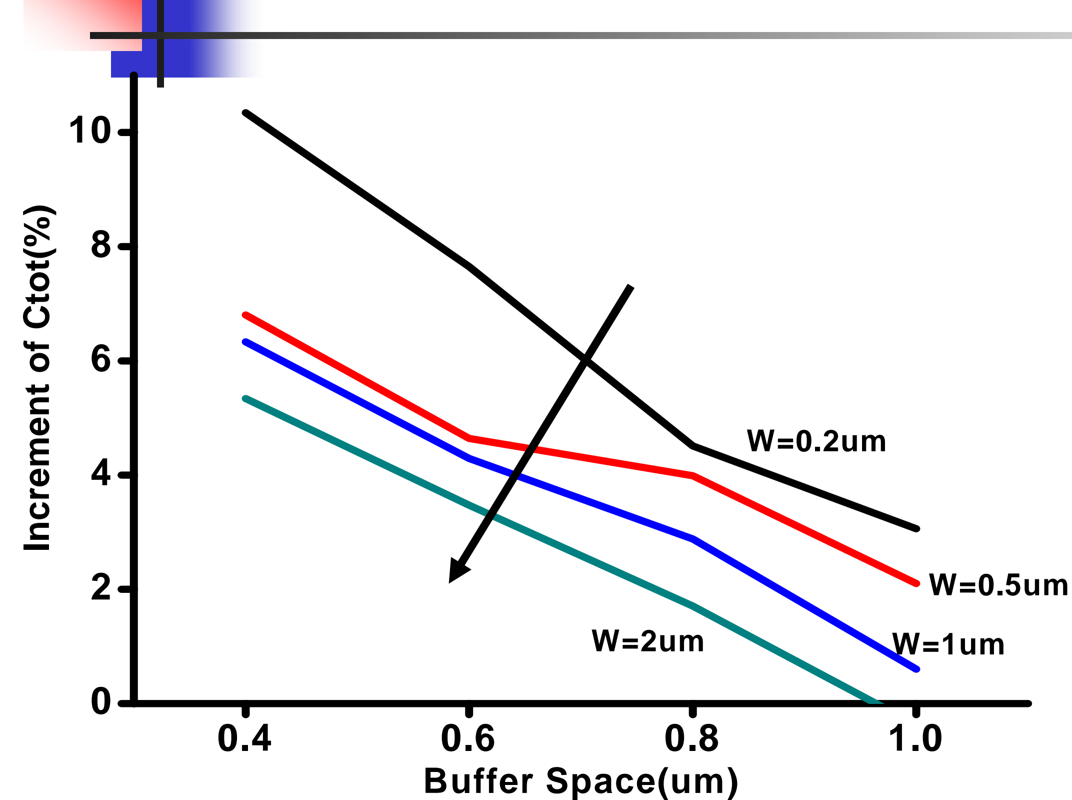
Inter-layer dummy



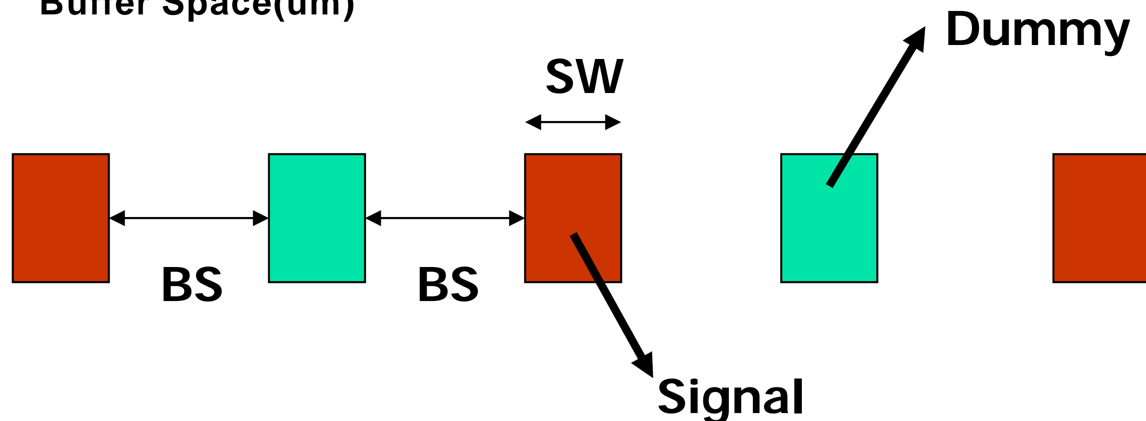
Space (um)	Cap. increment(%)		
	Cc	Cg	Ct
0.2	**0.09%**	**12.64%**	**4.96%**
1	**4.55%**	**14.06%**	**9.53%**
2	**10.61%**	**12.77%**	**12.51%**
3	**12.25%**	**10.80%**	**10.44%**
4	**17.72%**	**10.98%**	**11.57%**
5	**15.56%**	**11.27%**	**11.68%**

- Impact on both *Cc* and *Cg* components
- *Cc* component in *Ctot* is getting smaller as space increases (< 1/10 of *Cg*)
  - *Ctot* increment mainly due to *Cg* increment

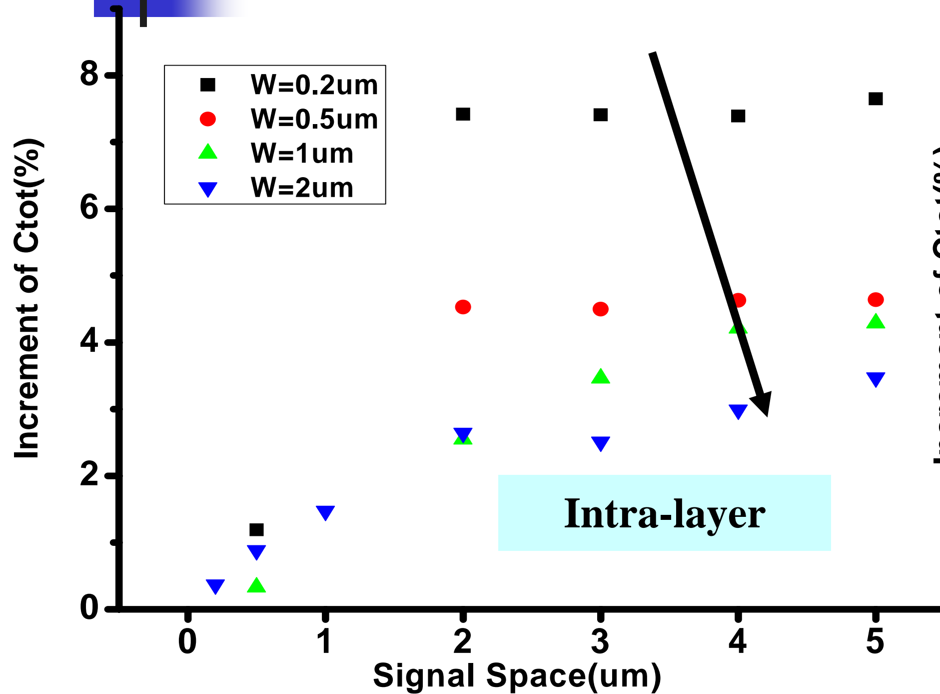
Buffer Space(BS); Intra-layer

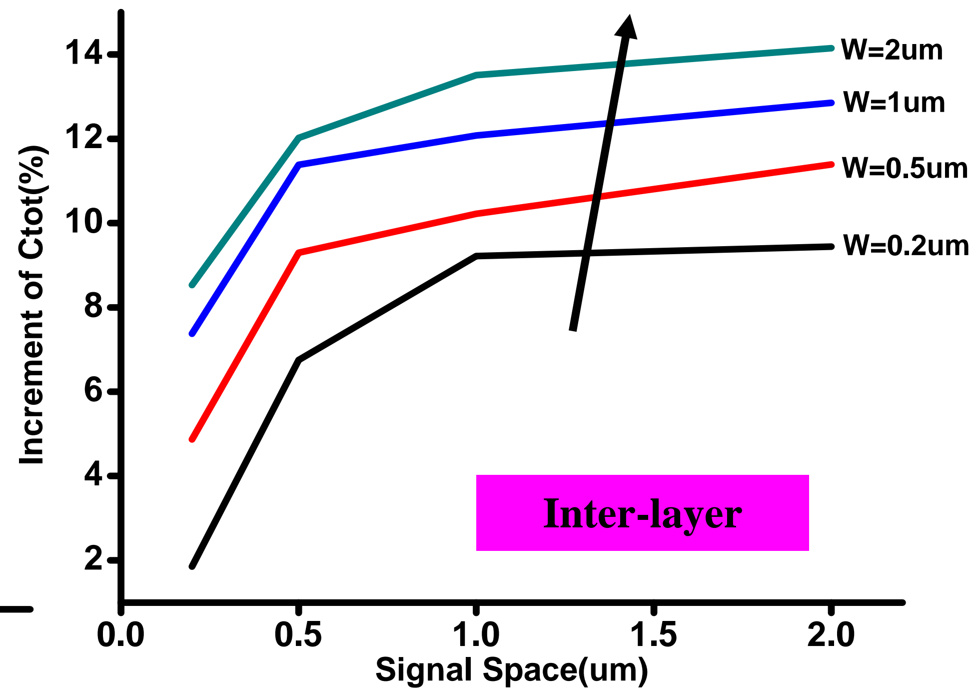


- Minimum distance of floating dummy from interconnect
- One of major factors
- *Ctot* increment decreases as signal width increases
- BS=0.4um →0.8um; 50% reduction



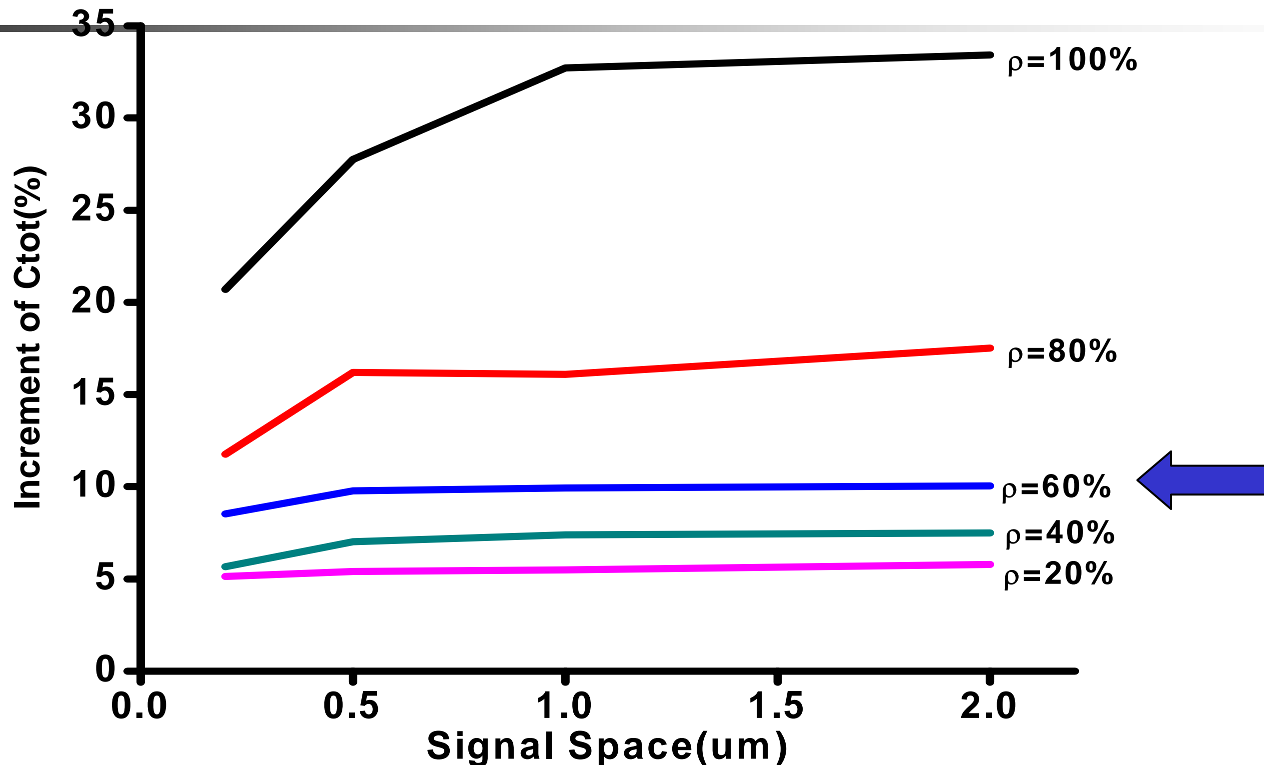
Signal Width and Spacing





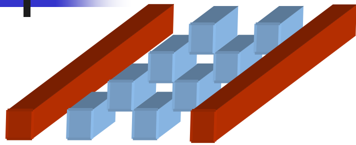
- Intra-layer dummy: *ΔCtot* decreases as width increases
- Inter-layer dummy: *ΔCtot* increases as width increases

Signal Space & Density(W=2um)

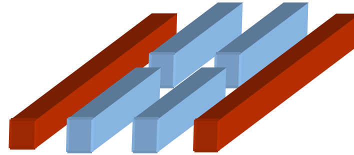


- Strong dependency on dummy density of other layers (inter-layer)
- *ΔCtot* saturates when signal space > 1um
- At density 60%: ~ 10% cap. increment by floating metal fills

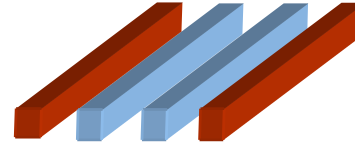
Dummy Shapes and Orientation



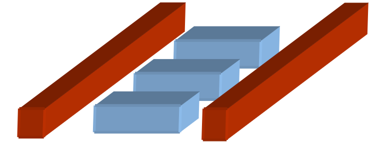
Square



Rectangular



Parallel line



Orthogonal

Ground Dummy
Float Dummy

Increment of Ctot(%)

60
50
40
30
20
10
0

square rectangular line orthogonal

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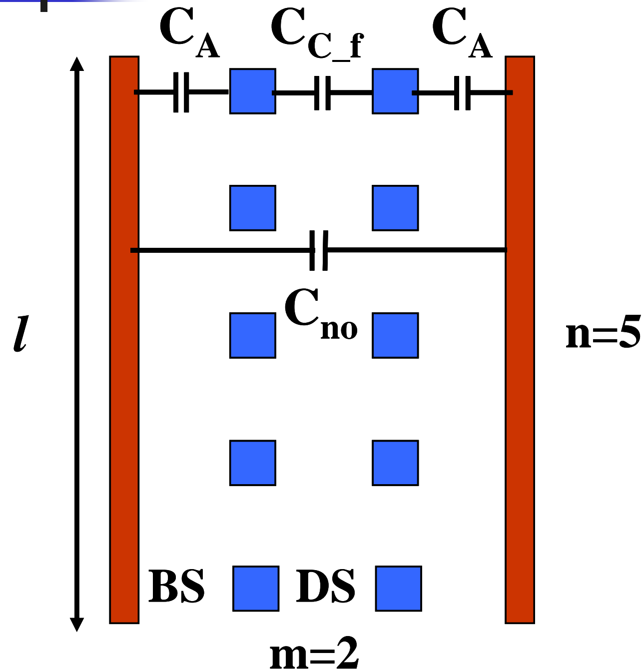
Capacitance Increment Models

- Intra-layer dummy
  - Negligible impact on signals when buffer space > 1um
  - More impact on *Cc*
  - Model only for coupling capacitance change
  - Parallel plate capacitance model
- Inter-layer dummy
  - More impact on *Cg*
  - Model only ground capacitance change
  - Approximate the floating dummy structure with dummy thickness reduction [Kurokawa '04]
  - Ratio of dummy to signals (α)
- For 3D impact we combine the models by summing up the impact with α

Intra-layer dummy (Cc_inc)



$$C_C(\text{w/ dummy}) = C_{C_inc}(\text{intra}) + C_C(\text{w/o dummy})$$
$$= C_{dummy} \times DW \times n + C_{no} \times (l - DW \times n)$$

$$C_{dummy}(F/um) = \frac{\varepsilon \cdot T}{2BS + DS} \quad ;\text{when m=2}$$

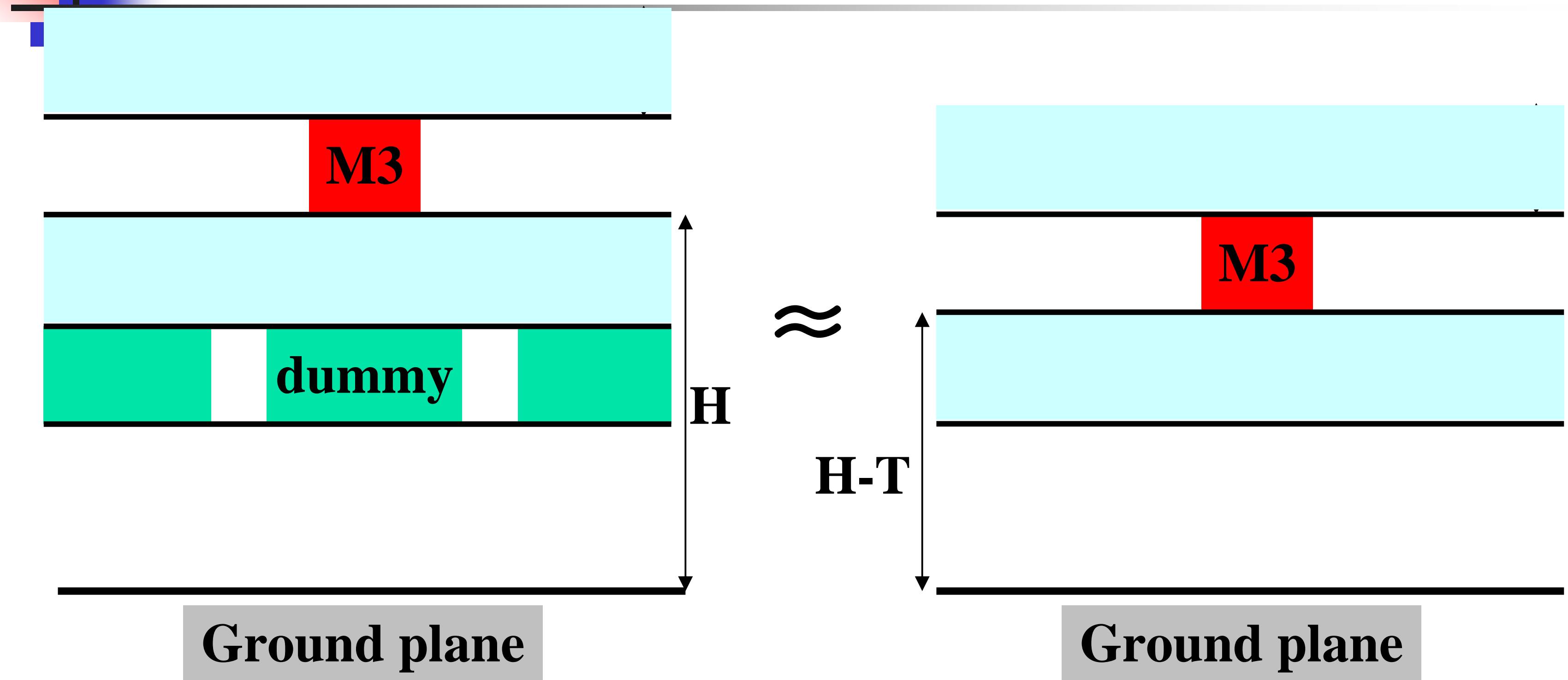
$$C_{dummy}(F/um) = \frac{\varepsilon \cdot T}{2BS + (m-1)DS}$$

[Y. Chen et al., DAC2003]

- DW=dummy width, DS= dummy space
- T = dummy thickness, BS = buffer space
- l = line length
- m=# of dummy column between signals
- n = # of dummy in one column
- Above example: m=2, n=5

$$\therefore C_{C_inc}(F) = \frac{\varepsilon \cdot T}{2BS + (m-1)DS} \times DW \times n$$

Inter-layer dummy (Cg_inc)



- Approximate the floating dummy impact by reducing its thickness [A. Kurokawa, CICC 2004]

$$C_{g_inc}(\text{inter}) = C_g(H-T) - C_g(H)$$

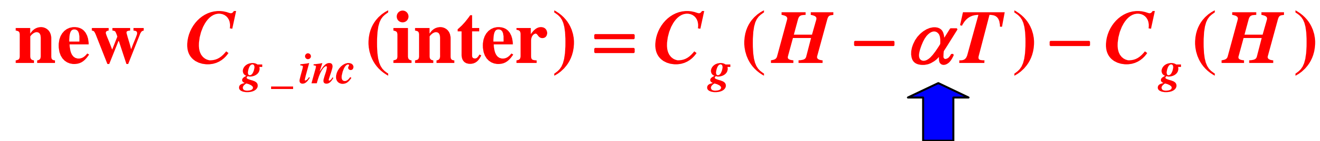
where $C_g \sim f(W, H, T, S)$

[S.C. Wong, Trans. on Semi. Manu. IEEE2000]

Combining Intra/Inter-layer dummy

$$C_{tot}(\textbf{w/ dummy}) = C_{tot}(\textbf{w/o dummy}) + C_{C_inc}(\textbf{intra}) + C_{g_inc}(\textbf{inter})$$

$$\begin{cases} C_{C_inc}(\textbf{intra}) = \dfrac{\varepsilon \cdot T}{2BS + (m-1)DS} \times DW \times n \\ C_{g_inc}(\textbf{inter}) = C_g(H-T) - C_g(H) \end{cases}$$



- *Cc* increment by intra-layer dummy
- *Cg* increment by inter-layer dummy
- In real designs, not all space under the signal layer is occupied by dummy → signals run orthogonally
- The model is still applicable by using weighting function (α) on the thickness of dummy layer

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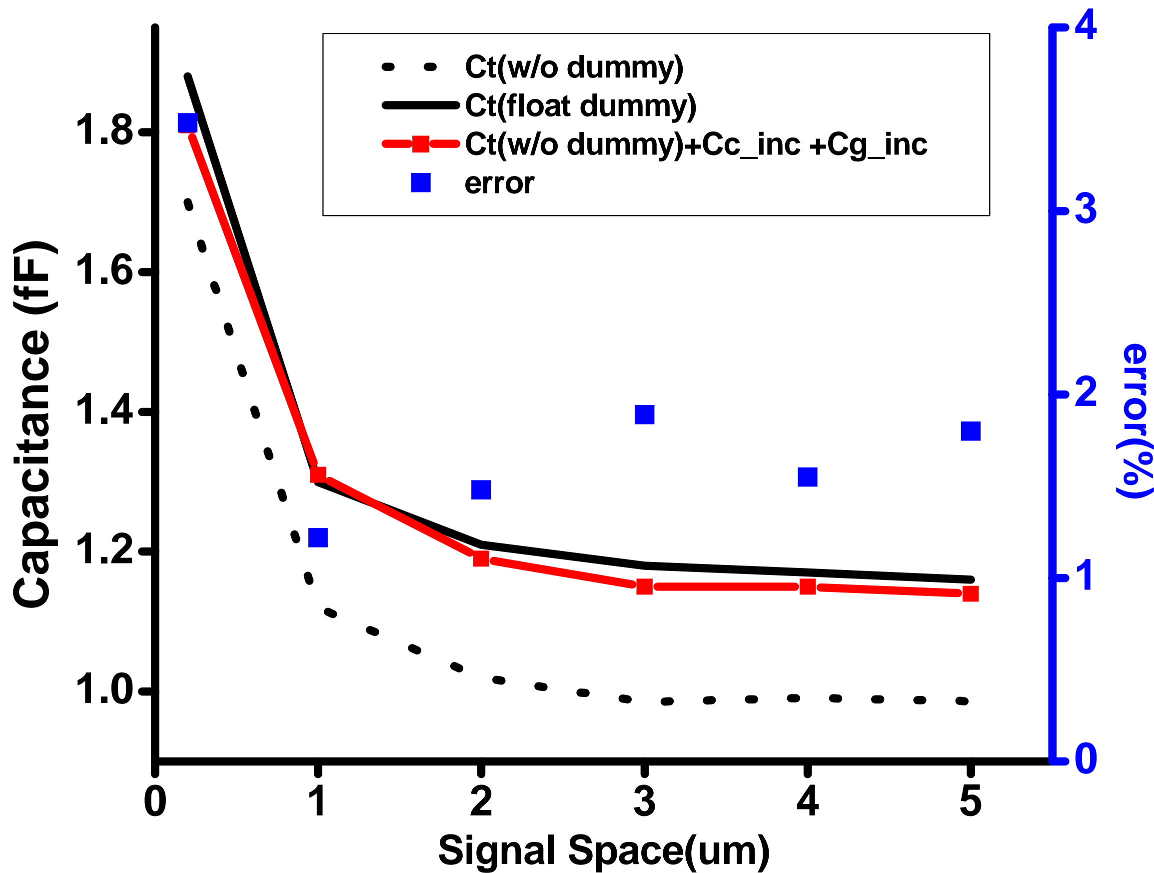
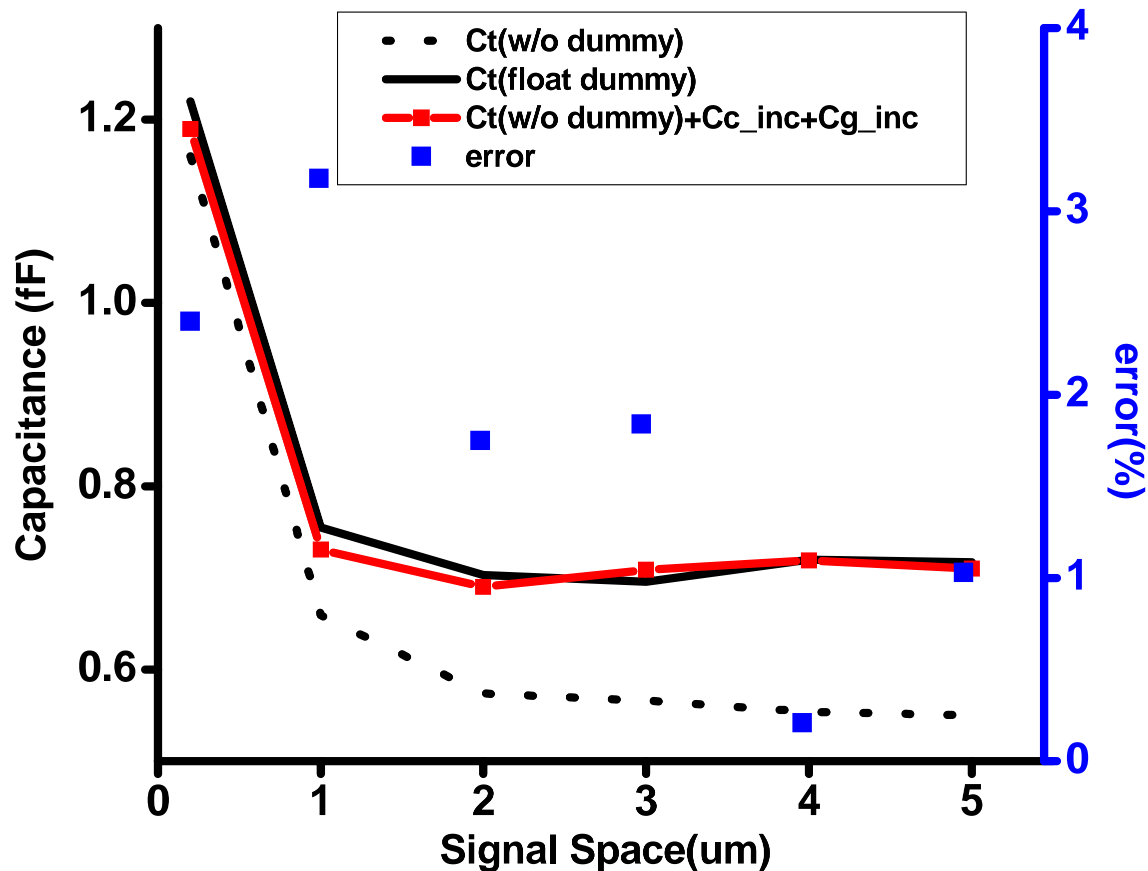
Case1:W=2.0um, DW=0.6um, DS=0.3um, square



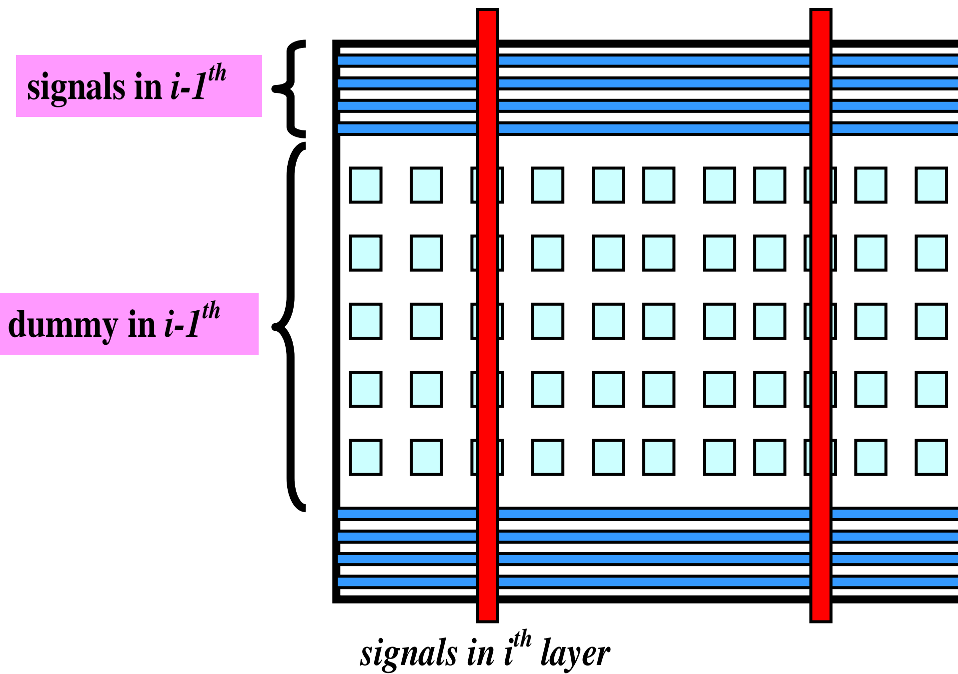
Space (um)	error(%)		
	Cc_inc only	Cg_inc only	Cc_inc + Cg_inc
0.2	**-9.33%**	**-3.48%**	-3.48%
1	**-13.74%**	**1.22%**	1.22%
2	**-12.27%**	**-5.02%**	-1.48%
3	**-13.38%**	**-4.72%**	-1.89%
4	**-13.03%**	**-3.98%**	-1.55%
5	**-13.15%**	**-3.94%**	-1.80%

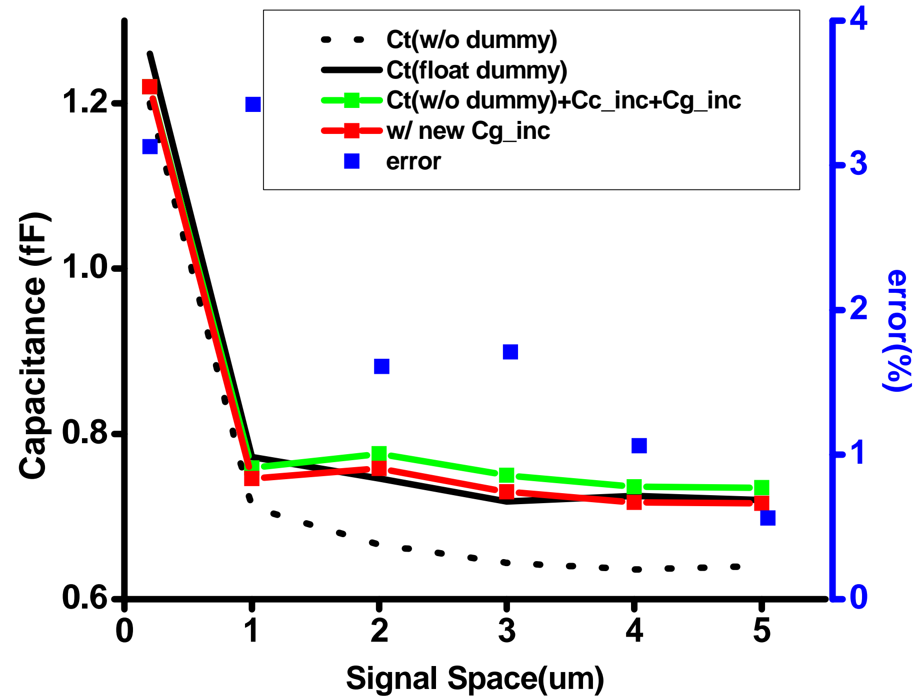
Case2: W=0.2um, DW=0.6um, DS=0.3um, orthogonal



Space (um)	error(%)		
	Cc_inc only	Cg_inc only	Cc_inc + Cg_inc
0.2	**-4.67%**	**-2.40%**	-2.40%
1	**-12.73%**	**-3.18%**	-3.18%
2	**-14.74%**	**-5.30%**	-1.75%
3	**-11.50%**	**-5.32%**	1.84%
4	**-12.63%**	**-10.59%**	-0.21%
5	**-12.87%**	**-11.45%**	-1.03%

Case3: W=0.2um, DW=0.6um, DS=0.3um, α=75%



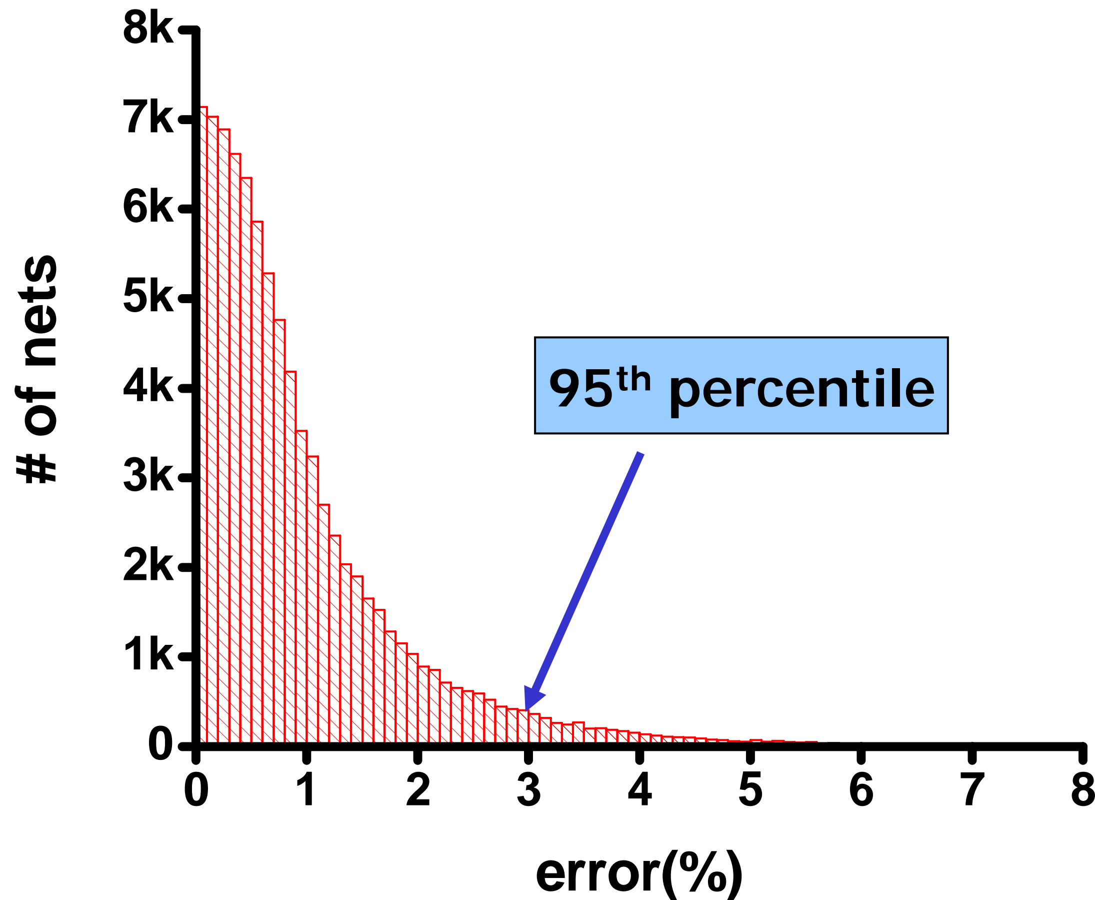


- The ratio of dummy area to signals in *n-1* layer (*n+1* also) within certain window size
- *α*=75% means 35% of area are interconnects

Block Verification

Circuits	# of gates	Total nets	Average Ctot (fF)			Errors (%)			Run Time (s)			
			w/o dummy	dummy + FNC	dummy + models	mean	median	95th percentile	w/o dummy	dummy + FNC	dummy + models	Savings (%)
c17	11	42	0.52	0.55	0.56	1.1	0.7	2.4	80	165	104	71.8
c432	140	770	1.11	1.30	1.34	1.2	0.6	4.5	120	180	135	75.0
c3540	521	2966	0.83	0.96	0.99	1.1	0.6	3.7	154	248	178	74.5
c6288	2118	13039	1.22	1.47	1.51	1.2	0.7	2.7	583	1177	707	79.1
S	14538	53401	0.48	0.62	0.63	1.3	0.9	4.1	1282	2832	1714	72.1
R	31930	114803	0.53	1.07	1.11	1.0	0.7	2.9	3765	6601	4533	72.9

Error Histogram (circuit R)



- Most of the nets have smaller error with proposed models
- 95th percentile: 2.9%

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Conclusion

- Bigger impact by grounded dummy than floating dummy (e.g., up to 70% vs. 12%)
- Intra-layer dummy has impact on Cc component
- If buffer space is > 1um, the impact by intra-layer dummy is negligible (< 2%)
- Inter-layer dummy has higher impact on Cg component
- Propose simple capacitance increment models
  - Cc: parallel plate capacitance model
  - Cg: reducing the dummy thickness and weighting function
  - Function of density and design rules (e.g., buffer space, dummy space, and dummy width, metal thickness, etc..)
- 1.2% average error and ~75% runtime savings

Future Work

- Smart insertion of metal-fills based-on the proposed increment models
  - e.g., Performance-impact limited fills [Y. Chen DAC 2003]
- Analysis of influence of metal-fills on the signal delay and crosstalk

Thank You !!