University of
Southampton, UK

Exploiting Power-Area Tradeoffs in Behavioural Synthesis through clock and operations throughput selection

M. A. Ochoa-Montiel
mao02r@ecs.soton.ac.uk

B. M. Al-Hashimi
bmah@ecs.soton.ac.uk

P. Kollig
peter.kollig@philips.com

School of Electronics and Computer Science

Electronic Systems Design Group

Outline

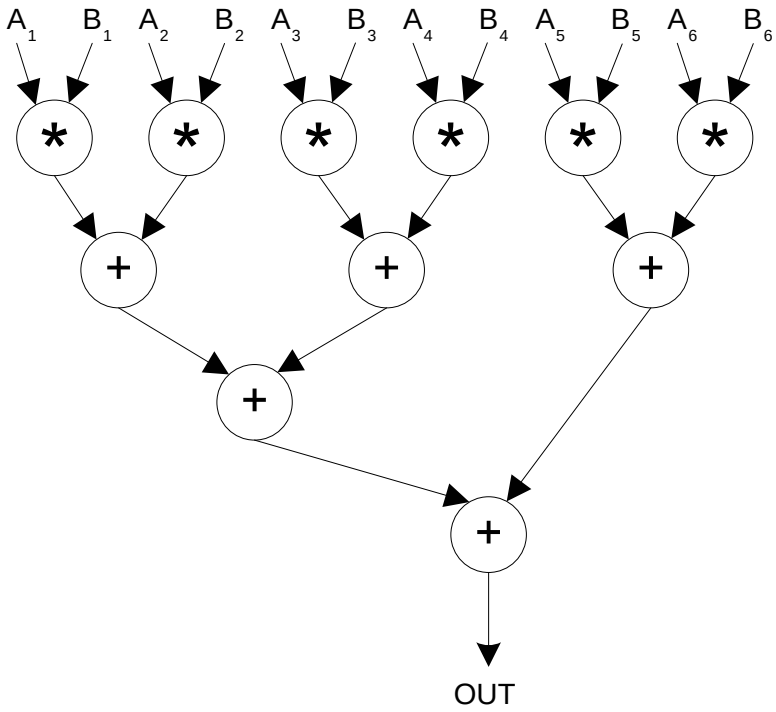
- Introduction
- Motivational example
- Proposed algorithm
- Experimental results
- Conclusions

Introduction

- Clock selection has a significant effect on the design in terms of:
  - performance
  - area
  - power
- Raghunathan and Jha developed a behavioural system that includes supply voltage and clock period pruning techniques to eliminate inferior design points during the search for the minimum power solution [11].

Motivational example

- Benchmark: Dot product of two vectors in cartesian form



Motivational example

- Library

	MULTIPLIER		**ADDER**		**REGISTER**	
***V* (V)**	***P* (mW)**	***D* (ns)**	***P* (mW)**	***D* (ns)**	***P* (mW)**	***D* (ns)**
1.08	**1.237**	**11.048**	**0.040**	**4.292**	**0.047**	**0.547**
1.2	**1.870**	**7.143**	**0.049**	**2.861**	**0.055**	**0.344**
1.32	**2.556**	**4.650**	**0.066**	**1.976**	**0.077**	**0.233**
***A* (μm)**	**10660.9**		**1107.4**		**548.7**	

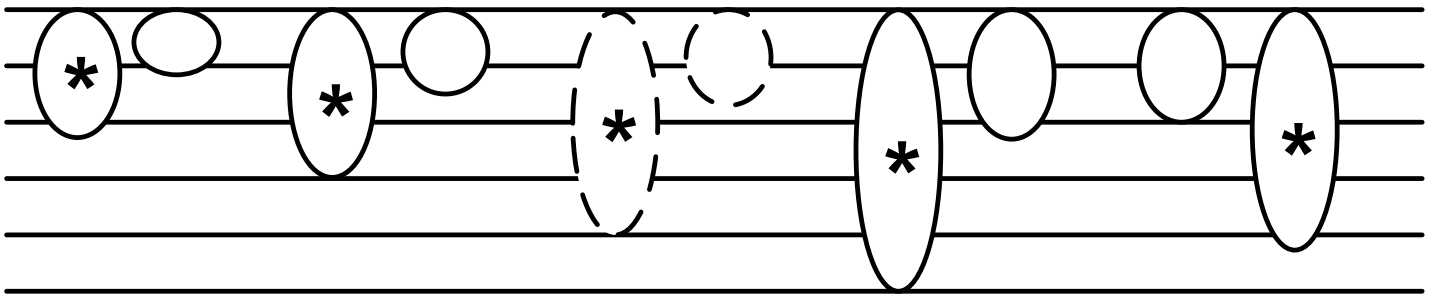
Motivational example

- Possible solutions

sol.	*Ls* (cs)	*Tclk* (ns)	TP_m (cs)	TP_a (cs)	sk_{cp} (ns)	*V* (V)	*A* (μm)	*P* (mW)	*Ct* (s)
1	**9**	**5.2**	**3**	**1**	**21.6**	**1.13**	**81251**	**1.304**	**134**
2	**5**	**9.4**	**2**	**1**	**16.5**	**1.08**	**78971**	**1.063**	**3**
3	**8**	**5.9**	**1**	**1**	**32.4**	**1.29**	**20192**	**2.976**	**57**
4	**19**	**2.5**	**6**	**3**	**16.5**	**1.08**	**35478**	**1.929**	**34**

Proposed algorithm. Part 1

```
1 initialise_Ls ( );
2 determine_max_Ls
3 calculate_Tclk
4 while Ls < =  max_Ls do
5       calculate_throughput_bounds;
6       increase_Ls( );
7       calculate_Tclk( );
8 end while
```



Proposed algorithm. Part 1

- Structure of clock candidates list

Ls_1	clk_1	$TP_{ops\ 1}$	Sch_1	V_1	$P_{FUs}(V_1)$	$D_{FUs}(V_1)$	$P_R(V_1)$	$D_R(V_1)$
Ls_2	clk_2	$TP_{ops\ 2}$	Sch_2	V_2	$P_{FUs}(V_2)$	$D_{FUs}(V_2)$	$P_R(V_2)$	$D_R(V_2)$
Ls_3	clk_3	$TP_{ops\ 3}$	Sch_3	V_3	$P_{FUs}(V_3)$	$D_{FUs}(V_3)$	$P_R(V_3)$	$D_R(V_3)$
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
Ls_n	clk_n	$TP_{ops\ n}$	Sch_n	V_n	$P_{FUs}(V_n)$	$D_{FUs}(V_n)$	$P_R(V_n)$	$D_R(V_n)$

Proposed algorithm. Part 2

1 generate initial solutions for group of clock candidates
2 **while** system is not frozen **do**
3 **while** valid solutions < number of solutions to generate at this control parameter **do**
4 choose one operation randomly
5 generate a new solution applying one of the following moves:
6 1) schedule selected operation into a new control step
7 2) bind the selected operation result to a new register
8 3) bind selected operation to a new functional module
9 4) swap the module inputs of selected operation
10 5) clock and operations throughput selection
11 evaluate the cost of the new solution
12 accept or reject the new solution
13 **end while**
14 decrease simulated annealing control parameter
15 **end while**

Proposed algorithm. Part 2

- Optimisation cost function

$$\cos t = \sqrt{\left(W_P - \frac{P_i}{P_0}\right)^2 + \left(W_Q - \frac{Q_i}{Q_0}\right)^2}$$

- Power estimation

$$P_{DP} = P_{REG} + P_{MUX} + P_{FU}$$

$$P_{FU} = \frac{\sum_{\text{All FUs}} N_F P_F D_F}{T} \qquad P_{REG} = \frac{\sum_{\text{All registers}} N_R P_R D_R}{T} \qquad P_{MUX} = \frac{\sum_{\text{All multiplexers}} N_X P_X D_X}{T}$$

Proposed algorithm. Part 2

- Area estimation

$$Q = \sum_{All\ FUs\ used} Fa_F + Ra_R + Xa_X$$

Experimental results. Exp. 1

- Area, power and computational time savings

	savings for AR			**savings for EWF**			**savings for DCT**		
T	***%A***	***%P***	***%Ct***	***%A***	***%P***	***%Ct***	***%A***	***%P***	***%Ct***
1.5cp	**11.7**	**13.8**	**-9.7**	**1.4**	**20.9**	**81.7**	**26.2**	**14.2**	**81.8**
2cp	**50.2**	**5.2**	**26.6**	**26.2**	**-0.8**	**93.8**	**25.4**	**8.3**	**92.9**
2.5cp	**53.8**	**-0.2**	**9.7**	**15.5**	**4.8**	**96.9**	**26.3**	**11.2**	**96.0**
3cp	**47.3**	**0.0**	**-28.0**	**41.0**	**0.8**	**97.2**	**36.6**	**0.0**	**96.2**
3.5cp	**57.3**	**4.4**	**21.6**	**37.7**	**6.3**	**97.1**	**38.6**	**19.6**	**96.1**

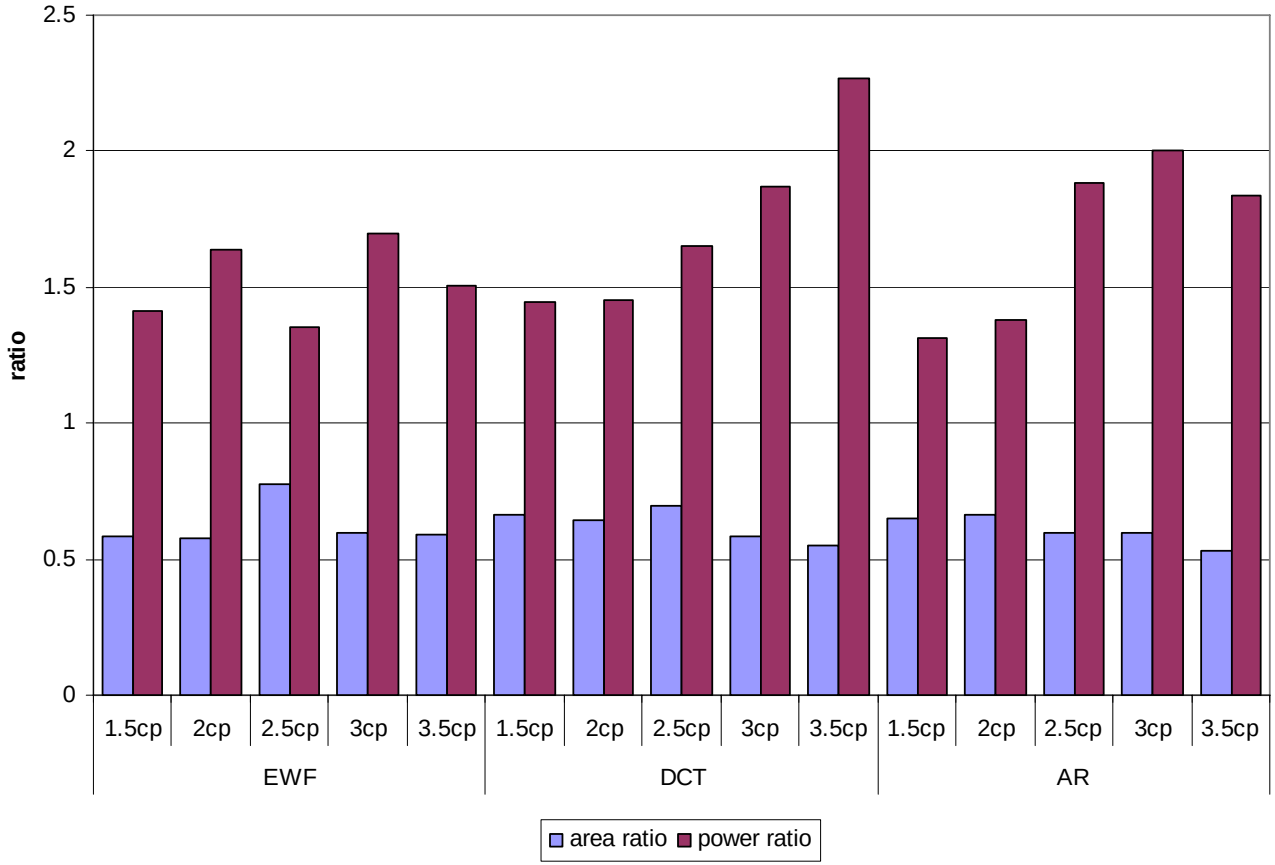
Experimental results. Exp. 1

- Minimum power solutions for DCT

	Base case					**Proposed approach**				
T	***Tclk*** **(ns)**	TP_m **(cs)**	Tp_a **(cs)**	***V*** **(V)**	***P*** **(mW)**	***Tclk*** **(ns)**	TP_m **(cs)**	Tp_a **(cs)**	***V*** **(V)**	***P*** **(mW)**
1.5cp	**3.2**	**3**	**1**	**1.30**	**9.828**	**4.0**	**3**	**1**	**1.23**	**8.435**
2cp	**3.6**	**3**	**1**	**1.20**	**5.603**	**4.0**	**3**	**1**	**1.15**	**5.136**
2.5cp	**3.6**	**3**	**1**	**1.13**	**3.613**	**4.0**	**3**	**1**	**1.08**	**3.208**
3cp	**3.6**	**3**	**1**	**1.08**	**2.539**	**3.6**	**3**	**1**	**1.08**	**2.539**
3.5cp	**1.5**	**5**	**2**	**1.08**	**2.652**	**4.6**	**2**	**1**	**1.08**	**2.133**

Experimental results. Exp. 2

- Power and area ratios for different tradeoffs



Experimental results. Exp. 2

- Power-area tradeoffs for EWF with 2cp

Tclk **(ns)**	***Ls*** **(cs)**	TP_m **(cs)**	Tp_a **(cs)**	*	+	***r***	***x***	***V*** **(V)**	***A*** **(μm)**	***P*** **(mW)**
2.5	**37**	**3**	**2**	**1**	**5**	**17**	**16**	**1.23**	**31109.5**	**1.855**
2.6	**35**	**3**	**2**	**2**	**3**	**12**	**12**	**1.21**	**36650.8**	**1.787**
4.6	**20**	**2**	**1**	**2**	**3**	**17**	**11**	**1.17**	**37393.1**	**1.619**
5.4	**17**	**2**	**1**	**3**	**3**	**13**	**12**	**1.13**	**46698.4**	**1.412**

Conclusions

- The proposed approach provide solutions not only optimised for low power or low area, but also facilitates the automatic exploration of power-area tradeoffs.
- Solutions have been obtained in less computational time and with lower power and area than a base case approach.
- Power reductions were due to the use of larger clock periods (lower frequencies), or a combination of lower voltages and lower frequencies obtained after an appropriate selection of clock period and operations throughput.

Contact

M. A. Ochoa-Montiel
Electronic Systems Design Group
School of Electronics and Computer Science
University of Southampton
United Kingdom

mao02r@ecs.soton.ac.uk