Numerical Function Generators Using Edge-Valued Binary Decision Diagrams

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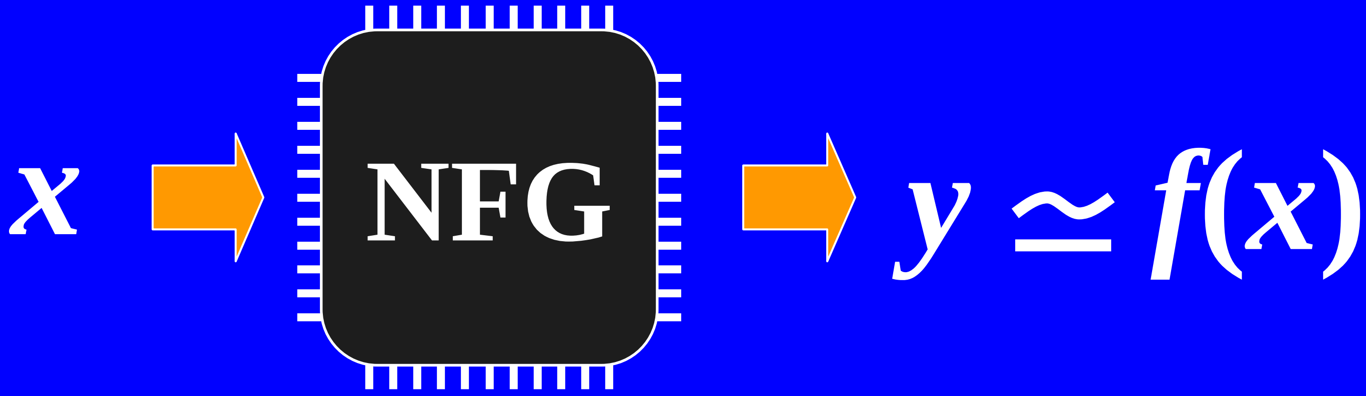
Numerical Function Generators (NFGs)



NFG computes an approximated value *y* for a numerical function *f*(*x*) for some given acceptable error.

e.g. elementary, compound functions

Background

- **Numerical functions** are extensively used in:
  - Digital signal processing
  - Communication systems
  - Robotics
  - Graphics applications
  - Astrophysics
  - Fluid physics
  - Etc.
- **Fast and compact** NFGs are required.

Research Objectives

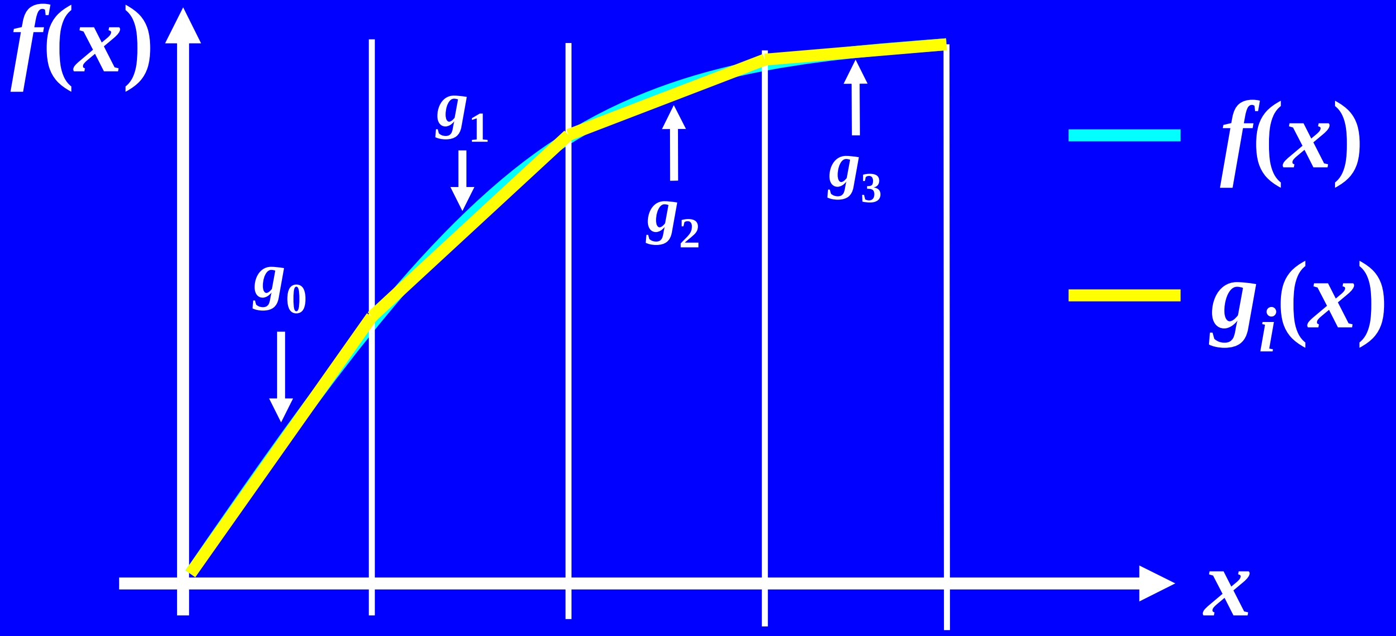
- We propose an architecture for **fast and compact NFGs**.
  - Realizes a piecewise polynomial approximation based on non-uniform segmentation.
  - Uses a **fast and compact segment index encoder (SIE).**
    - Realizes a **recursive segmentation.**
    - Uses an **EVBDD**.

  } Memory: 8%
  Delay: 47%

- We develop an **automatic synthesis system** for NFGs.

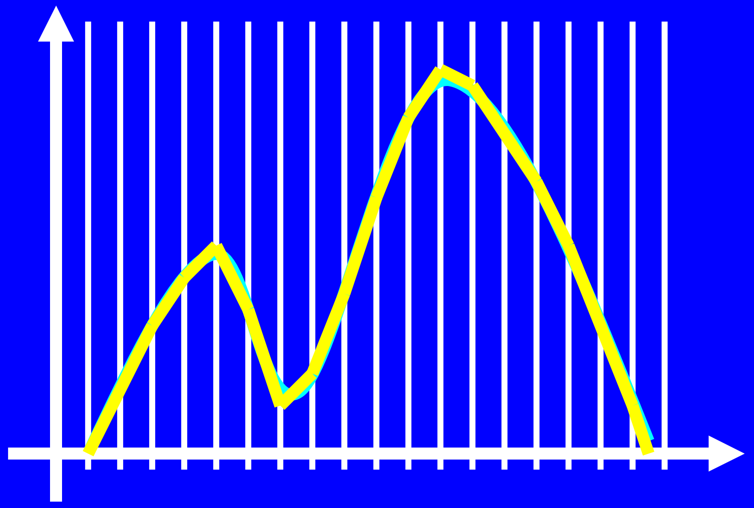
Piecewise Polynomial Approximation

- Partition the domain into segments.
- Approximate $f(x)$ by a polynomial function $g_i(x)$ for each segment.

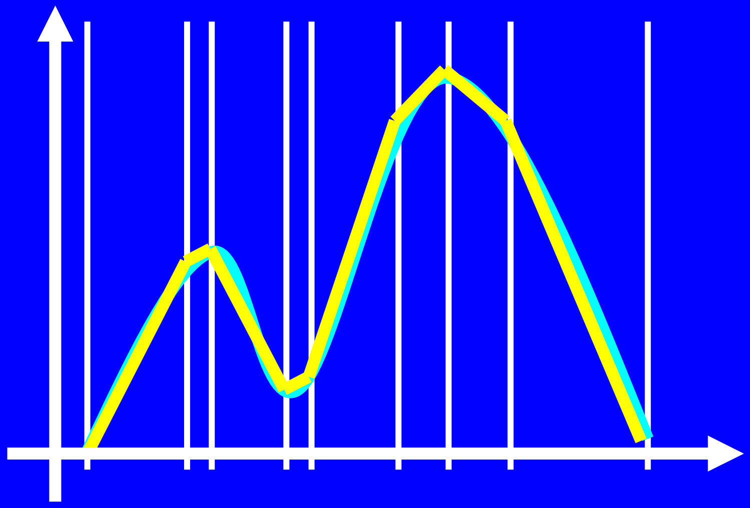


Non-uniform Segmentation

- **Approximates the function with fewer segments than uniform segmentation.**

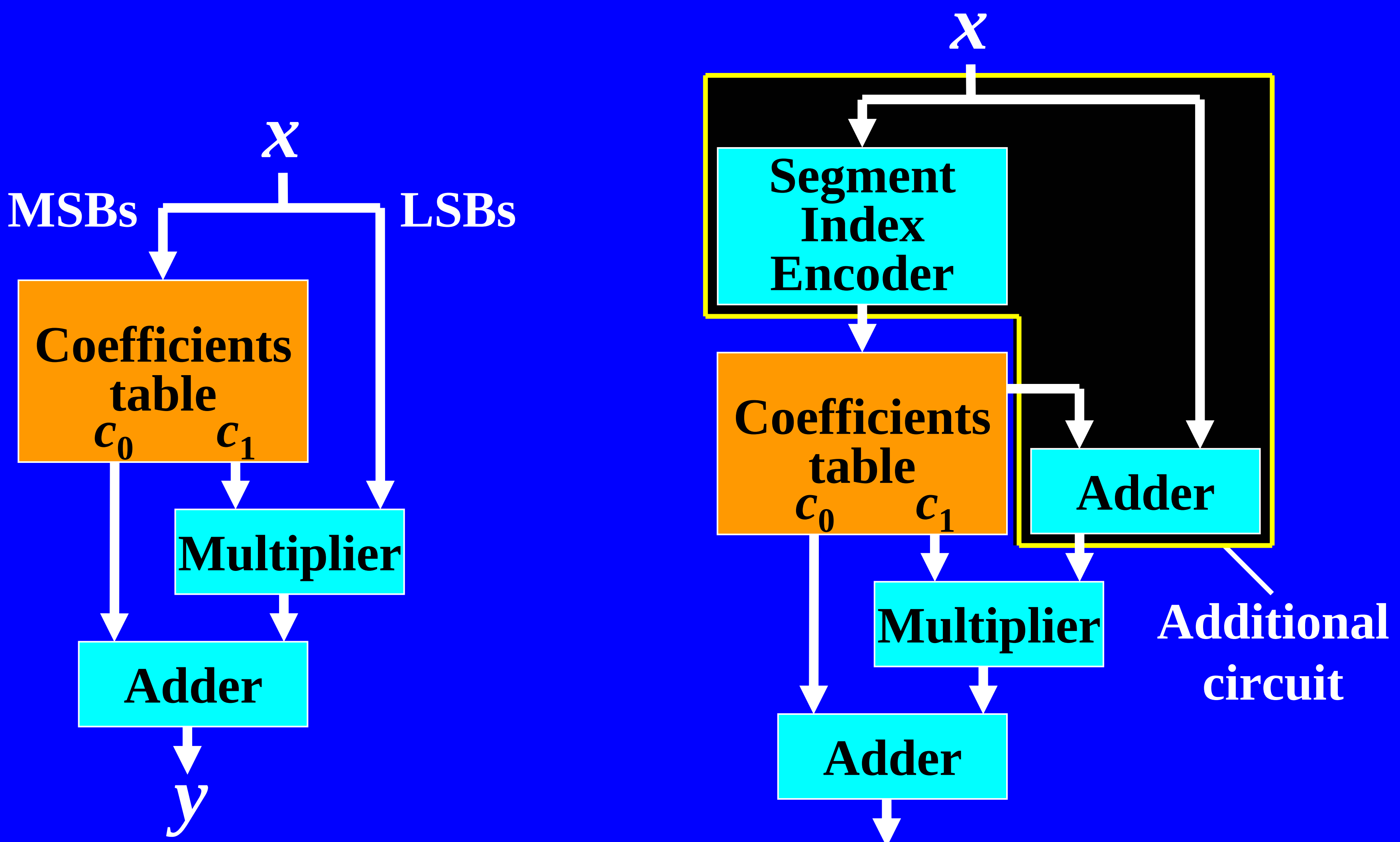


Uniform segmentation



Non-uniform segmentation

Two Architectures for NFG



Uniform segmentation

Non-uniform segmentation

Uniform and Non-uniform Segmentations

Segmentation method	Coefficients table (No. of segments)	Segment Index Encoder (SIE)
Uniform	Large	Not necessary
Non-uniform	Small	Necessary

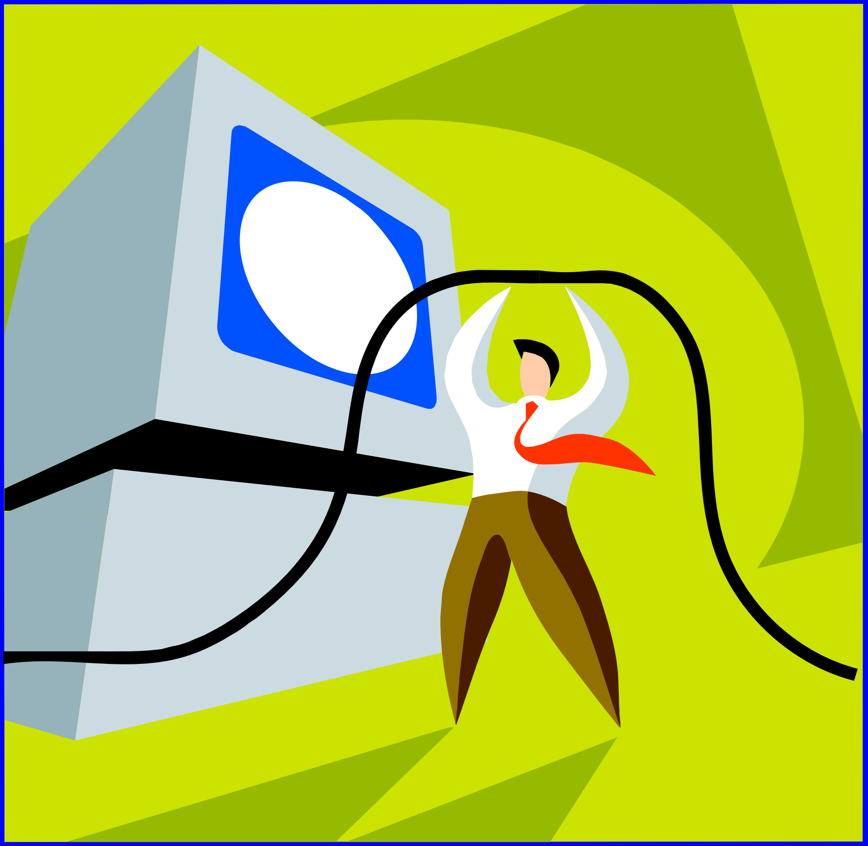
Simplifying the SIE is important.

Two Approaches to Simplify SIE

1. Segmentation approach
    - Uses a restricted segmentation to simplify the SIE.
    - Uniform segmentation is one of segmentation approaches.
    - We use a recursive segmentation.

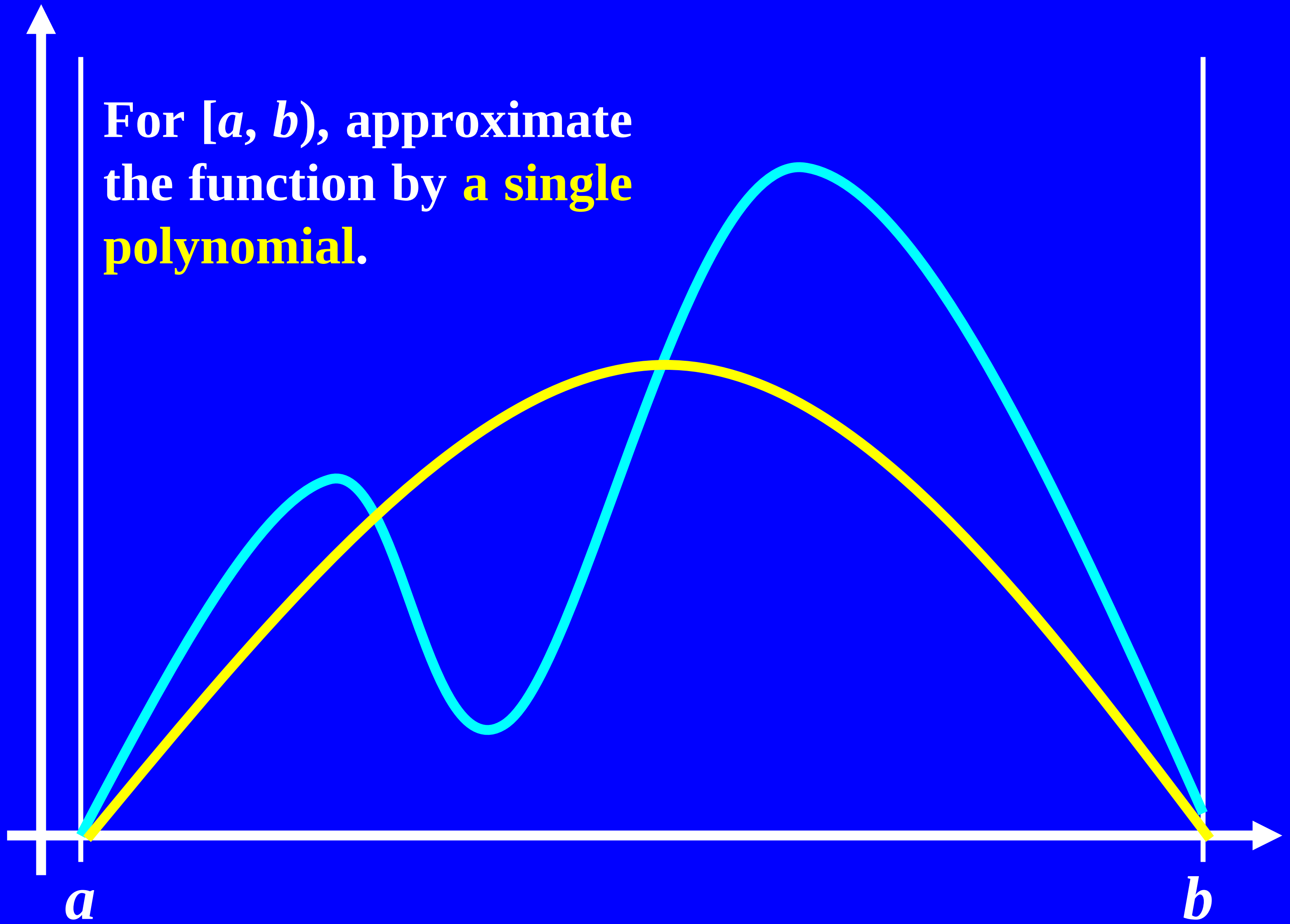
2. Realization approach
    - Realizes any segmentation compactly using a special architecture.
    - LUT cascade has been proposed.
    - We use a realization method using an EVBDD.

1. Segmentation Approach (Recursive Segmentation)

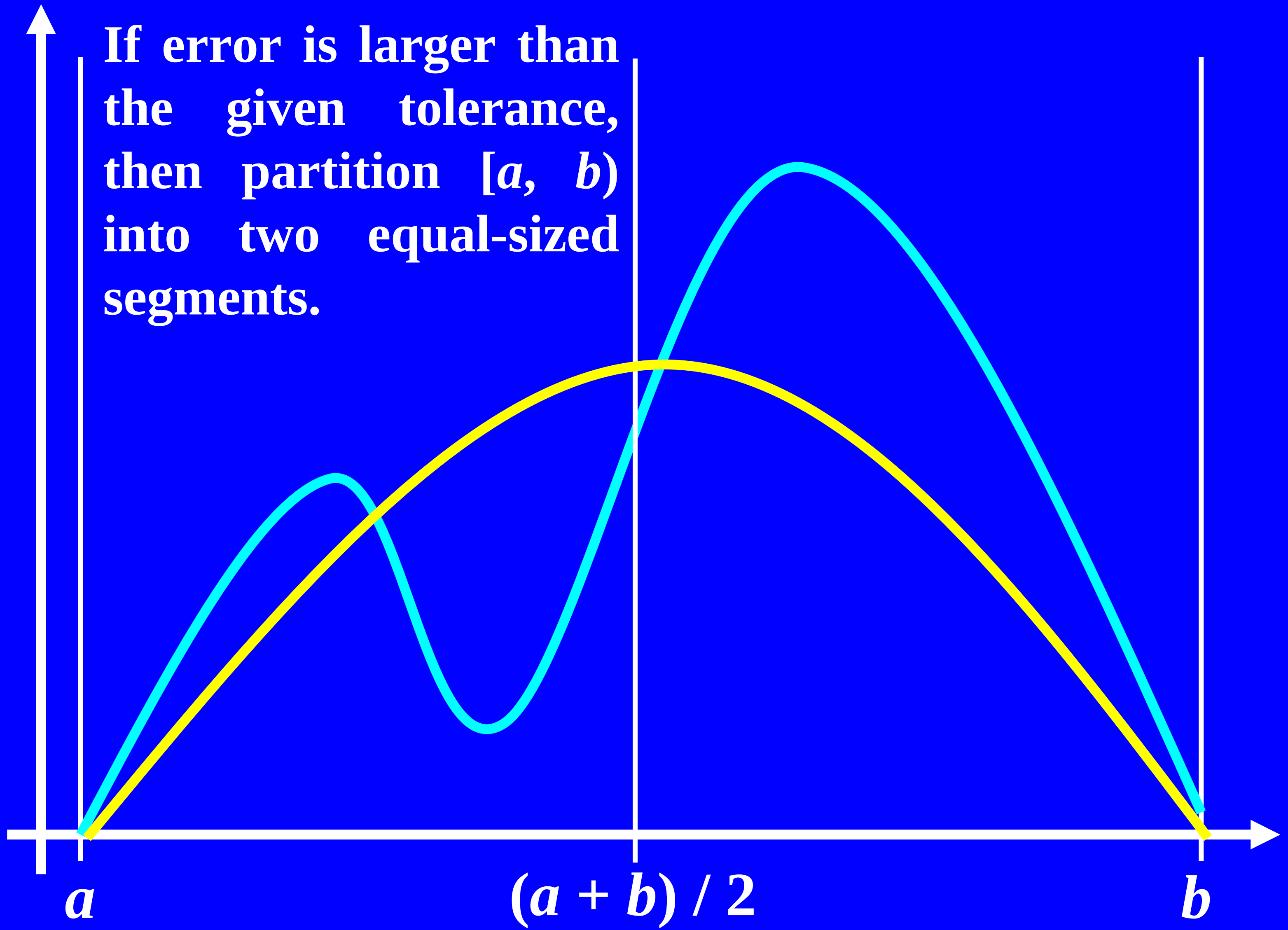


- Generates segmentation appropriate to the given function automatically.
  - No. of segments is small.
- Reduces memory size and delay time of the SIE.

Recursive Segmentation Algorithm

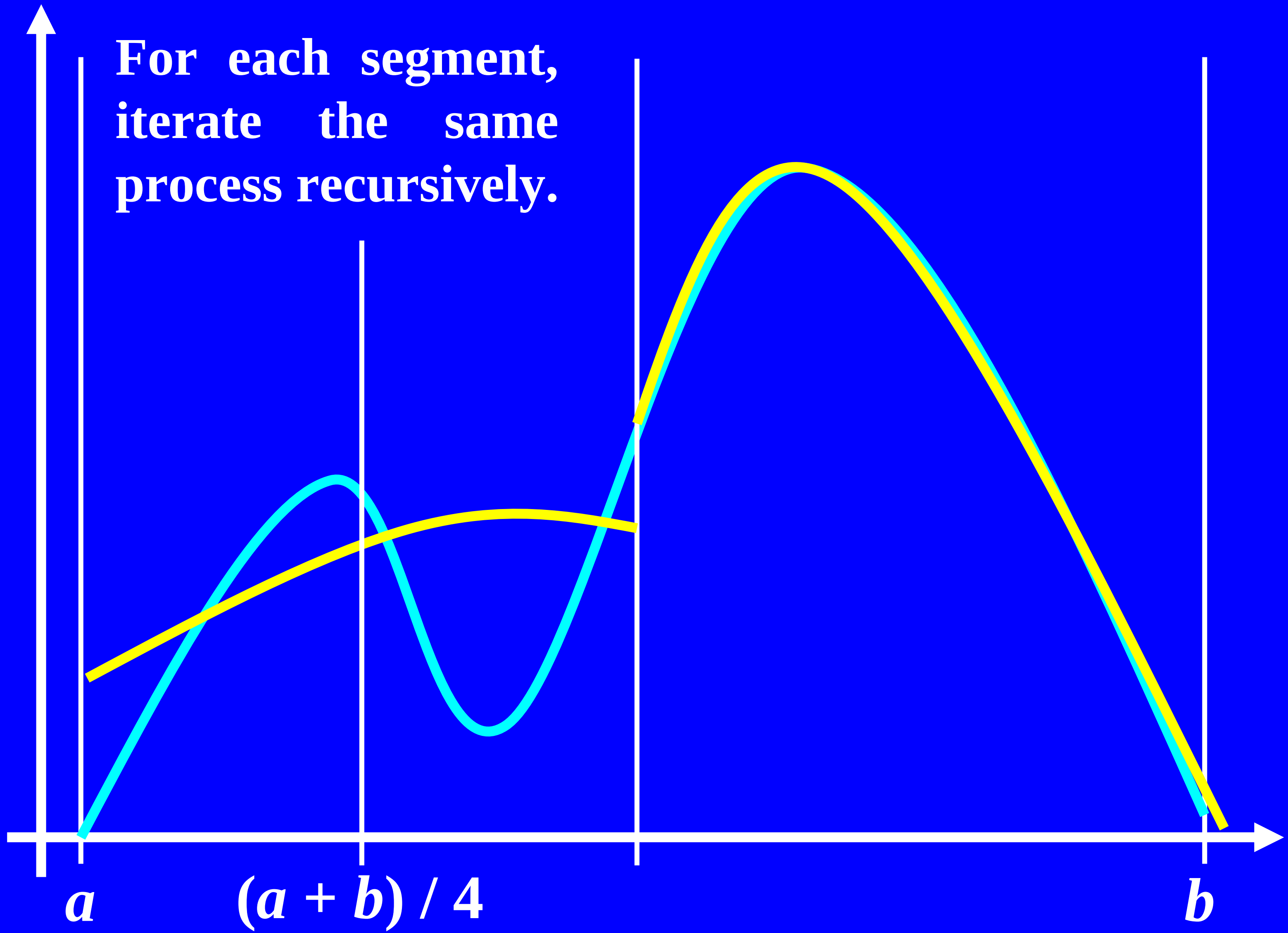


Recursive Segmentation Algorithm

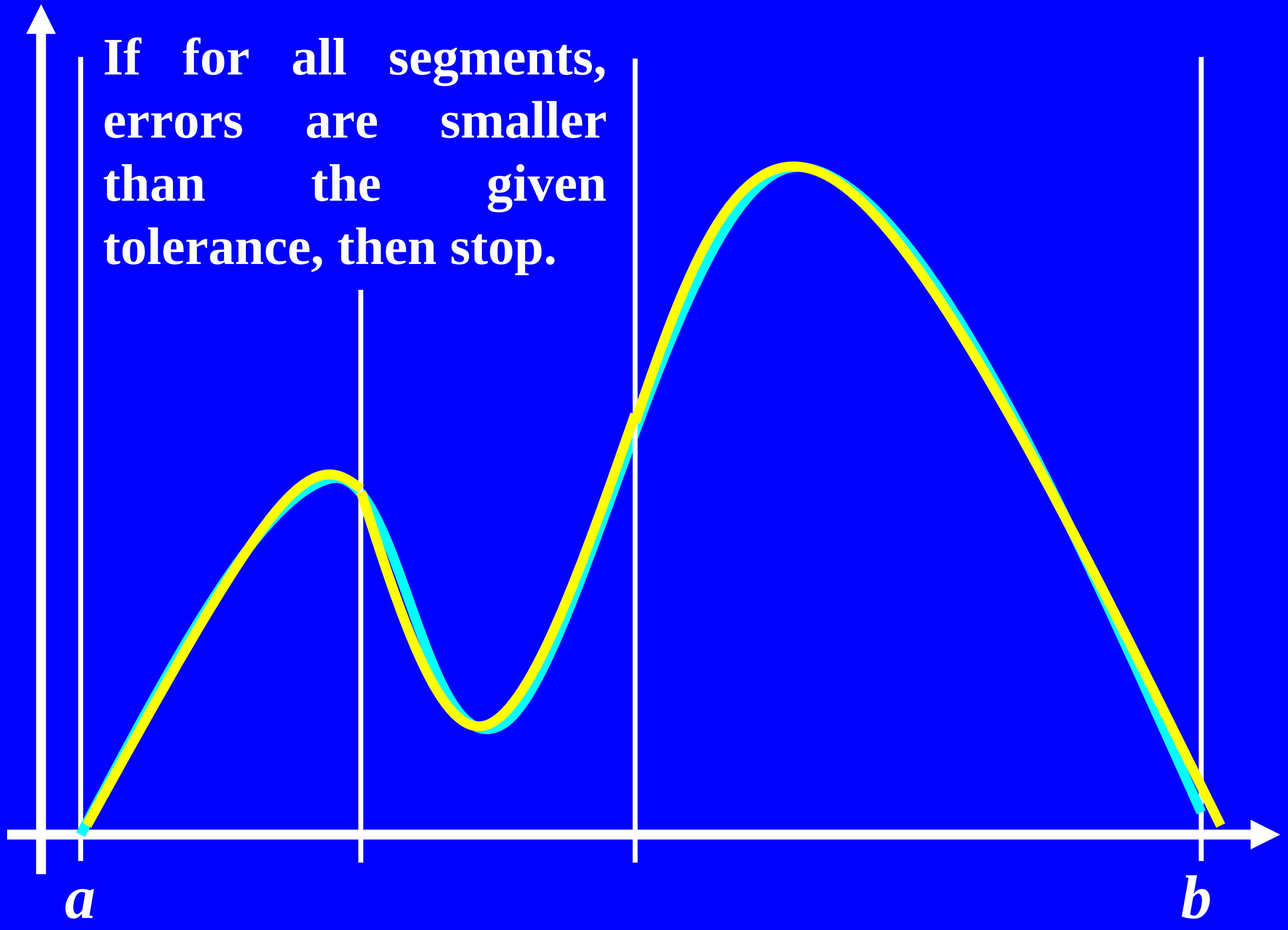


Recursive Segmentation Algorithm

For each segment, iterate the same process recursively.



Recursive Segmentation Algorithm



Number of Segments for Various Segmentation Methods.

Function $f(x)$	Domain [a, b)	Uniform	Non-uniform	Recursive
$\sin(\pi x)$	[0, 0.5)	128	74	128
$\tan(\pi x)$	[0, 0.5)	4,194,304	4,594	8,192
$\mathrm{asin}(x)$	[0, 1)	8,388,608	256	512
$\sqrt{x}$	(0, 1)	8,388,607	228	512
$\sqrt{-\ln(x)}$	(0, 1)	8,388,607	698	1,024
$x \ln(x)$	(0, 1)	2,097,152	172	256

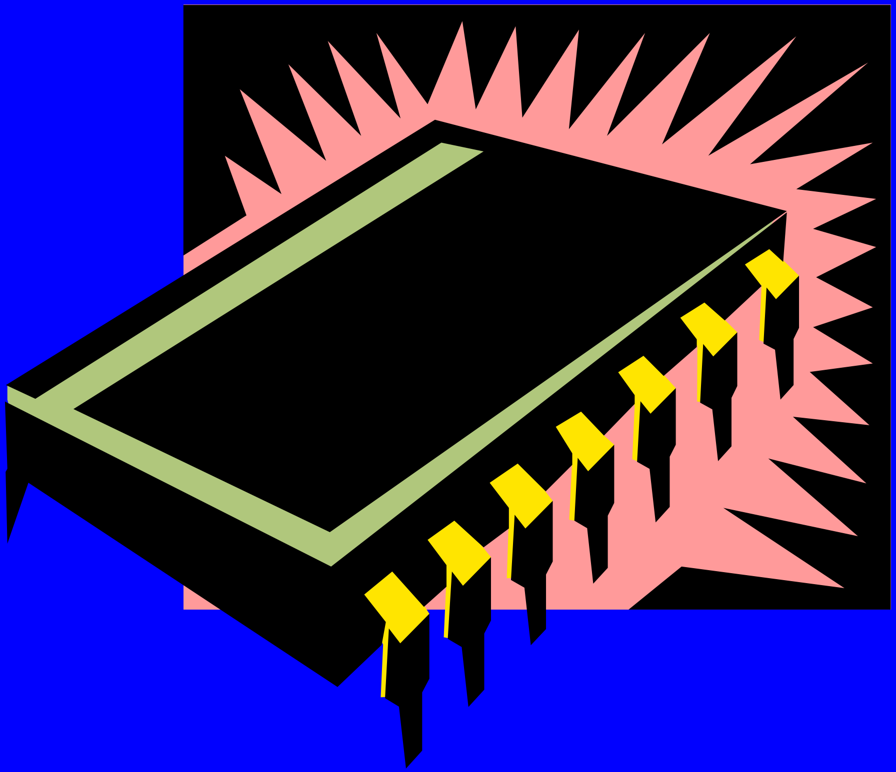
Acceptable approximation error: 2^{-25}

Sizes and Delay Times of SIEs (LUT cascades)

Function $f(x)$	Non-uniform		Recursive	
	Size [bits]	Delay [nsec.]	Size [bits]	Delay [nsec.]
$\sin(\pi x)$	26,880	27.5	0	0
$\tan(\pi x)$	1,802,240	--	1,687,552	--
$\mathrm{asin}(x)$	61,440	27.5	49,152	24.3
$\sqrt{x}$	61,440	27.5	44,544	24.1
$\sqrt{-\ln(x)}$	266,240	33.2	172,032	28.1
$x\ln(x)$	61,440	27.5	20,992	17.2

FPGA device: Altera Stratix (EP1S10F484C5)
-- Insufficient memory blocks in the FPGA.

2. Realization Approach (Realization Method Using EVBDD)



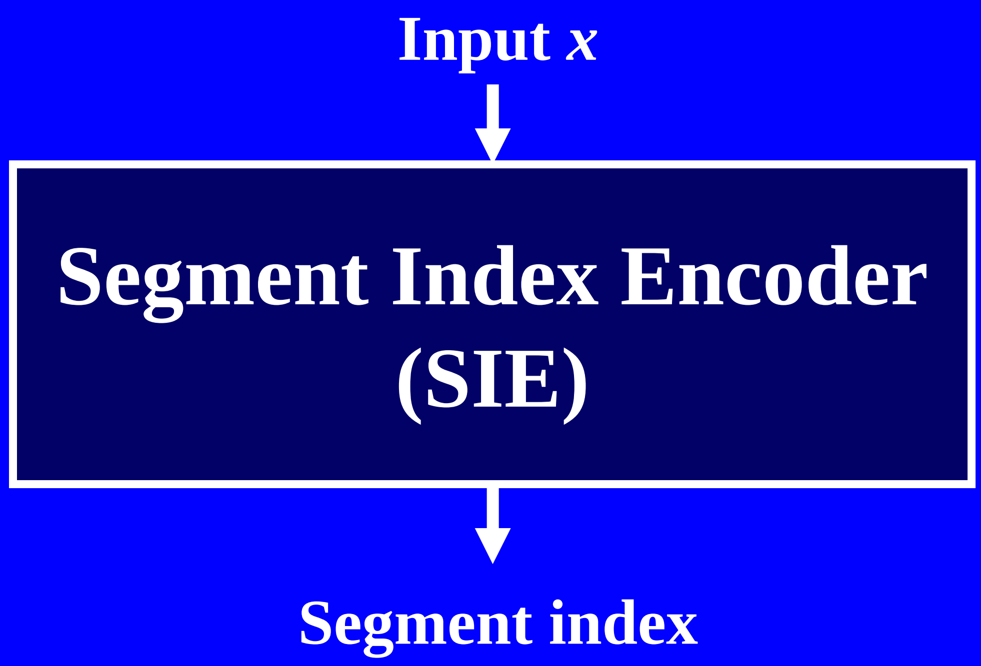
- Can realize arbitrary segmentation.
- Reduces memory size required for the SIE.

Segment Index Encoder (SIE)

Interval	Index
$a \leq x < p_0$	0
$p_0 \leq x < p_1$	1
$p_1 \leq x < p_2$	2
⋮	⋮
$p_{t-2} \leq x < b$	t - 1

Segment index function

- It converts input x into a segment index.
- It realizes a segment index function.

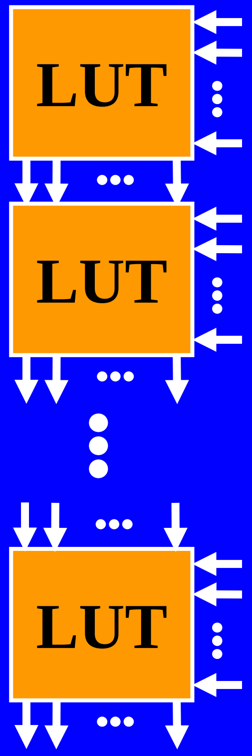


Realization of Segment Index Function

Interval	Index
$a \le x < p_0$	0
$p_0 \le x < p_1$	1
$p_1 \le x < p_2$	2
⋮	⋮
$p_{t-2} \le x < b$	t - 1

Segment index function

→ MTBDD →



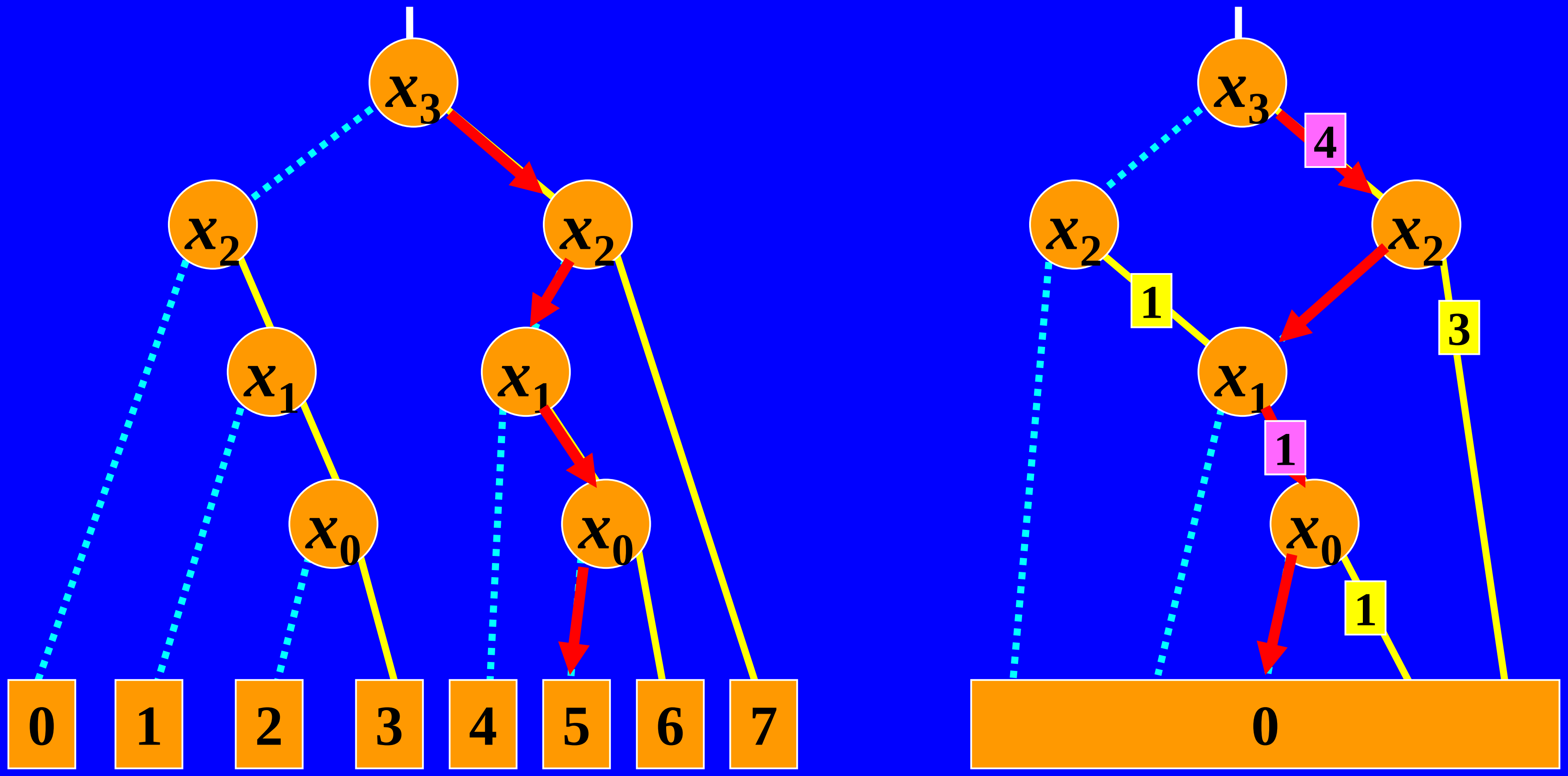
LUT cascade

↓

EVBDD → LUT cascade and adders

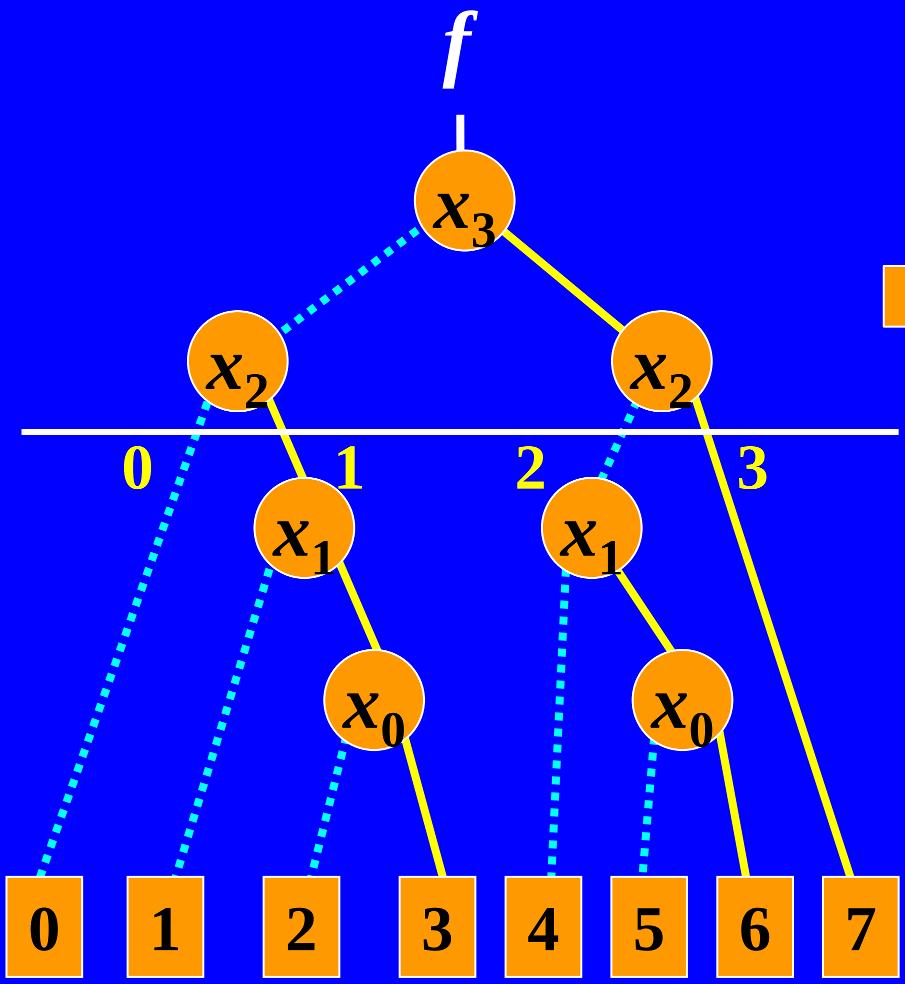
MTBDD and EVBDD

$f(1010) = 5$ $f(1010) = 5$

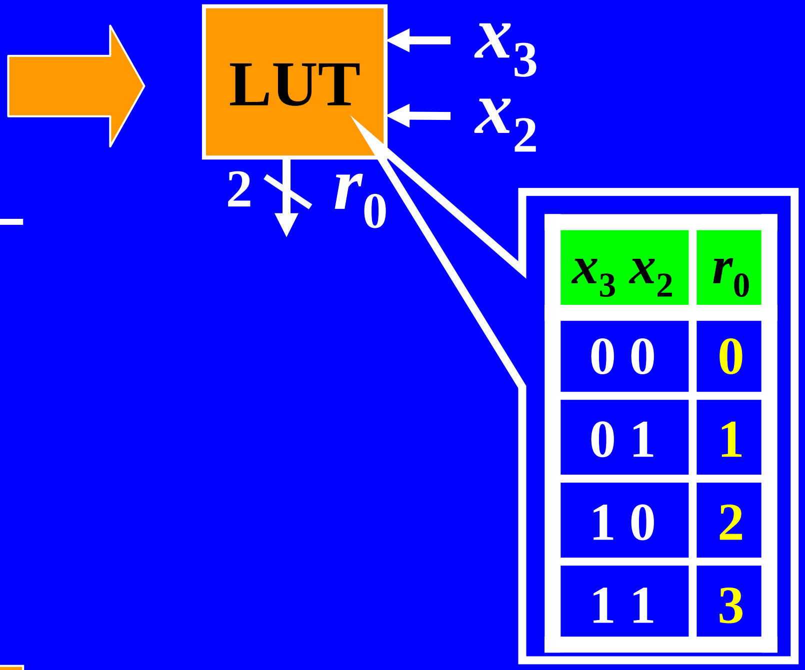


MTBDD EVBDD

SIE Using MTBDD



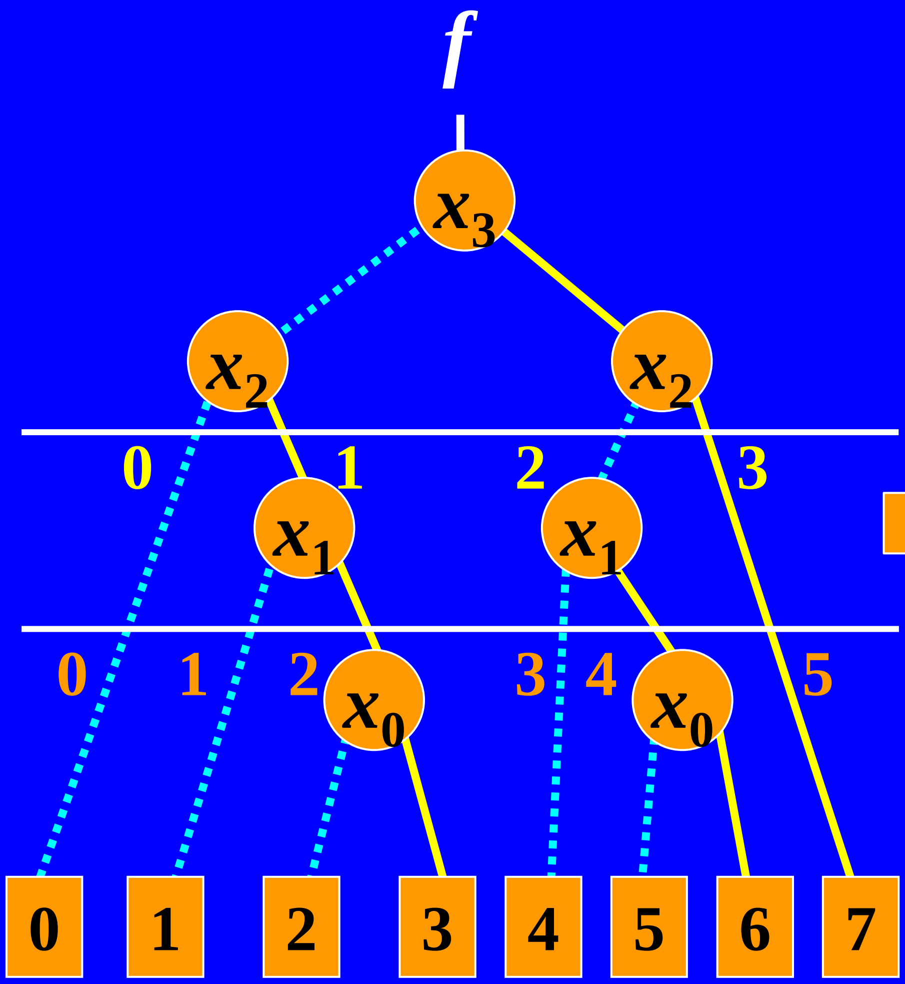
MTBDD



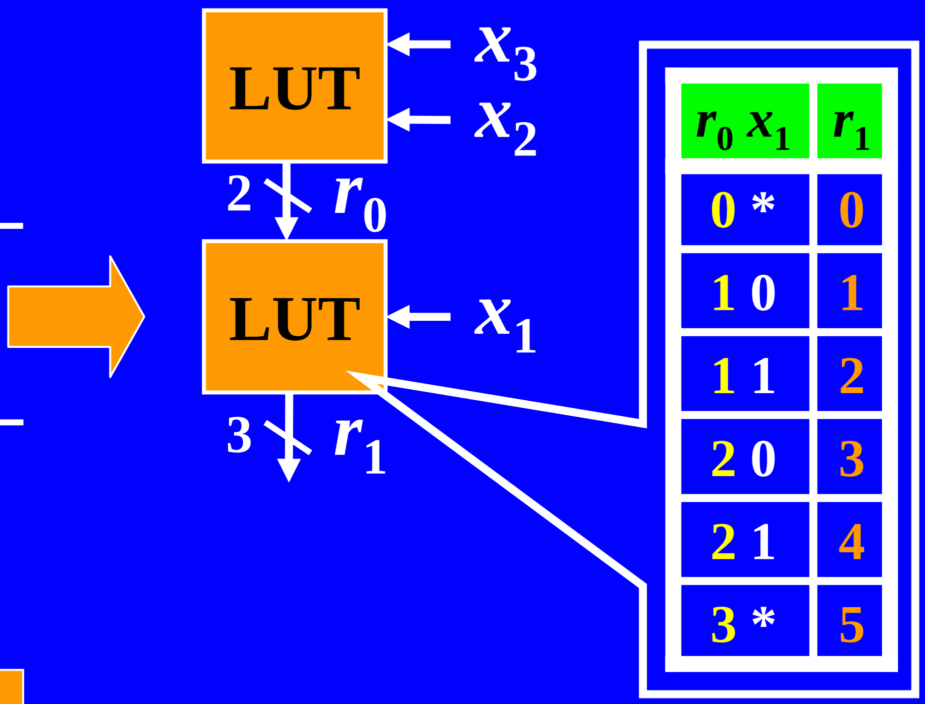
x_3 x_2	r_0
0 0	0
0 1	1
1 0	2
1 1	3

LUT cascade

SIE Using MTBDD



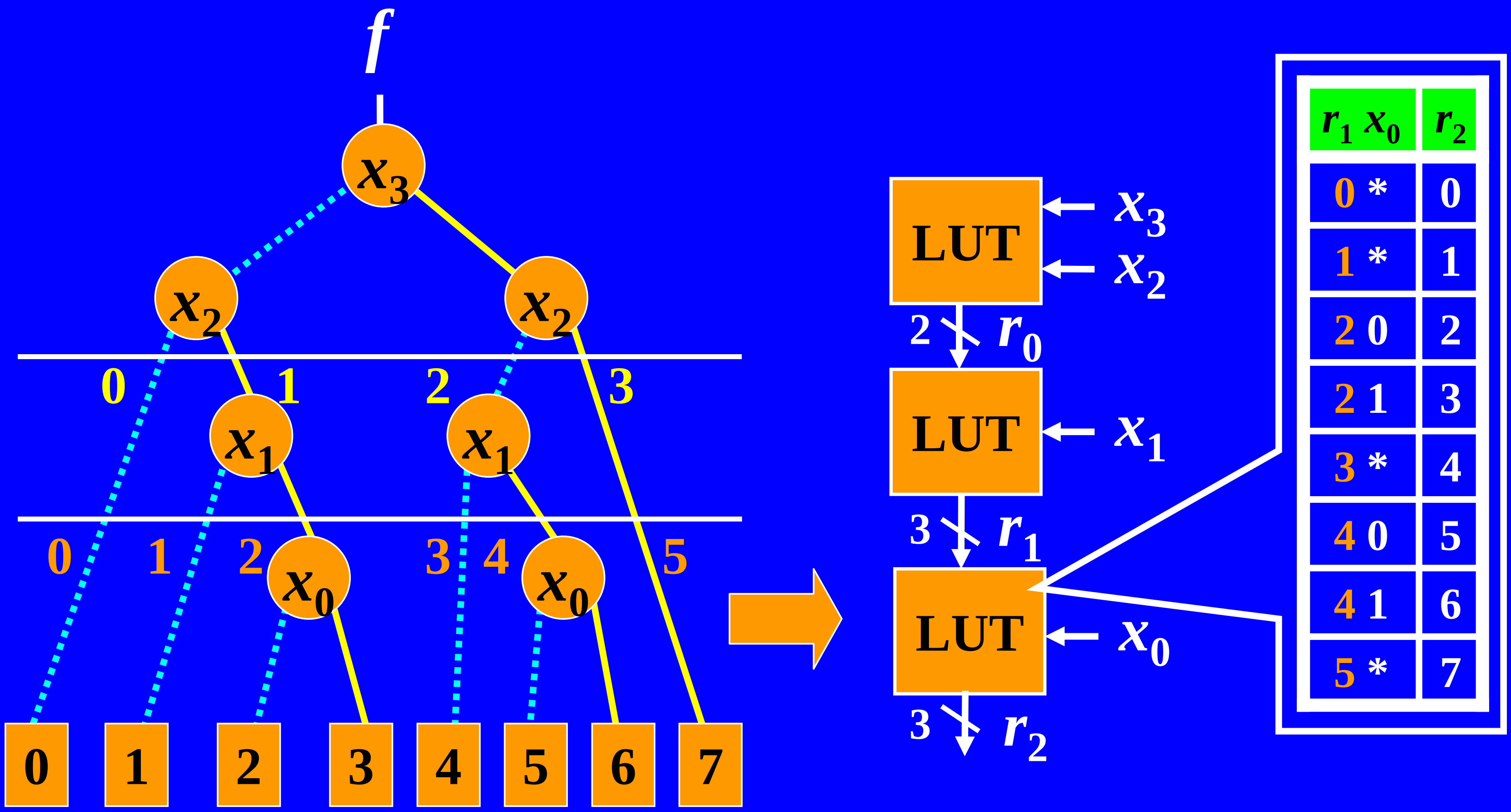
MTBDD



r_0 x_1	r_1
0 *	0
1 0	1
1 1	2
2 0	3
2 1	4
3 *	5

LUT cascade

SIE Using MTBDD

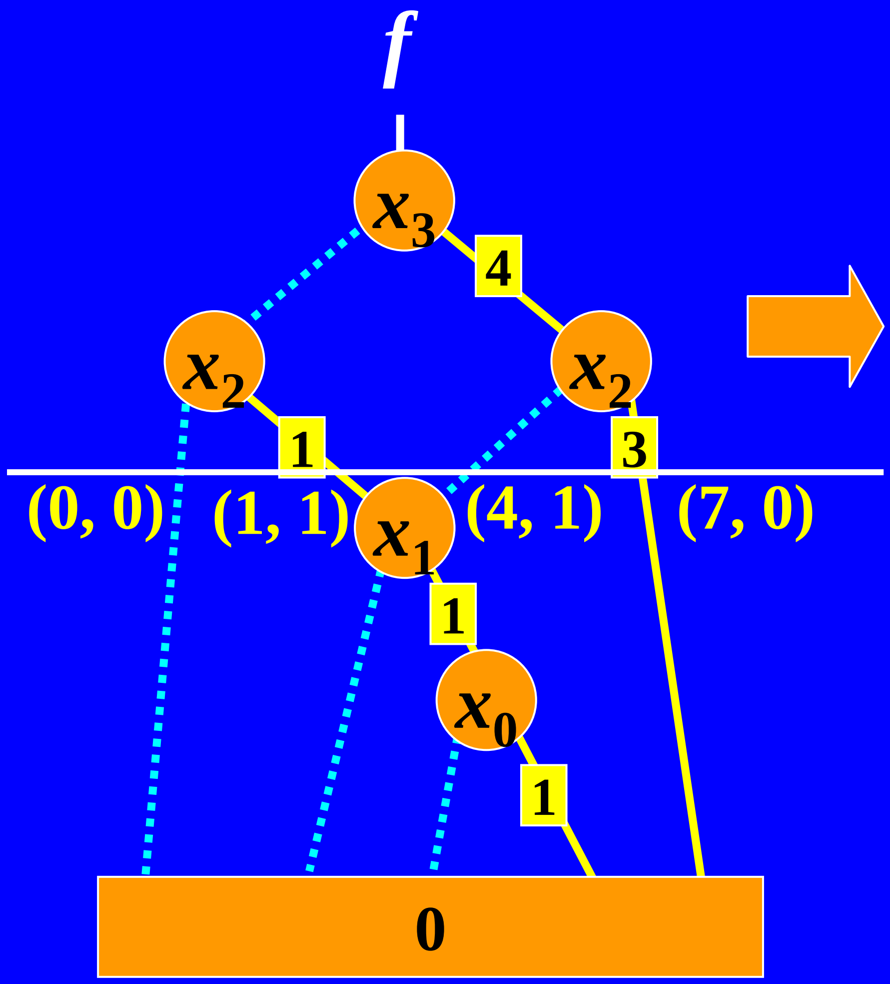


r_1 x_0	r_2
0 *	0
1 *	1
2 0	2
2 1	3
3 *	4
4 0	5
4 1	6
5 *	7

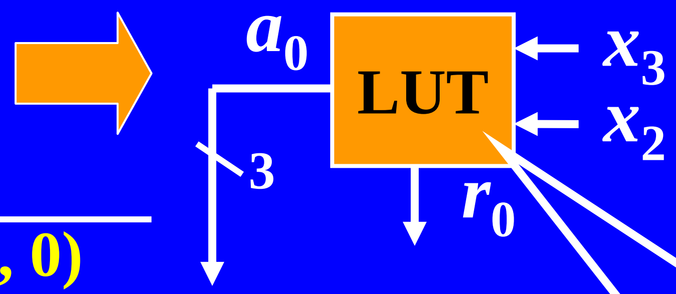
MTBDD

LUT cascade

SIE Using EVBDD



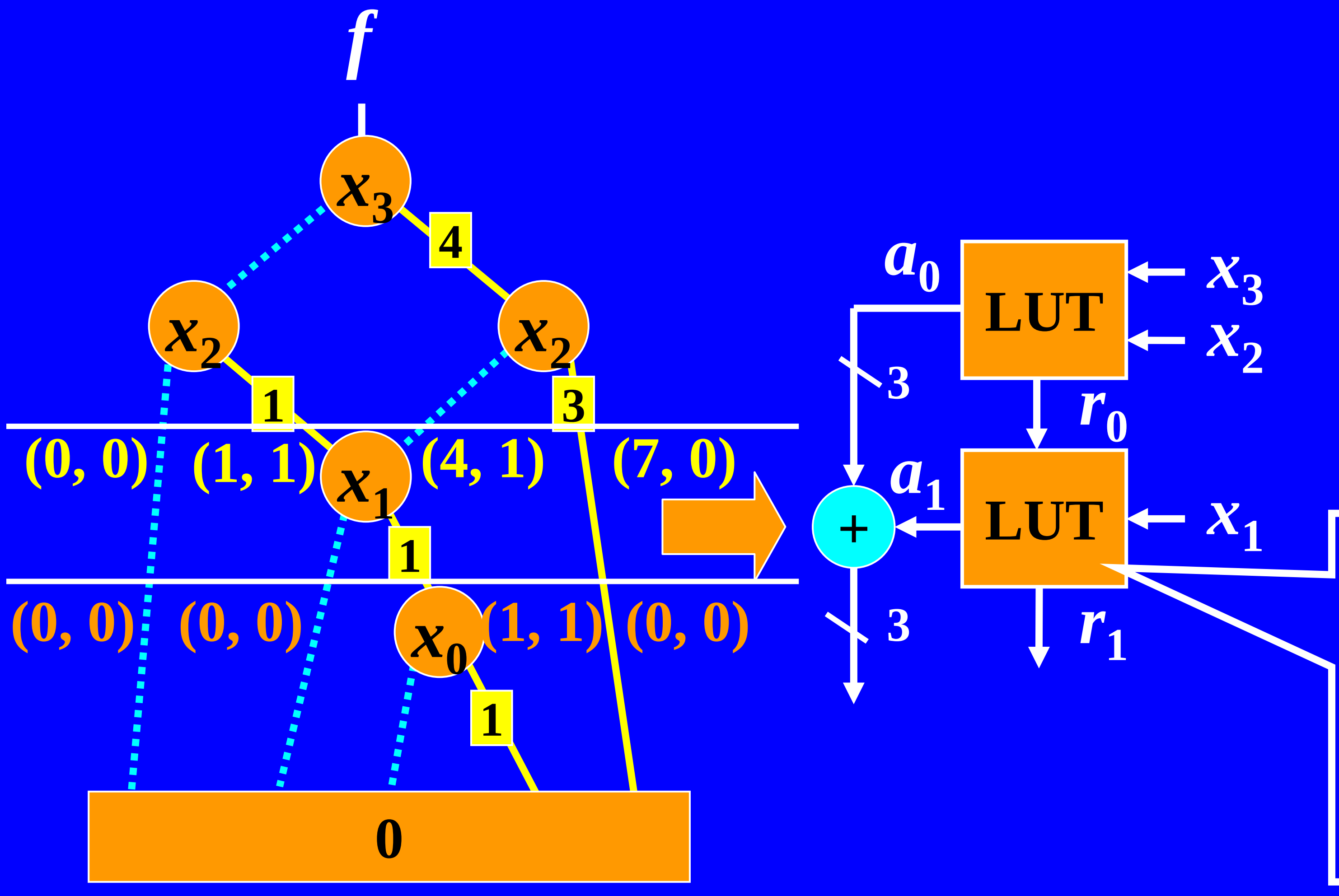
EVBDD



x_3 x_2	a_0	r_0
0 0	0	0
0 1	1	1
1 0	4	1
1 1	7	0

SIE

SIE Using EVBDD

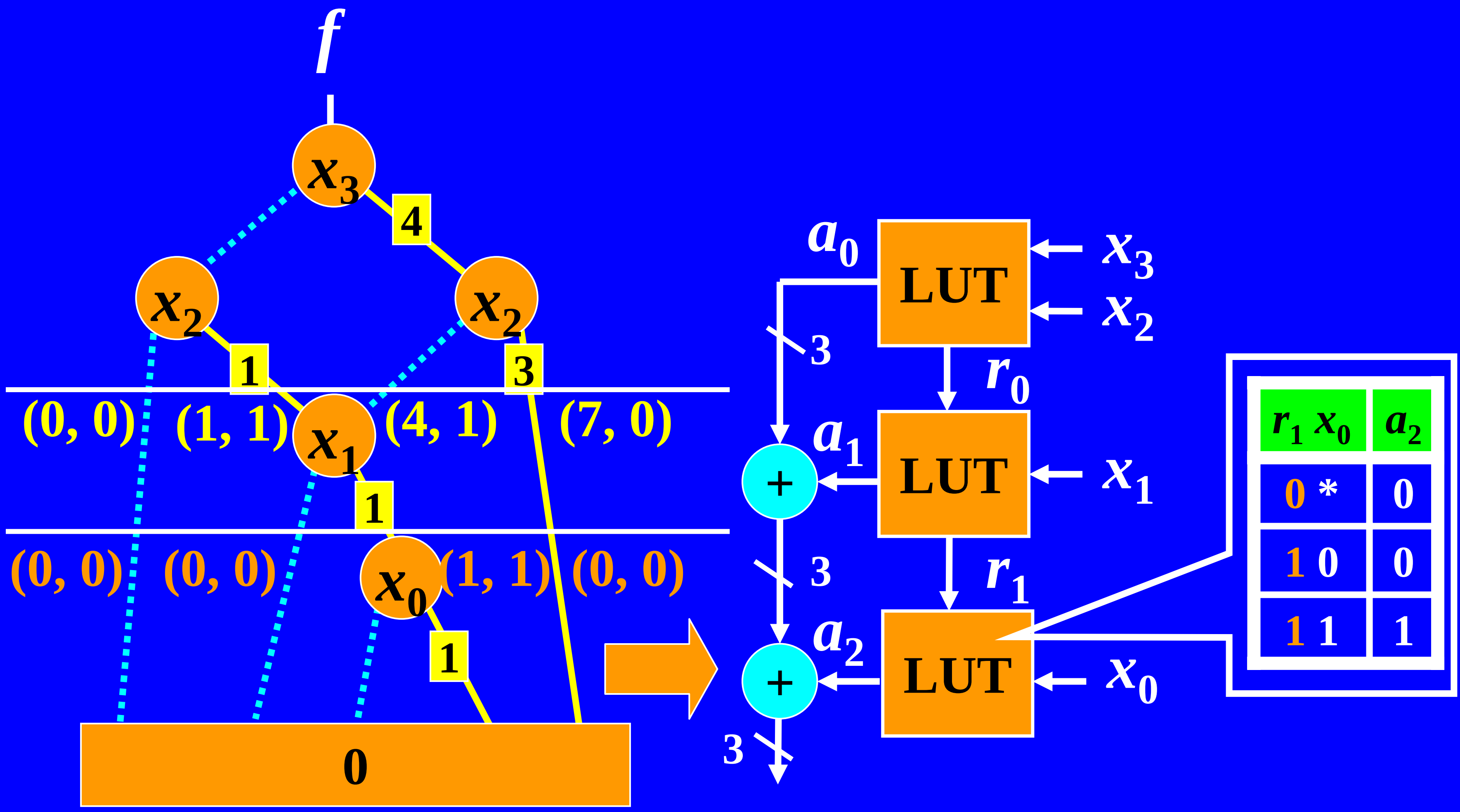


r_0 x_1	a_1	r_1
0 *	0	0
1 0	0	0
1 1	1	1

EVBDD

SIE

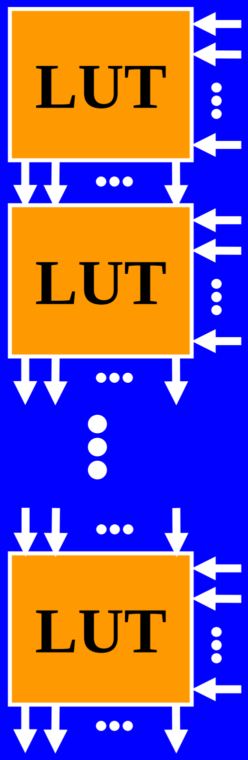
SIE Using EVBDD

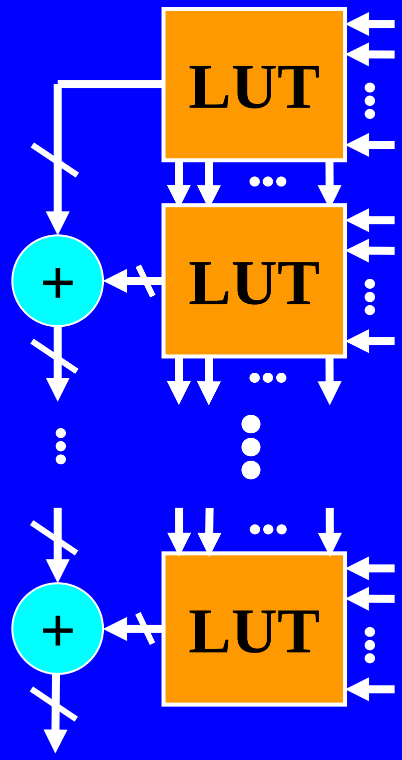


EVBDD

SIE

Two types of SIEs





SIE using MTBDD
MT_SIE
(Memory only)

SIE using EVBDD
EV_SIE
(Memory and adders)

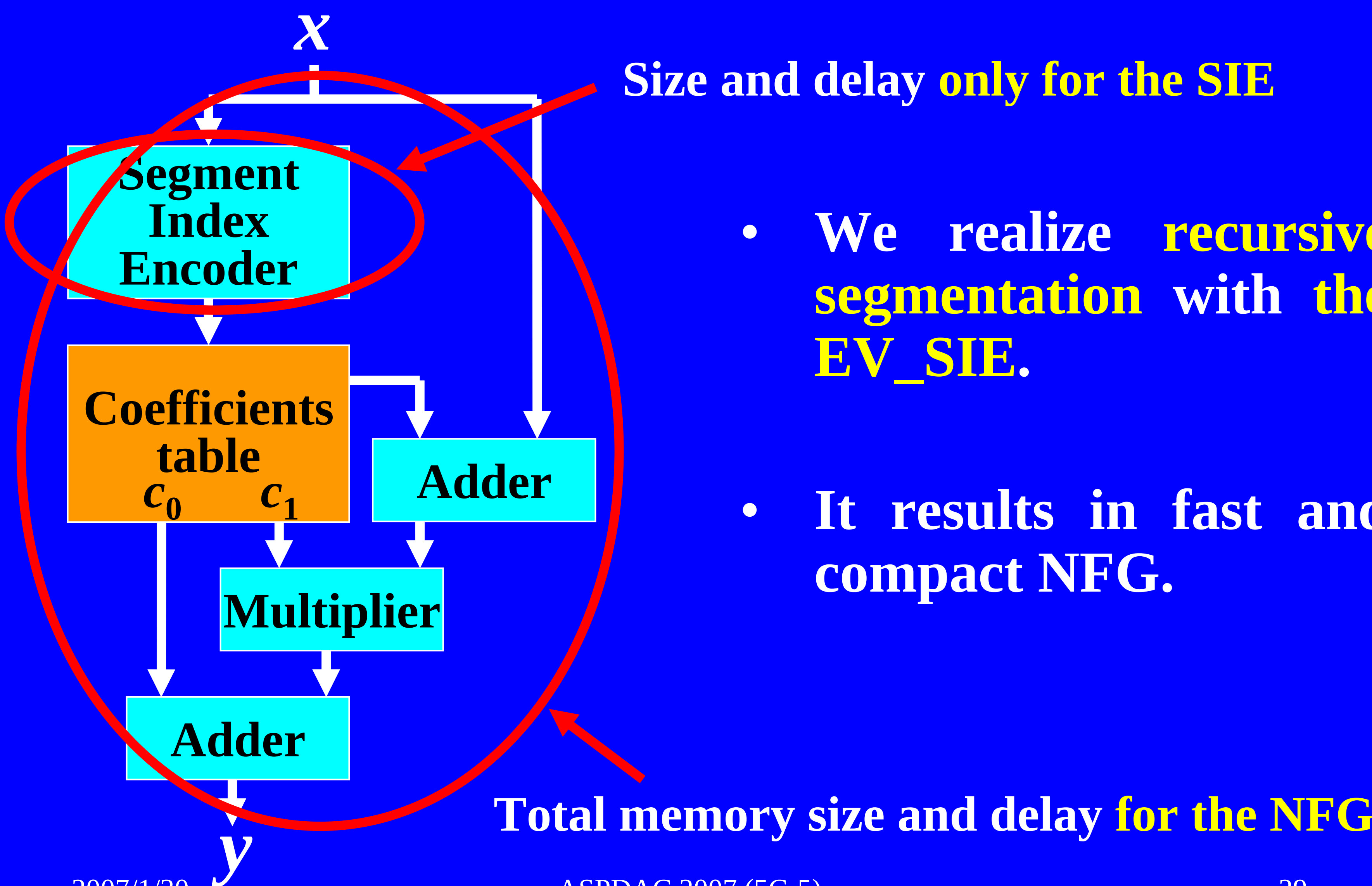
Sizes and Delay Times of SIEs for Non-uniform Segmentation

Function $f(x)$	MT_SIE		EV_SIE	
	Size [bits]	Delay [nsec.]	Size [bits]	Delay [nsec.]
$\sin(\pi x)$	26,880	27.5	23,552	24.1
$\tan(\pi x)$	1,802,240	--	179,968	36.3
$\mathrm{asin}(x)$	61,440	27.5	53,824	44.7
$\sqrt{x}$	61,440	27.5	57,408	40.3
$\sqrt{-\ln(x)}$	266,240	33.2	116,160	40.2
$x \ln(x)$	61,440	27.5	48,384	30.9

FPGA device: Altera Stratix (EP1S10F484C5)

-- Insufficient memory blocks in the FPGA.

3. SIE Using Both Approaches



- We realize recursive segmentation with the EV_SIE.
- It results in fast and compact NFG.

Sizes and Delay Times of SIEs

Function $f(x)$	MT_SIE (Non-uniform)		EV_SIE (Recursive)	
	Size [bits]	Delay [nsec.]	Size [bits]	Delay [nsec.]
$\sin(\pi x)$	26,880	27.5	0	0
$\tan(\pi x)$	1,802,240	--	15,108	24.1
$\mathrm{asin}(x)$	61,440	27.5	9,984	17.2
$\sqrt{x}$	61,440	27.5	9,216	17.2
$\sqrt{-\ln(x)}$	266,240	33.2	12,736	20.6
$x \ln(x)$	61,440	27.5	6,912	13.8

FPGA device: Altera Stratix (EP1S10F484C5)

-- Insufficient memory blocks in the FPGA.

Total Memory Size for SIEs and Coefficients Table and Delay for NFGs*

Function $f(x)$	MTNFG (Non-uni)		EVNFG (Recursive)	
	Memory [bits]	Delay [nsec.]	Memory [bits]	Delay [nsec.]
$\sin(\pi x)$	36,864	99.1	7,936	28.3
$\tan(\pi x)$	2,867,200	--	973,572	92.3
$\mathrm{asin}(x)$	84,736	107.3	53,504	80.3
$\sqrt{x}$	83,712	116.5	52,224	85.5
$\sqrt{-\ln(x)}$	357,376	99.8	103,872	88.3
$x \ln(x)$	83,200	116.0	29,696	70.3

FPGA device: Altera Stratix (EP1S60F1020C5)

-- Insufficient memory blocks in the FPGA.

***23-bit precision**

Concluding Remarks

- We proposed architecture of NFG using an EVBDD.
  - Uses fast and compact SIE.
    - Realizes a recursive segmentation.
    - Uses an EVBDD.

    } Memory: 8%
    Delay: 47%
  - Efficiently implements the NFGs for a wide range of functions.
- Our automatic synthesis system
  - Produces faster and more compact NFGs than the existing NFGs.