
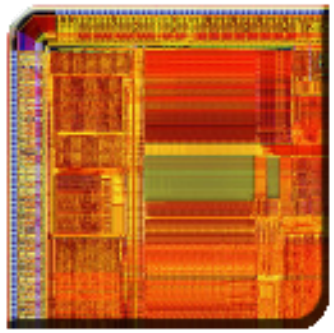


# An Efficient Computation of Statistically Critical Sequential Paths Under Retiming

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# Outline

- Motivation
- Related Work
- SRTA Algorithm
- Experimental Results
- Conclusion

# Motivation

- Process Variation
  - Varied transistor length, width, thickness
  - “Same” transistor, different gate delay

- Today in statistical timing analysis research
  - FFs are ignored (in most cases)
  - Retiming is still an useful/powerful method.

# Motivation

| **Timing Analysis** | Static Timing Analysis (STA) | Statistical Static Timing Analysis (SSTA) | Retiming-based Timing Analysis (RTA) | Statistical Retiming-based Timing Analysis (SRTA) **this work** |
|---|---|---|---|---|
|  | •Simple, Fast | •Handle process variation | •Faster Circuit | •Faster Circuit<br>•Handle process variation |
|  | •No retiming<br>•No statistical | •No retiming | •No statistical | |

# Main Contribution

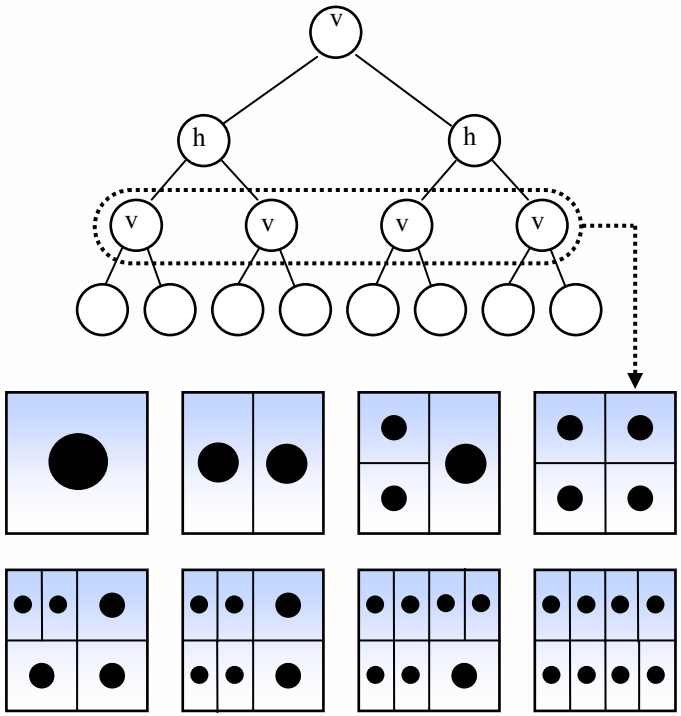
- In this research, we show
  - How to compute timing slack distribution of statistically critical paths under retiming.
  - This timing info helps select “correct” paths to focus on under process variation.
  - How to apply mincut based global placement the connected critical gates closer together

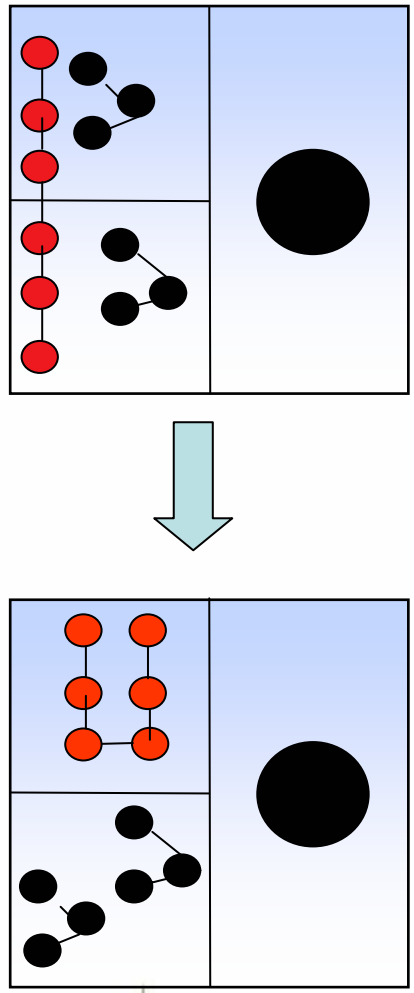
# Related Work I

- Retiming-based Timing Analysis (RTA)
  - Cong and Lim [ICCAD00]
  - Combines timing analysis and retiming
    - computes timing slack after retiming
  - Identifies critical paths assuming retiming will follow
    - Focusing on these paths provides better performance-driven placement results

# GEO Overview [Cong and Lim, ICCAD00]

- Mincut-based global placer
- RTA is used during partitioning



# Related Work II

- Statistical Bellman-Ford (SBF) algorithm
  - Ekpanyapong, Watewai, and Lim [ASPDAC06]
  - BF computes longest paths on cyclic graphs
    - BF does not converge if the graph contains positive cycles
  - Statistical BF
    - Delay values are distribution
    - It is possible a negative cycle becomes positive with some probability
    - Showed how to handle statistically positive cycles

# Our SRTA Algorithm

- Overview
  - Statistical version of RTA algorithm (= RTA+SBF)
  - RTA needs Bellman-Ford, so we need SBF
  - Computes timing slack distribution of statistically critical paths under retiming
    - $O(n^2)$ in the worst-case, $O(k \cdot n)$ in practice
  - Used in performance-driven min-cut global placement

# Statistical Timing Model

- Gate/Wire delay distribution

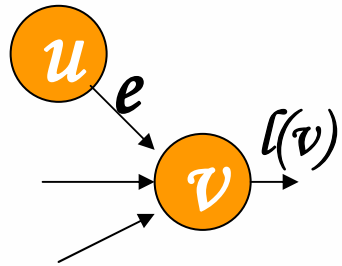
$$d(v) = d_m(v) + a_1 \Delta L_g^t(v) + a_2 \Delta W_g^t(v)$$

$$d(e) = d_m(e) + \sum_{k \in T(e)} \left[ b_1 \Delta W_i^k(e) + b_2 \Delta T_i^k(e) \right]$$

# Statistical Sequential Slack

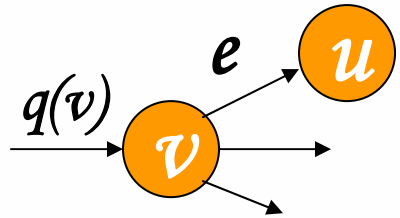
- Statistical Sequential Arrival Time (SSAT)
  - Arrival time distribution at *v* if all PI-to-*v* paths are retimed to φ

$$l(v) = \max\{l(u) - \phi \cdot w(e) + d(e) + d(v) | e(u,v) \in E\}$$




- Statistical Sequential Required Time (SSRT)
  - Required time distribution at *v* if all *v*-to-PO paths are retimed to φ

$$q(v) = \min\{q(u) + \phi \cdot w(e) - d(e) - d(v) | e(v,u) \in E\}$$



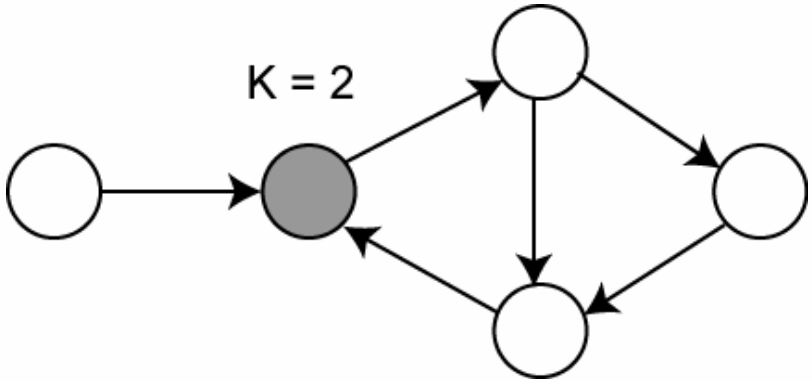

- Statistical Sequential Slack (SSSK) = SSRT-SSAT

# Overview of SRTA

```
Given: φ (target clock period for retiming)
1. Perform DFS and compute K;
2. for (i = 0 to K+1)
3.     for (each vertex v)
4.         compute SSAT(v,φ);
5.         compute SSRT(v,φ);
6. compute MFCPD (Min Feasible Clock Period Distrubition);
7. Pc = probability(positive_cycle);
8. if (Pc < threshold)
       return(MFCPD);
9. return(FALSE);
```

# Number of Iterations

- Computation of *k* using depth-first search
  - K = maximum number of cycles a node is included in
  - A single DFS finds this number



# Statistical Target Clock Period

- Computation of MFCPD
  - Min Feasible Clock Period Distribution
  - Statistical Maximum between
    - SSAT (Statistical Sequential Arrival Time) of all sink nodes
    - Delay distribution of the longest cycle

# Comparisons

- We compare
  - STA: Static Timing Analysis
  - SSTA: Statistical Static Timing Analysis
  - RTA: Retiming-based Timing Analysis
  - SRTA: Statistical Retiming-based Timing Analysis

# Comparisons (cont)

| | STA | SSTA | RTA | SRTA |
|---|---|---|---|---|
| Basic Algorithm | Topological sort | Topological sort with statistical operation | Bellman-Ford | Bellman-Ford with statistical operation |
| Complexity | O($n$) | O($n$) | O($n^2$)<br>O($k.n$) in practice | O($n^2$)<br>O($k.n$) in practice |
| Advantage | Simple<br>Fast | Can handle process variation | Model retiming delay | Faster Circuit<br>Can handle process variation |
| Disadvantage | No retiming<br>No statistical | Slow<br>No retiming | Slow<br>No statistical | Slow |

# Experimental Results

- Benchmark circuits

| ckt | gate | PI | PO | FF | K+1 |
|---|---|---|---|---|---|
| **s5378** | 2828 | 36 | 49 | 163 | 76 |
| **s9234** | 5597 | 36 | 39 | 211 | 239 |
| **s13207** | 8027 | 31 | 121 | 669 | 510 |
| **s15850** | 9786 | 14 | 87 | 597 | 495 |
| **s38417** | 22397 | 28 | 106 | 1636 | 1444 |
| **s38584** | 19407 | 12 | 278 | 1452 | 1860 |
| **b14o** | 5401 | 32 | 299 | 245 | 451 |
| **b15o** | 7092 | 37 | 519 | 449 | 988 |
| **b20o** | 11979 | 32 | 512 | 490 | 1486 |
| **b21o** | 12156 | 32 | 512 | 490 | 1511 |
| **b22o** | 17351 | 32 | 725 | 703 | 1870 |

# Experimental Results

- MFCPD results

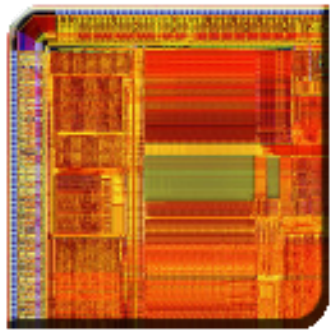
| ckt | Final MFCPD | Max Cycle | Sink SSAT |
|---|---|---|---|
| s5378 | **199.00** | **62.76** | 199.00 |
| S9234 | **257.03** | **225.08** | 257.03 |
| S13207 | **344.87** | **281.36** | 344.87 |
| S15850 | **410.53** | **276.76** | 410.53 |
| s38417 | **214.23** | 214.23 | **152.89** |
| s38584 | **494.73** | **394.07** | 494.73 |
| b14o | **176.36** | **137.44** | 176.36 |
| b15o | **278.53** | 278.53 | **57.56** |
| b20o | **295.11** | 295.11 | **117.14** |
| b21o | **295.70** | 295.70 | **275.72** |
| b22o | **366.36** | **318.80** | 366.36 |

# Global Placement Results

| ckt | Without retiming | | With retiming | |
|---|---|---|---|---|
| | STA | SSTA | RTA | SRTA |
| s5378 | 232.00 | 218.96 | 212.00 | 199.00 |
| s9234 | 407.00 | 379.05 | 287.00 | 257.03 |
| s13207 | 426.00 | 403.43 | 364.00 | 344.87 |
| s15850 | 575.00 | 532.59 | 435.00 | 410.53 |
| s38417 | 390.00 | 363.29 | 217.00 | 214.23 |
| s38584 | 576.00 | 554.21 | 515.00 | 494.73 |
| b14o | 375.00 | 351.86 | 195.00 | 176.36 |
| b15o | 352.00 | 327.57 | 292.00 | 278.53 |
| b20o | 516.00 | 484.09 | 318.00 | 295.11 |
| b21o | 518.00 | 479.66 | 320.00 | 295.70 |
| b22o | 626.00 | 605.99 | 375.00 | 366.36 |
| **Avg.** | 1 | 0.94 | 0.71 | 0.67 |

# Conclusions

- Process variation will make timing analysis more difficult in deep submicron design
- We propose an effective algorithm to compute statistical critical paths under retiming
- We show that the placement optimization based on SRTA achieves better performance results compared to other well-known timing analyzers



That’s all, folks !

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