Modeling the Overshooting Effect for CMOS Inverter in Nanometer Technologies

Zhangcai Huang*†,

Hong Yu*, Atsushi Kurokawa† and Yasuaki Inoue*

*Graduate School of Information, Production and Systems,

Waseda University, Kitakyushu, 808-0135 Japan

†Sanyo Semiconductor Co., Ltd, Gunma, 370-0596 Japan

Email: †hzc_2002@asagi.waseda.jp

Outline

- Background
- Analytical expressions for overshooting effect
- Considering process variation
- Simulation results
- Conclusions

Outline

- Background
- Analytical expressions for overshooting effect
- Considering process variation
- Simulation results
- Conclusions

$$C_L \frac{dV_{out}}{dt} = I_p - I_n + C_M \frac{d\left(V_{in} - V_{out}\right)}{dt},$$

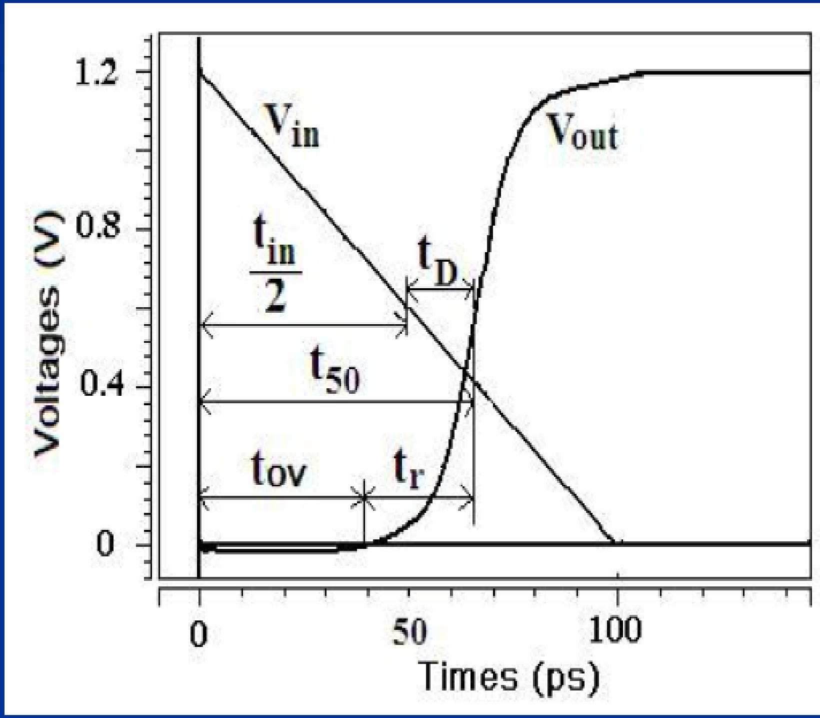
in

Vout

$$V_{in} = \begin{cases} V_{DD} & : \quad t \le 0 \\ (1 - \frac{t}{t_{in}})V_{DD} & : \quad 0 \le t \le t_{in} \\ 0 & : \quad t > t_{in} \end{cases},$$

“C_M is known as the Miller effect, but is seldom of importance in digital circuits. It is, however, of major importance in analog circuits.”

I. Background



$$t_D = t_{50} - \frac{1}{2} t_{in}$$

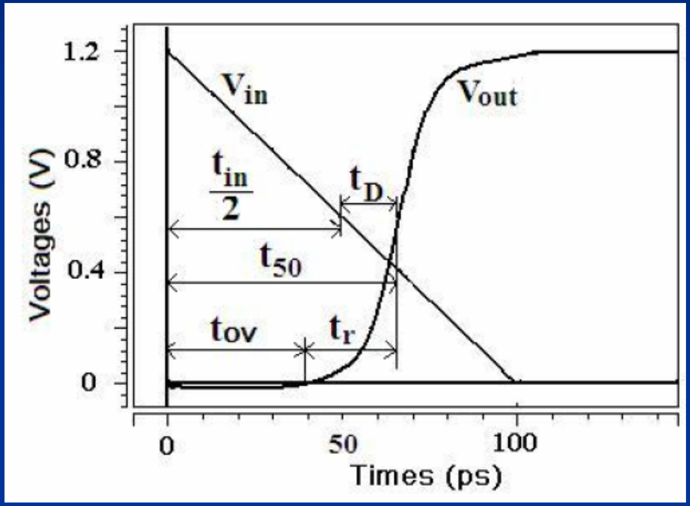
$$t_D = t_{ov} + t_r - \frac{1}{2} t_{in}$$

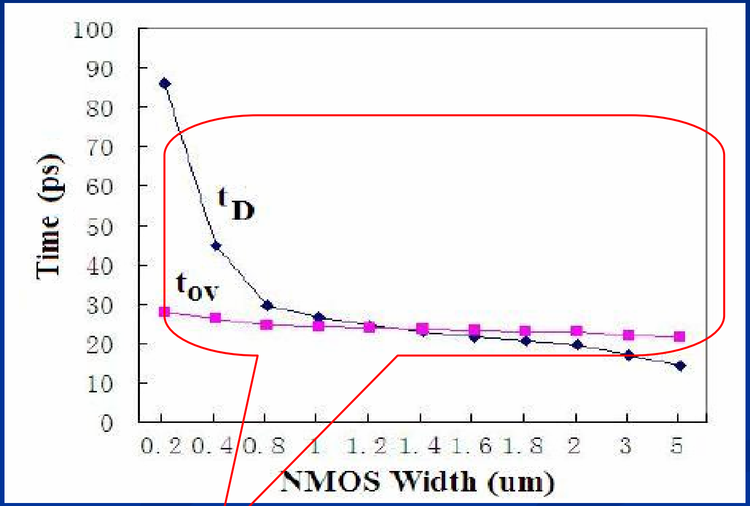
Proposed Model

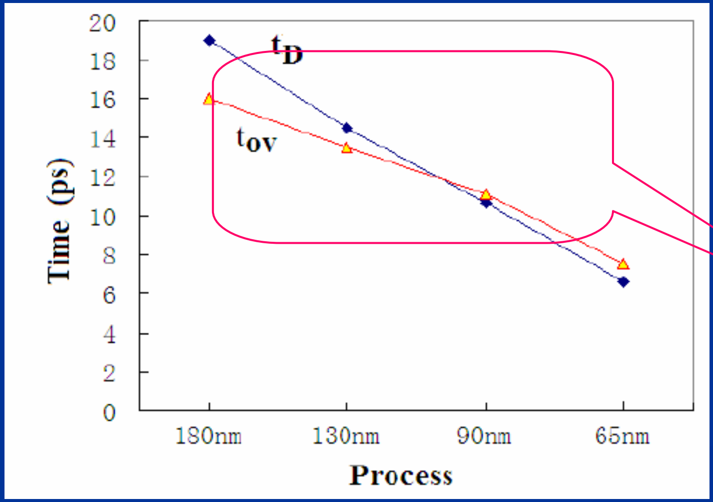
For traditional process technologies, the effect of overshooting is very small and can be neglected

I. Background

The influence of overshooting time on timing analysis





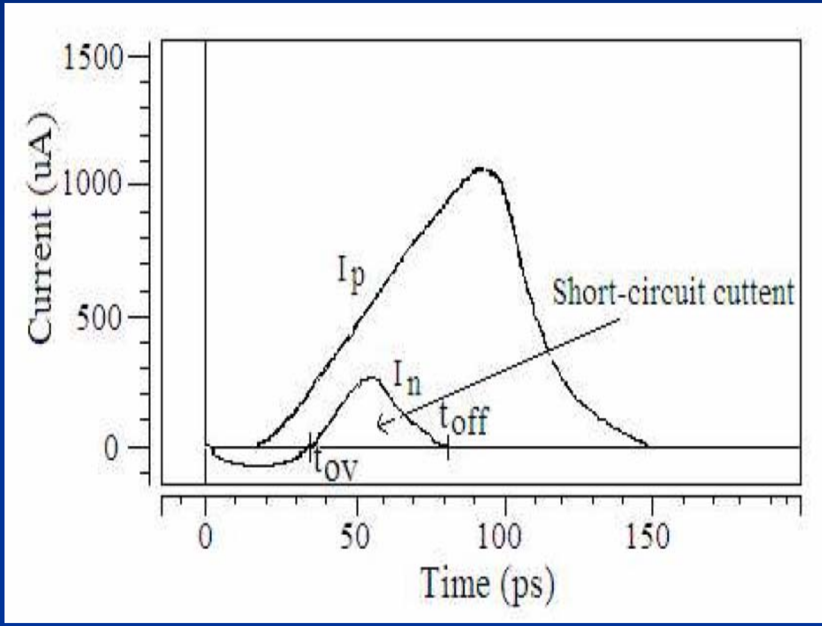


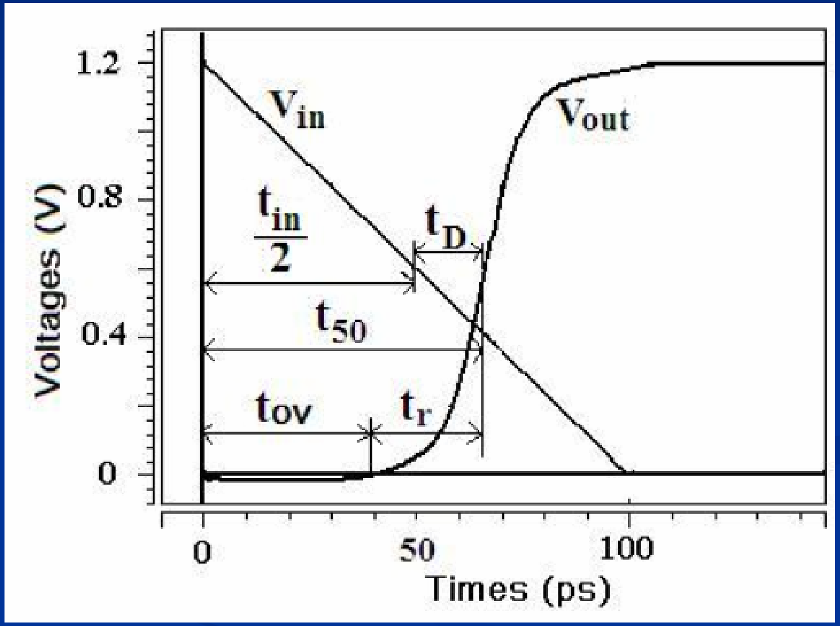
t_r and td decrease much faster than t_{ov} with the increasing of gate sizes. And t_{ov} is equal to or larger than t_r.

With the scaling of technology process, t_{ov} becomes much important for delay time.

I. Background

The influence of overshooting time on power analysis





Short-circuit power consumption

$$P = V_{DD} \int_{t_{ov}}^{t_{off}} I_n dt$$

The overshooting time is one important parameter for power consumption estimation.

I. Background

Conventional models for overshooting time

The overshooting time is neglected

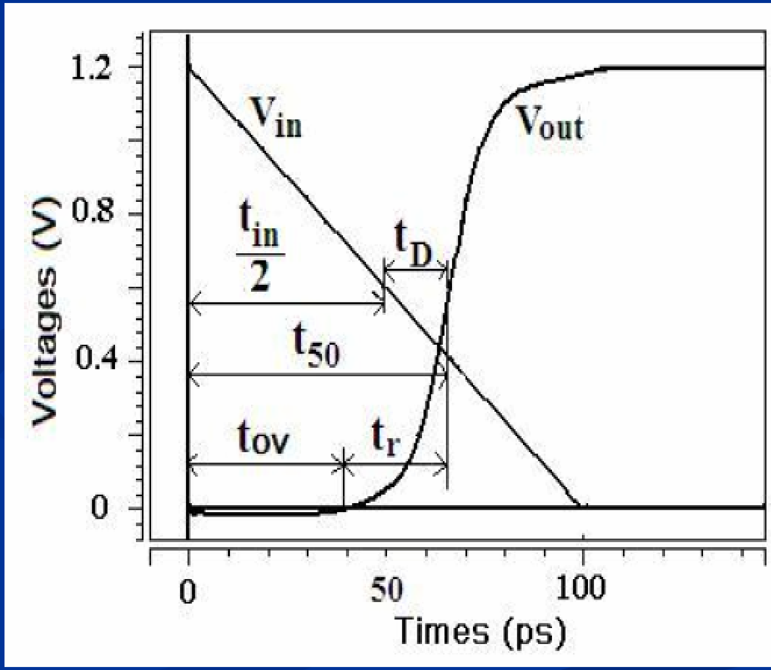
$t_{ov}=0.$

The overshooting time is assumed as simple value

$t_{ov} = (V_t / V_{dd}) t_{in}$

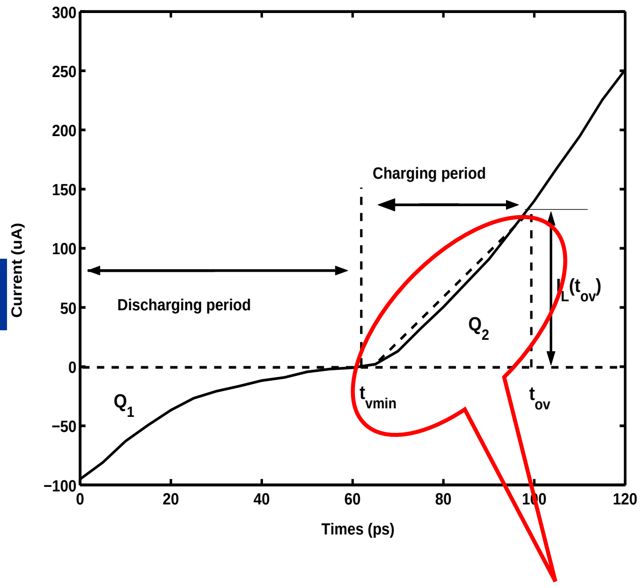
empirical expressions

J. L. Rossell, …"Charge-based analytical model for the evaluation of power consumption …", TCAD 2002.



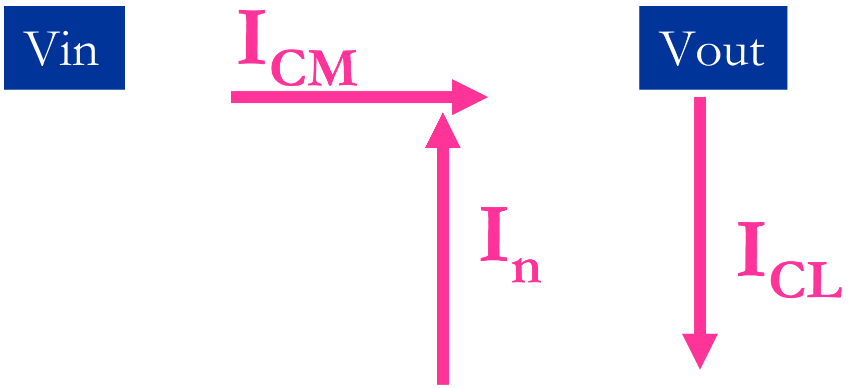
Outline

- Background
- Analytical expressions for overshooting effect
- Considering process variation
- Simulation results
- Conclusions



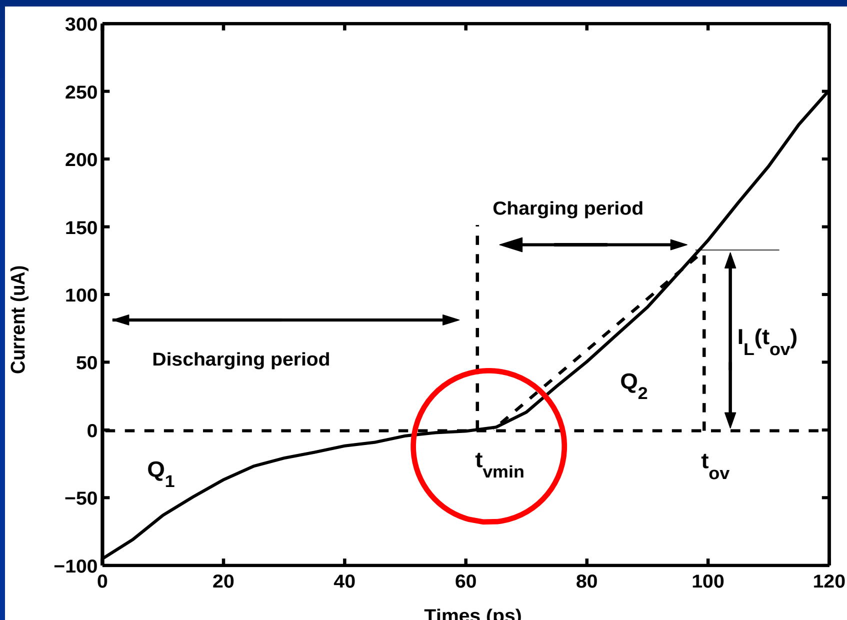
300
250
200
150
100
50
0
−50
−100
0
20
40
60
80
100
120
Current (uA)
Times (ps)
Charging period
Discharging period
Q1
Q2
I_L(t_ov)
t_vmin
t_ov

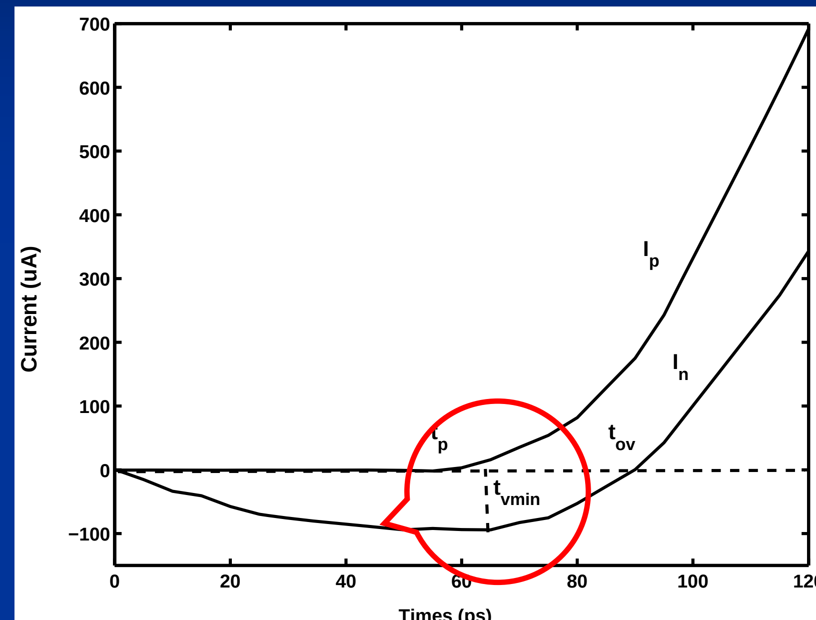
II. Proposed Model



$$V_{out}(t) = \frac{C_M \dfrac{dVin}{dt}}{\beta_n\left(\hat{V}_{GS} - V_{THN}\right)}\left[1 - e^{-\frac{\beta_n\left(\hat{V}_{GS} - V_{THN}\right)}{C_L + C_M}}\right]$$

II. Proposed Model





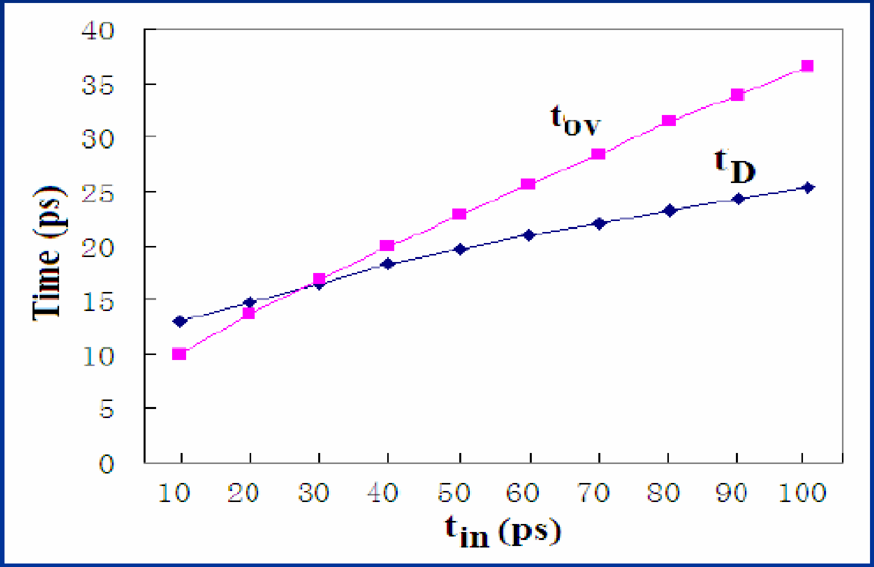
$$t_{vmin} = t_T + \kappa(t_{in} - t_T),$$

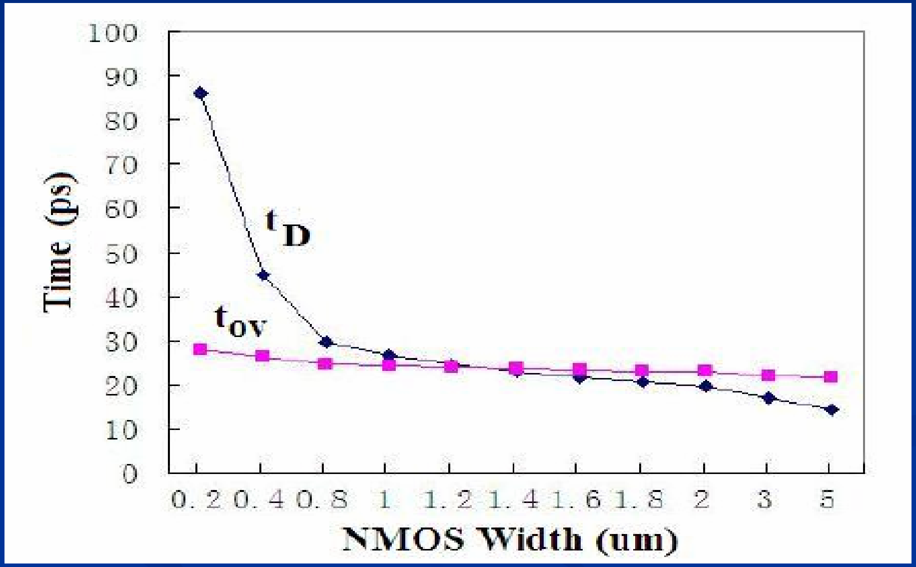
$$\kappa = \frac{C_M V_{DD} e^{-\frac{\beta(V_{DD}-V_T)}{CL+C_M} t_T}}{t_{in} I_{D0}}.$$

$$t_{ov} = t_{vmin} - \frac{1}{2}\left[t_{vmin} - t_{Teff} - C_M \frac{V_{DD}}{t_{in}} \frac{t_{in} - t_{Teff}}{I_{D0}}\right] + \sqrt{\frac{2Q_1}{I_{D0}}(t_{in} - t_{Teff}) + \frac{1}{4}\left[t_{vmin} - t_{Teff} - C_M \frac{V_{DD}}{t_{in}} \frac{t_{in} - t_{Teff}}{I_{D0}}\right]^2},$$

II. Proposed Model

Minimum overshooting time





$$\lim_{t_{in}\to 0} t_{ov} = t_{ov}^{min} = \frac{C_M}{I_{D0}}(V_{DD} - V_{Teff}),$$

$$t_D = t_{ov} + t_r - \frac{1}{2} t_{in}$$

The overshooting time has minimum values.

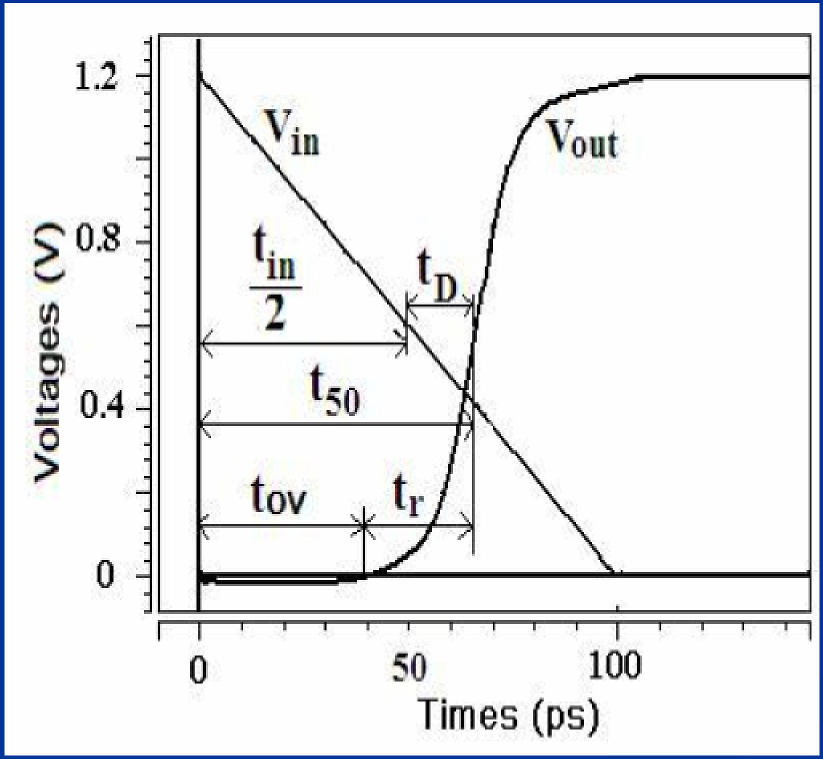
Minimum delay > Minimum overshooting time

Outline

- Background
- Analytical expressions for overshooting effect
- Considering process variation
- Simulation results
- Conclusions

III. Considering Process Variation

In recent technologies, the variability of circuit performance due to the process variation has become a significant concern. As process geometries continue to shrink, the evaluation for critical device parameters is becoming more and more difficult due to the significant variations



The sensitivities of the overshooting time with respect to the variation sources.

$$t_{ov} = t_{ov}^0 + \frac{\partial t_{ov}}{\partial V_T}\Delta V_T + \frac{\partial t_{ov}}{\partial T_{ox}}\Delta T_{ox} + \frac{\partial t_{ov}}{\partial L}\Delta L,$$

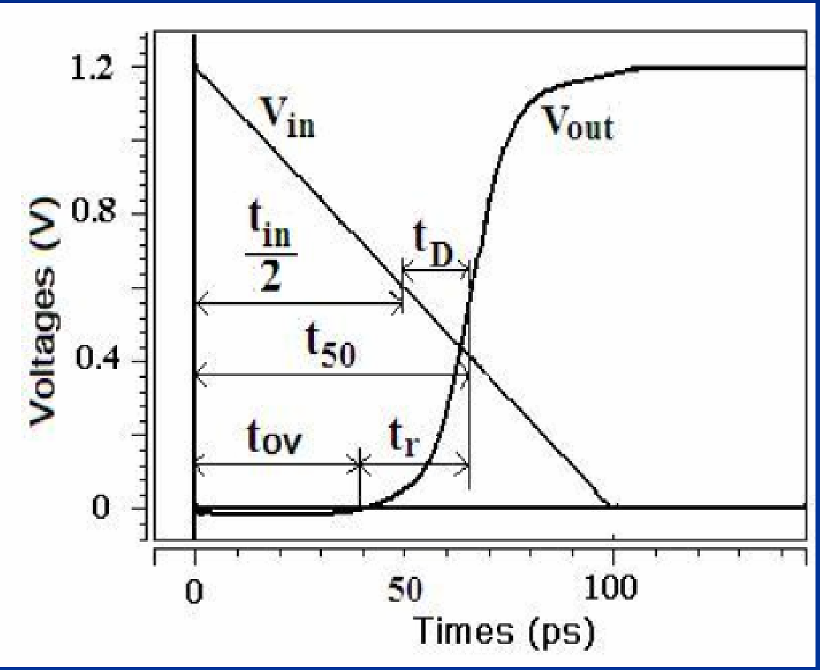
With respect to the variation of length.

$$\frac{\partial t_{ov}}{\partial L} = \lambda_L \simeq 0,$$

With respect to the variation of threshold voltage.

$$\frac{\partial t_{ov}}{\partial V_T} = \lambda_{V_T} \approx \frac{t_{in}}{V_{DD}}\left[1 - \kappa - \xi(1 - C_M \frac{V_{DD}}{t_{in} I_{D0}})\right],$$

III. Considering Process Variation



$$t_D = t_{ov} + t_r - \frac{1}{2} t_{in}$$

$$\frac{\partial t_{ov}}{\partial L} = \lambda_L \simeq 0,$$

Variation of L has no influence on the overshooting time.

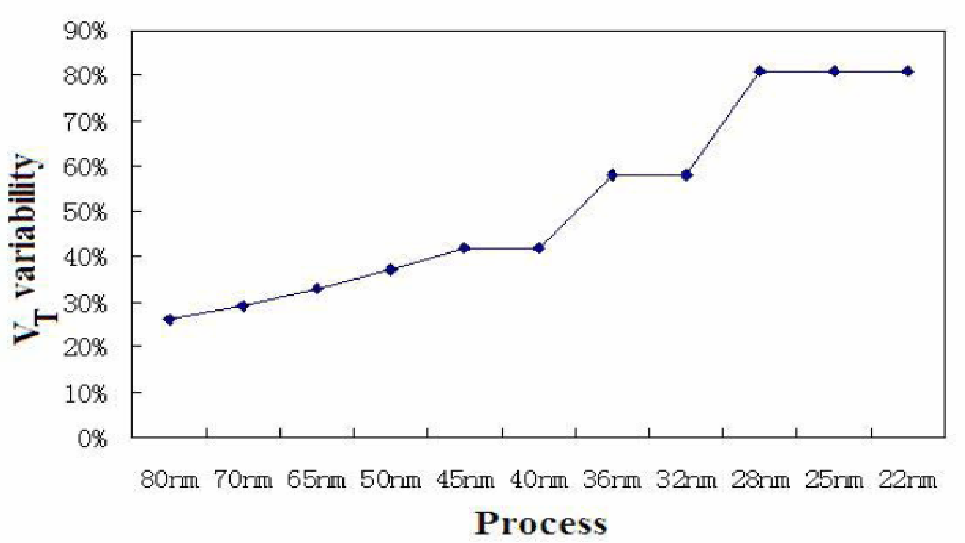
Variation of L has the influence only on the rising time.

Variation of L has significant influence on the gate delay.

D. Sinha, …"Gate Sizing Using Incremental Parameterized Statistical Timing Analysis" ICCAD-2005

III. Considering Process Variation

tin (ps)	mean (ps)	σ for V_T (ps)	σ for L (ps)	σ for Tox (ps)
20	14.65	0.24	0	0.04
40	21.18	0.41	0	0.12
60	27.06	0.57	0	0.21
80	32.62	0.73	0	0.305
100	37.95	0.9	0	0.402



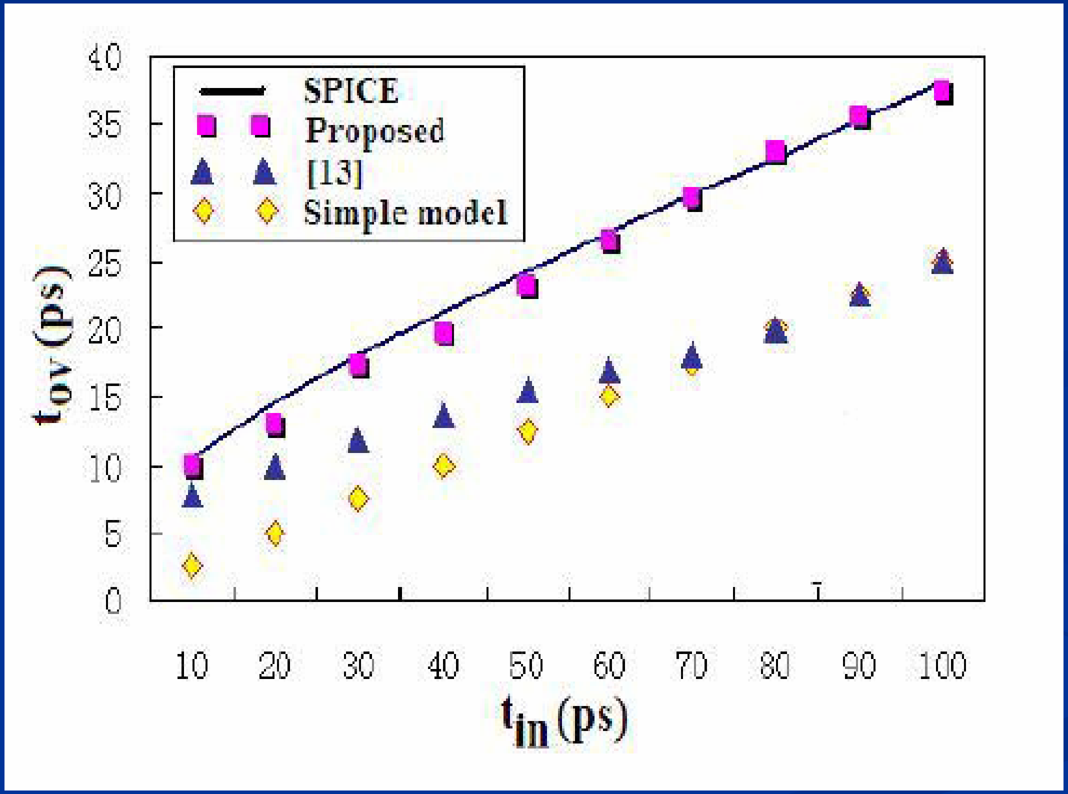
1. With input time decreases, the influence due to the Tox decreases greatly.
2. The influence due to L is 0.
3. With the scaling of process technologies, the variation of Vt increases, the influence due to Vt will increase greatly.

International Technology Roadmap for Semiconductors (ITRS) 2005.

Outline

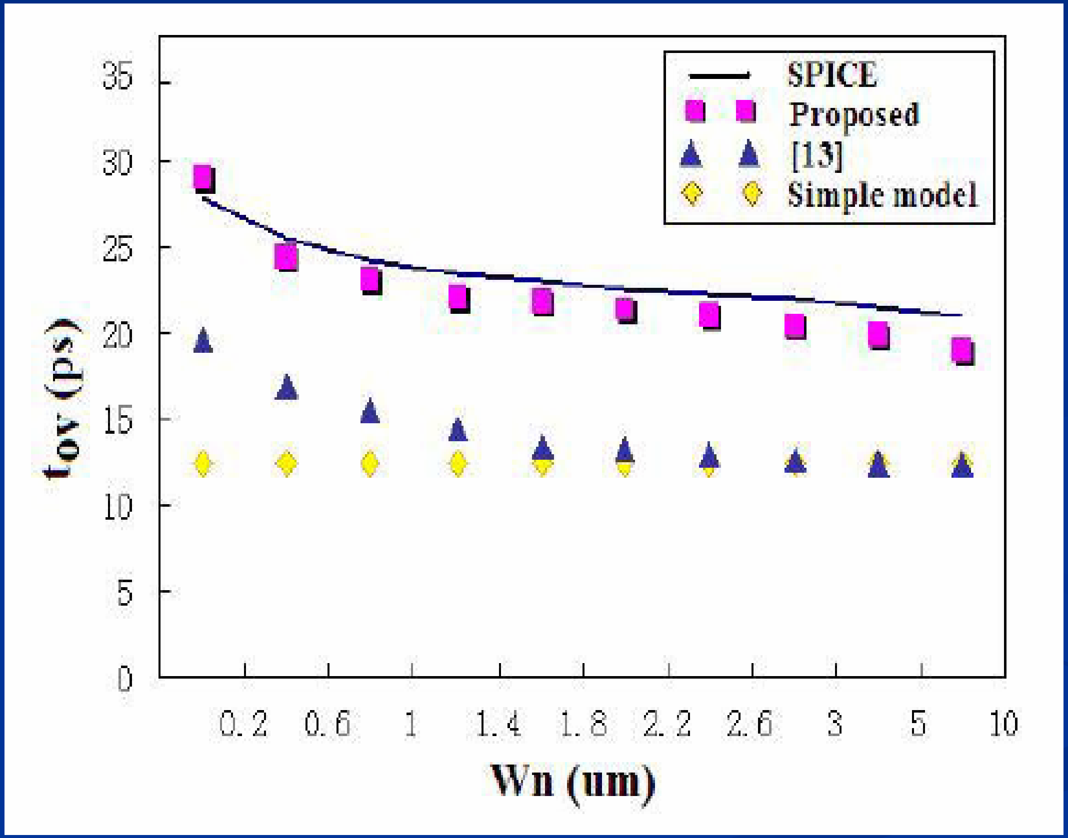
- Background
- Analytical expressions for overshooting effect
- Considering process variation
- Simulation results
- Conclusions

IV. Simulation Results



J.L. Rossell: "Charge-based analytical model for the evaluation of power consumption in submicron CMOS buffers", TCAD 2002.

IV. Simulation Results



J.L. Rossell: "Charge-based analytical model for the evaluation of power consumption in submicron CMOS buffers", TCAD 2002.

Outline

- Background
- Analytical expressions for overshooting effect
- Considering process variation
- Simulation results
- Conclusions

V. Conclusions

- The input-to-output coupling capacitance has been proved to has significant influence on CMOS gates: timing analysis and power analysis.
- The overshooting time has become one of main parts of gate delay.
- The analytical model for overshooting time is derived.

  1. The overshooting time has minimum value

  2. Gate delay cannot be smaller than this minimum value.
- Considering process variation:

  1. The variation due to L has the influence only on output rising time, but has almost no influence on overshooting time.

  2. The variation due to Vt has the most significant influence on overshooting time with the scaling of technologies.

Thank you for your attentions