Plenary Talk

Overview on Low Power SoC Design Technology

Kimiyoshi Usami

Dept. of Information Science and Engineering

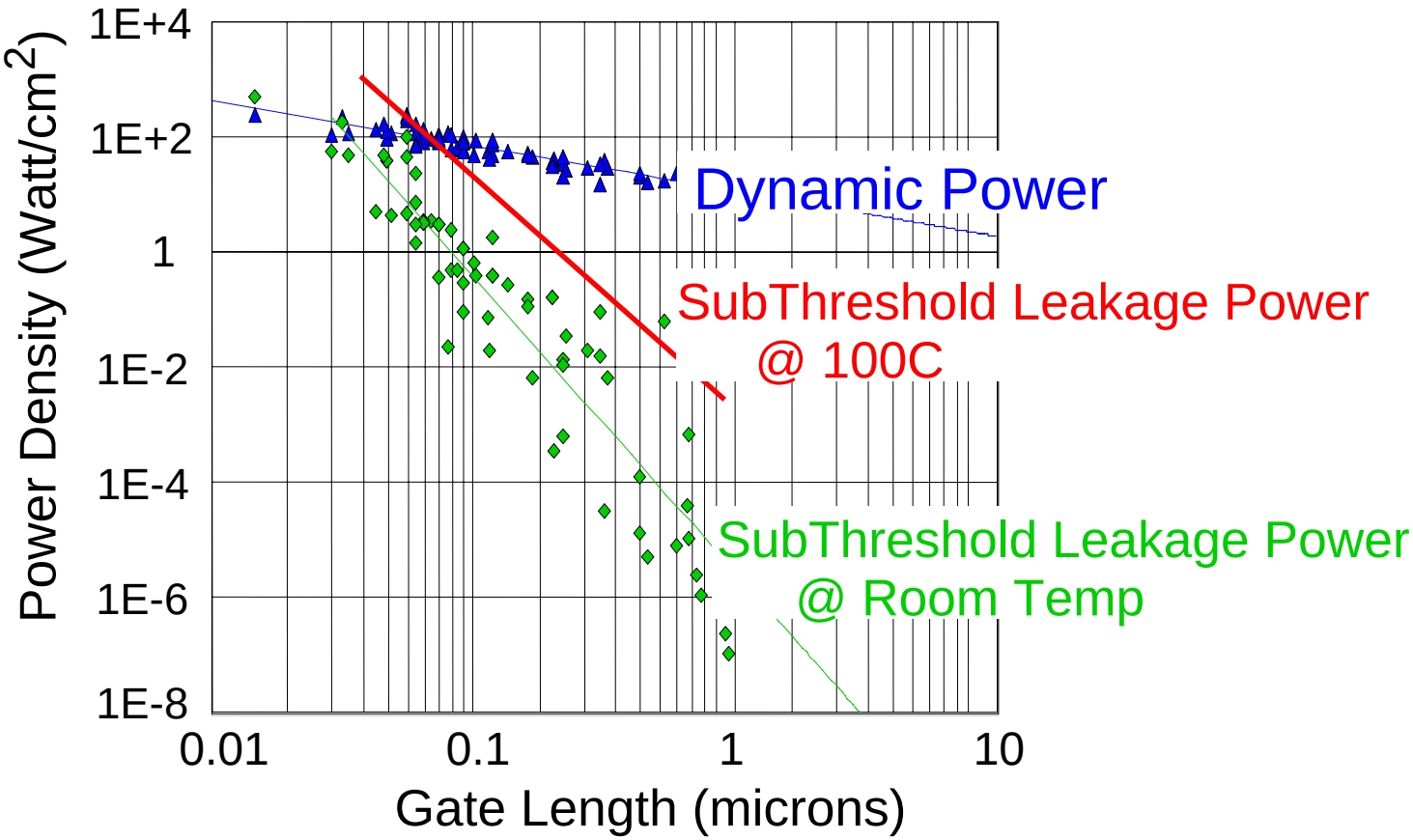
Shibaura Institute of Technology

Tokyo, Japan

Outline

1. Background
   Trend on power dissipation in SoC
2. Conventional design techniques to reduce leakage
3. Techniques to reduce Active Leakage
4. Summary

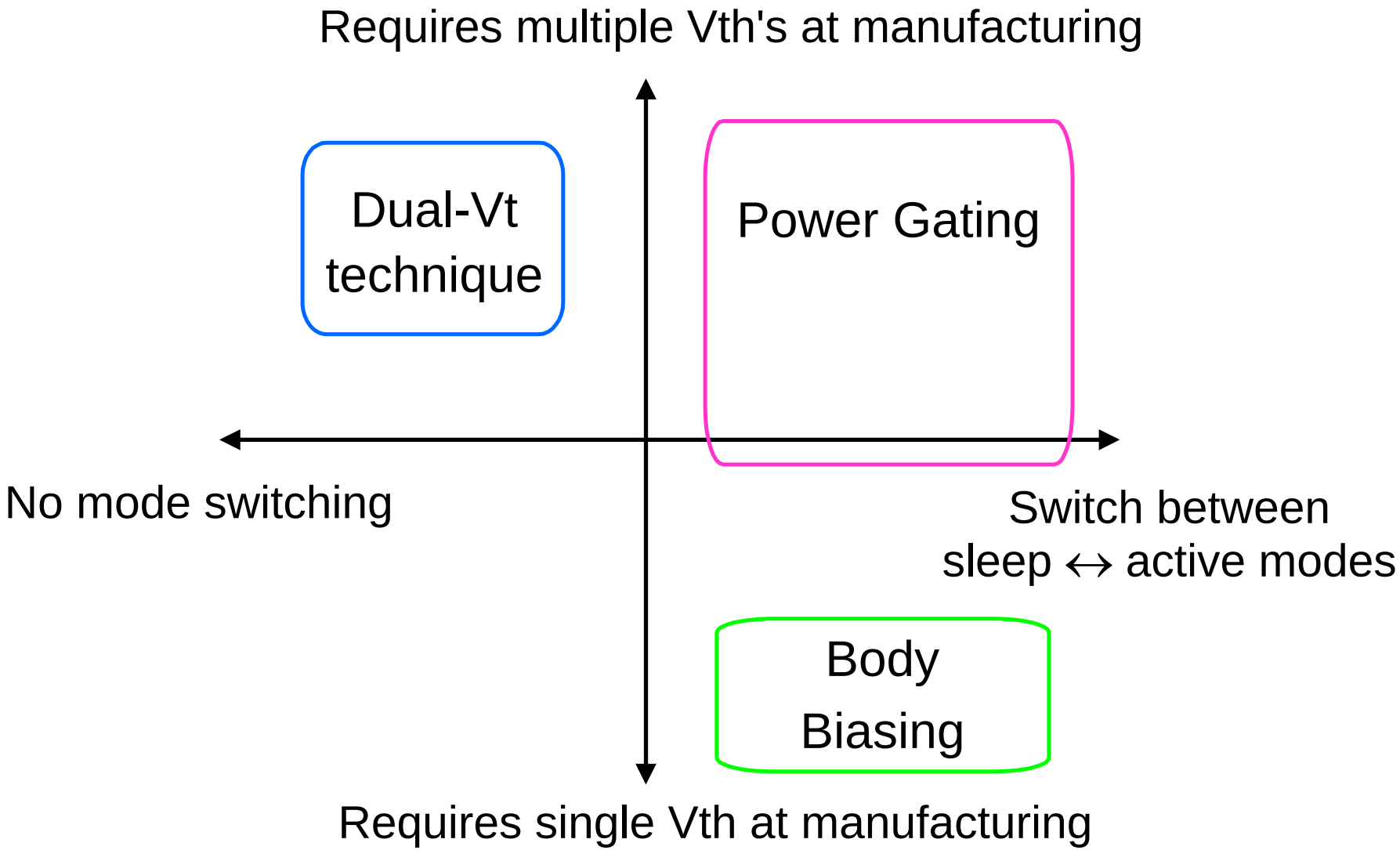
Trend on Power Dissipation



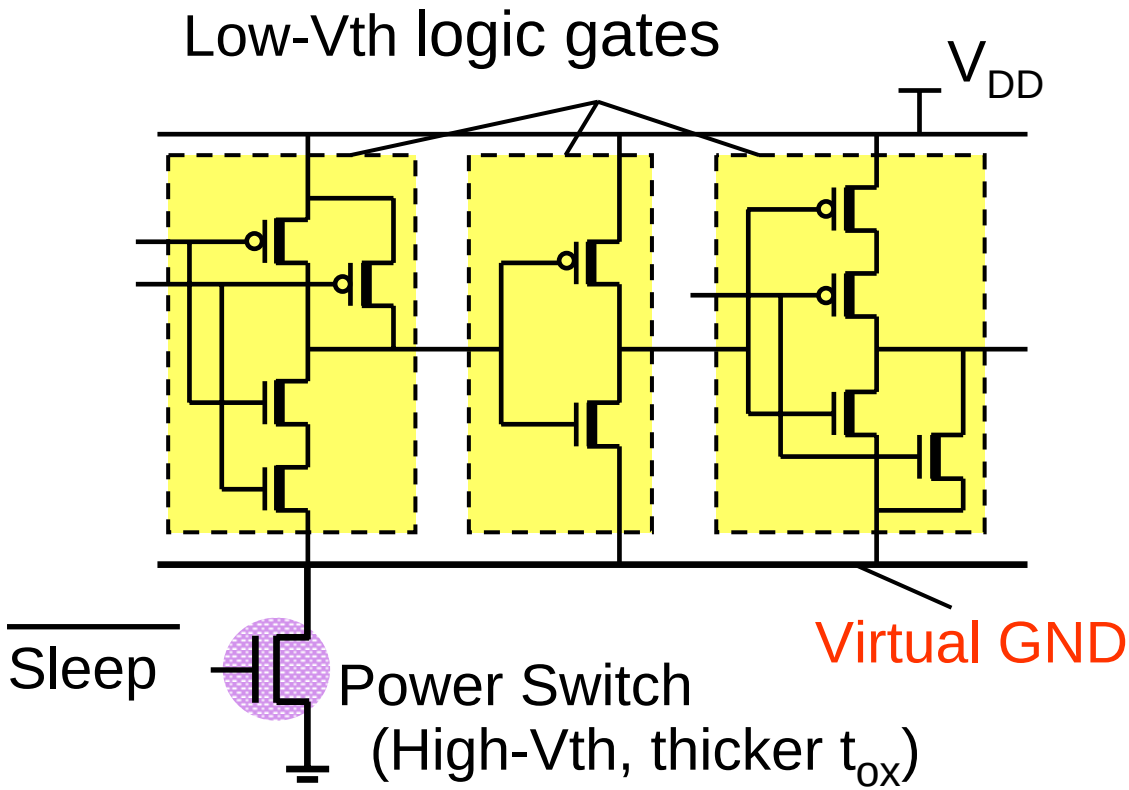
Source: D. Lackey, et al, DAC '03

- Dynamic power increases as device gets scaled
- Leakage power increases exponentially
  becomes equal to dynamic power at 20nm @RT; at 50nm @100C

Design techniques to reduce subthreshold leakage



Power Gating



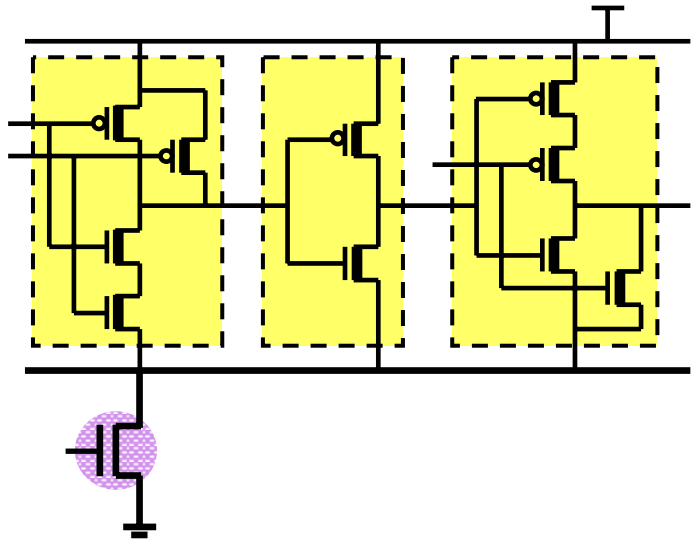
- Technique to turn off supply voltage
  using Power Switch (PS) to reduce leakage power
- Originally, used to reduce standby leakage

Approaches to reduce Active Leakage

- Power Gating to turn off PS even in operation time

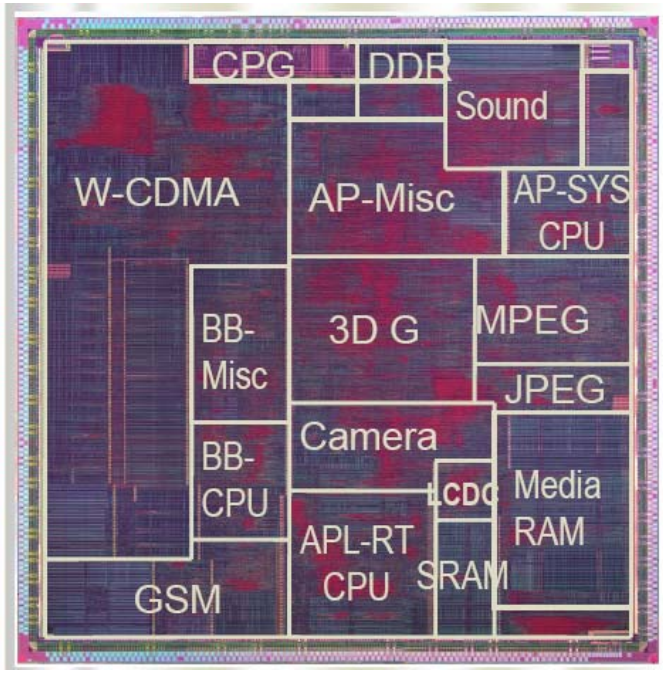
  " Run-time Power Gating "

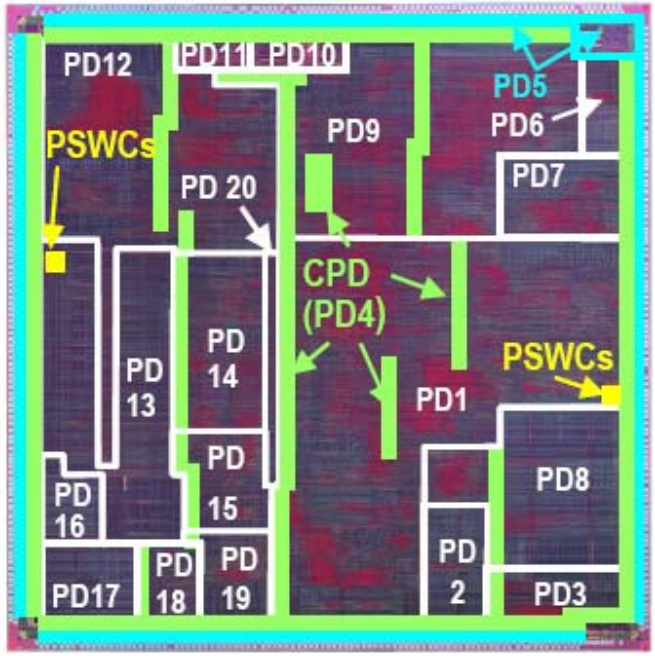
- Run-time Power Gating approaches
  - Module-level approach
  - Fine-grained approach



Module-level Run-time Power Gating

- Renesas Technology's mobile processor
- Partitioned into 20 Power Domains based on module
- Power Switch for each Power Domain controlled at run time corresponding to "scenes"

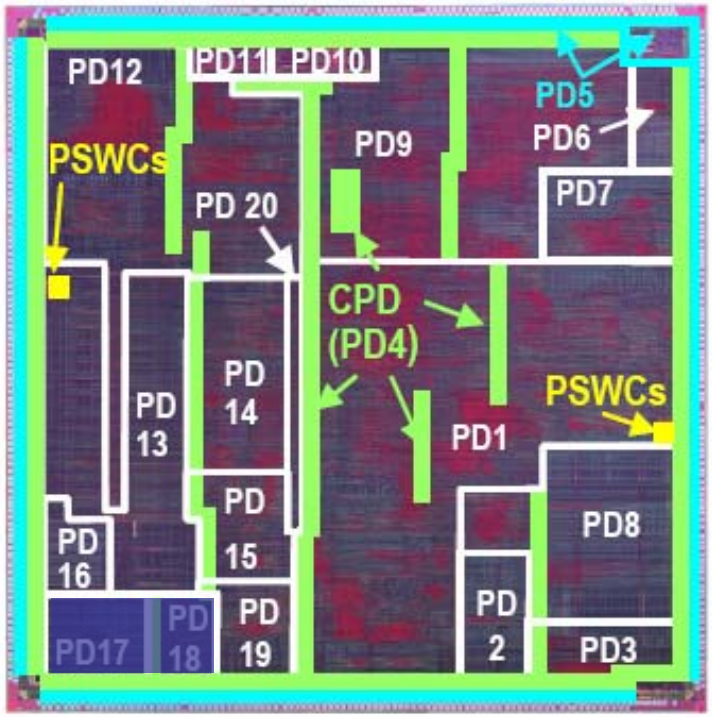




Courtesy: T. Hattori, et al, ISSCC2006, DAC'06

Module-level Run-time Power Gating (cont.)

Scene : Video telephony



Leakage: 849μA (RT, 1.2V)

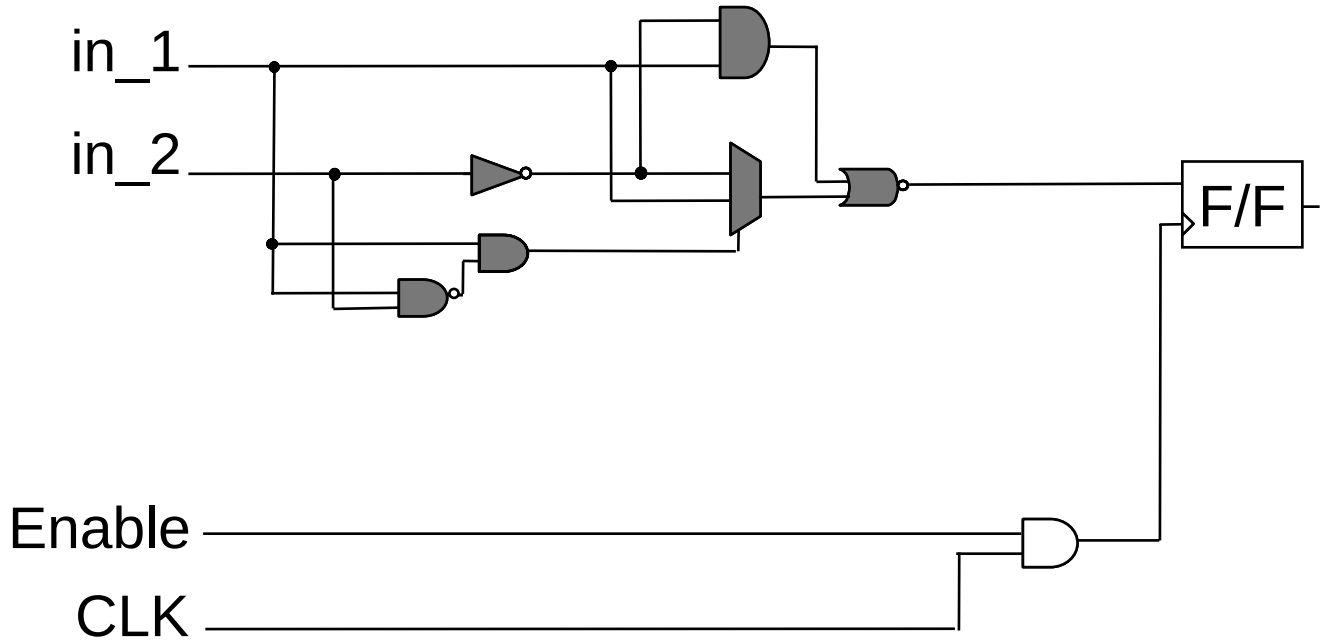
Scene : Waiting for calling

Leakage: 299μA (RT, 1.2V)

Courtesy: T. Hattori, et al, ISSCC2006, DAC'06

Fine-grained Run-time Power Gating

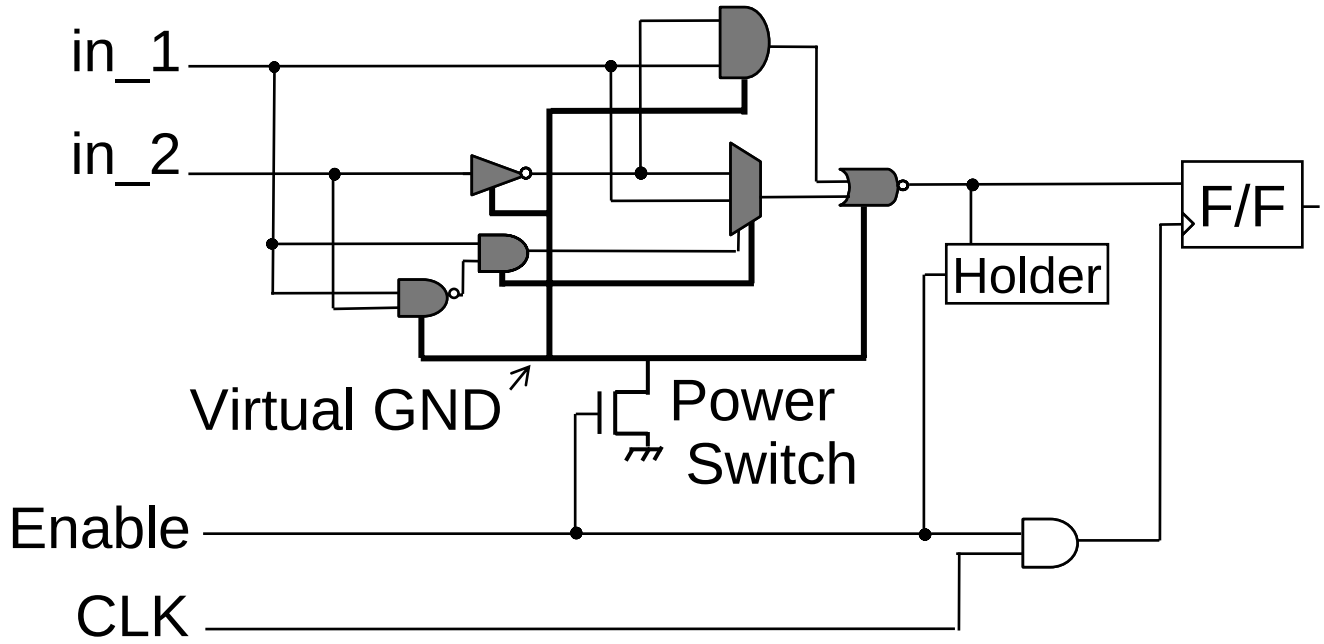
- Typical structure for gated clock design



- When enable = 0, stored data in F/F is not updated
  output of combinational logic is logically "don’t care"

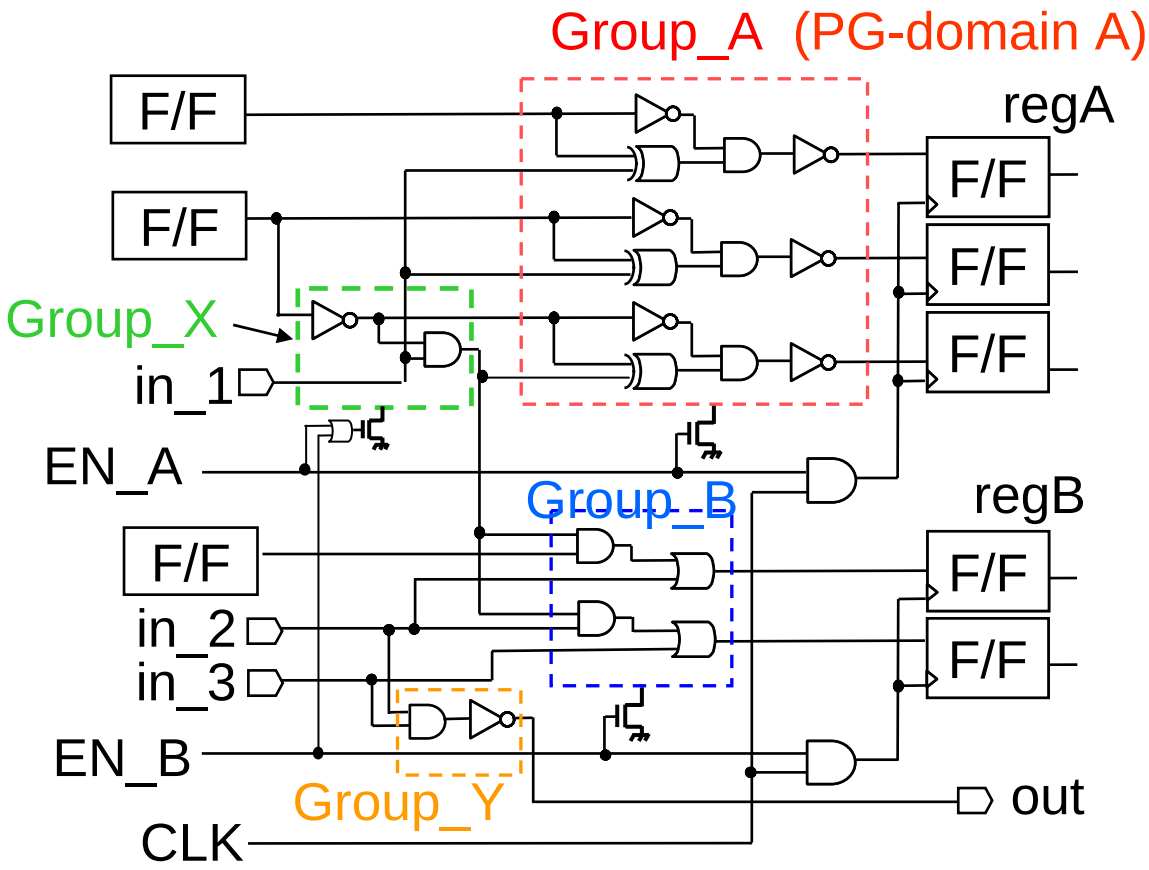
Fine-grained Run-time Power Gating (cont.)

- Exploiting enable signal of gated clock



K. Usami, et al, ICCD2006

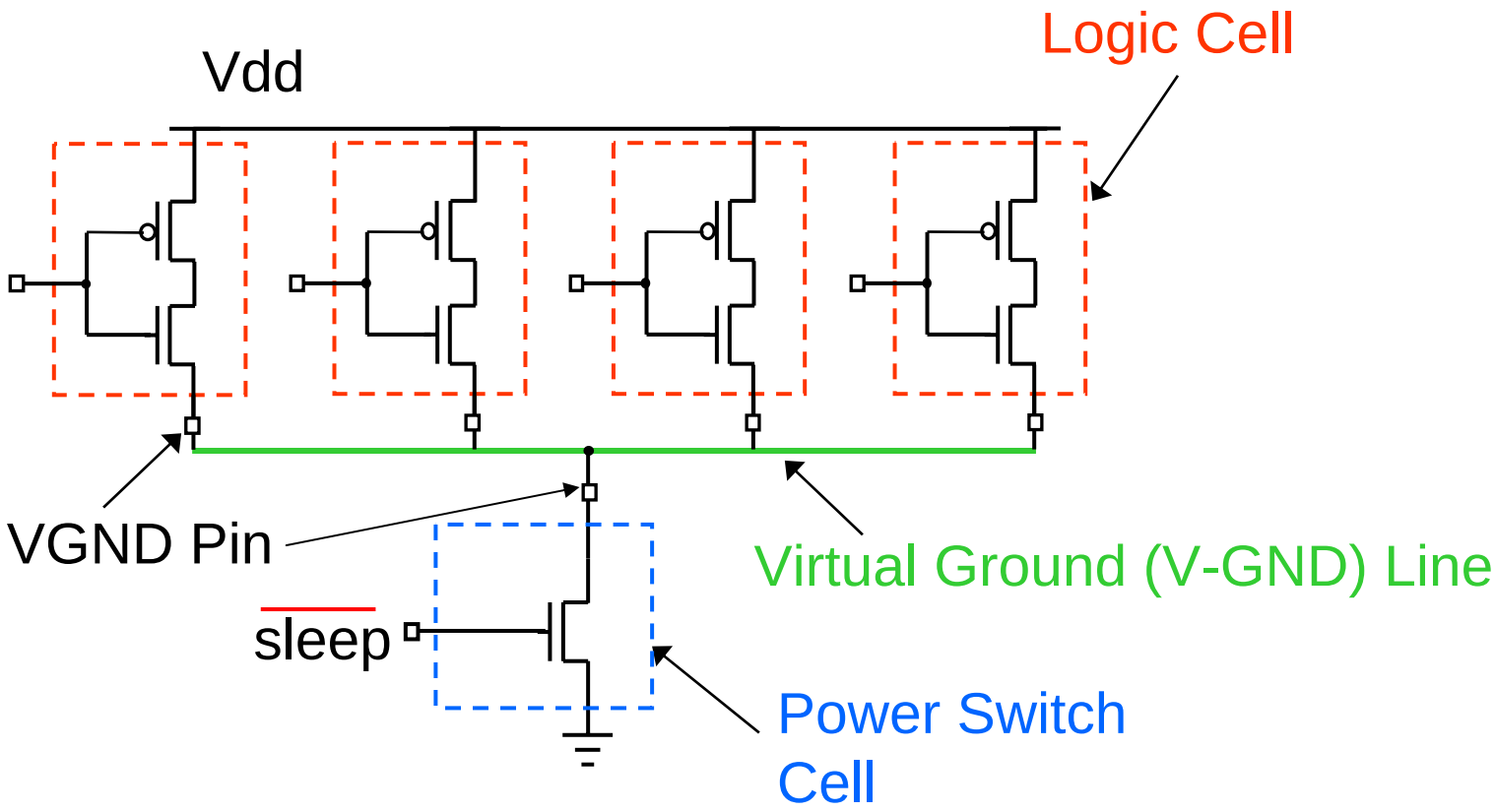
Fine-grained Run-time Power Gating (cont.)



- Partitioning logic gates into power-domains based on enable signals

K. Usami, et al, ICCD2006

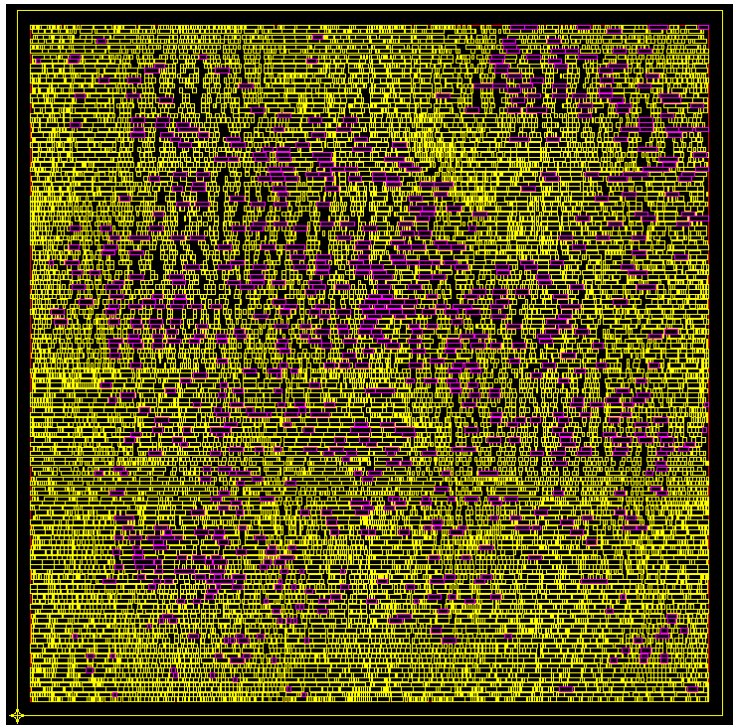
Fine-grained Run-time Power Gating (cont.)



- Logic gate and Power Switch are defined as "cell"
- V-GND line is routed as inter-cell wire

Fine-grained Run-time Power Gating (cont.)

- Applied to datapath in embedded microprocessor
- Datapath was partitioned into 66 Power domains based on enable signals



Power Switch cells highlighted in purple

Total: 17085 cells
incl. 1866 PS cells

- Active leakage power reduced by 83% at 90nm
- Area penalty by 20%

K. Usami, et al, ICCD2006

Summary

- Power dissipation in SoC gets more serious as device is scaled
- Share of leakage in the total operation power increases in further scaled devices
- Run-time Power Gating will become important to reduce active leakage power

Thank you !