Development of Low Power ISDB-T One-Segment Decoder by Mobile Multi-Media Engine SoC (S1G)

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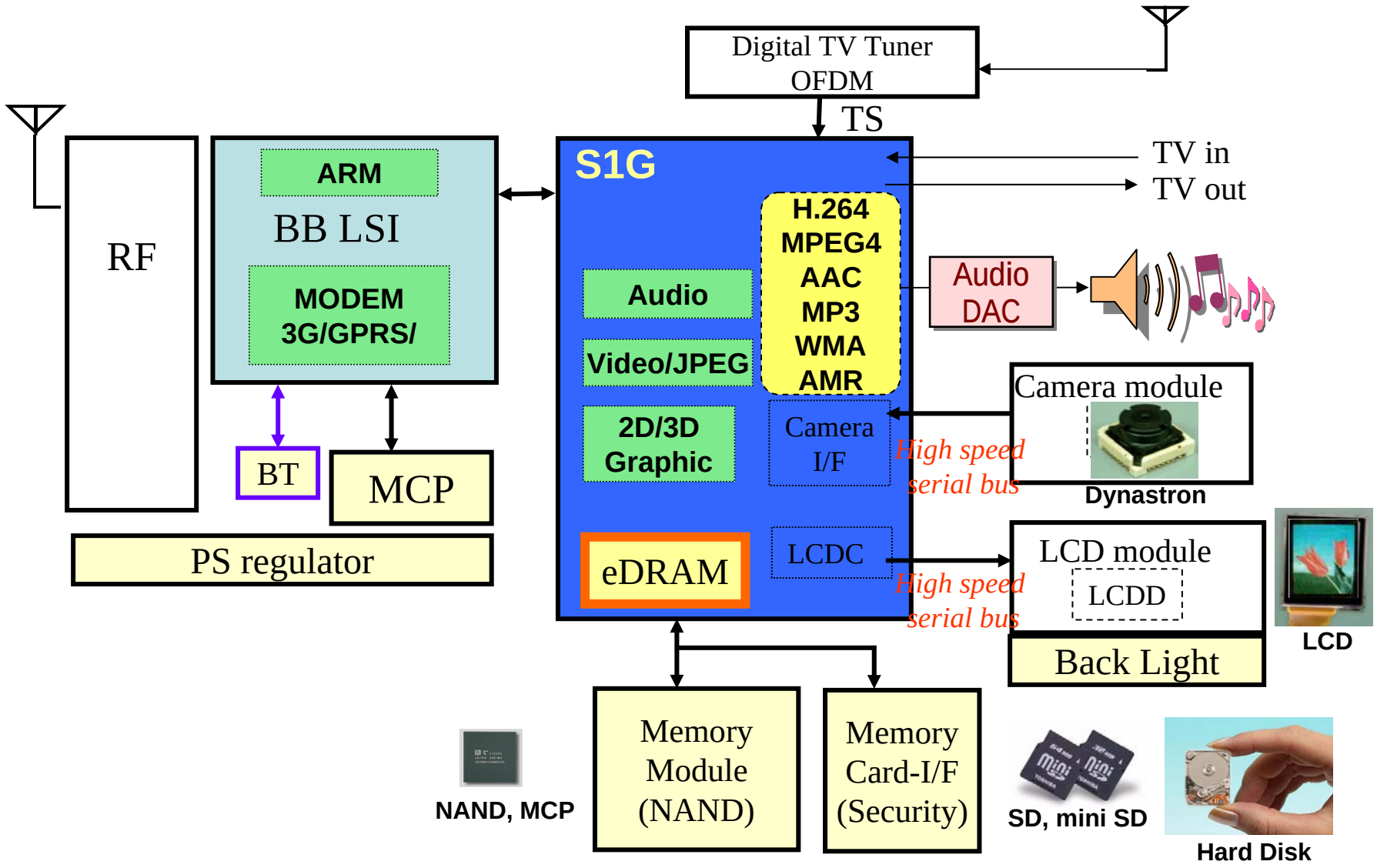
Jan. 25, 2007

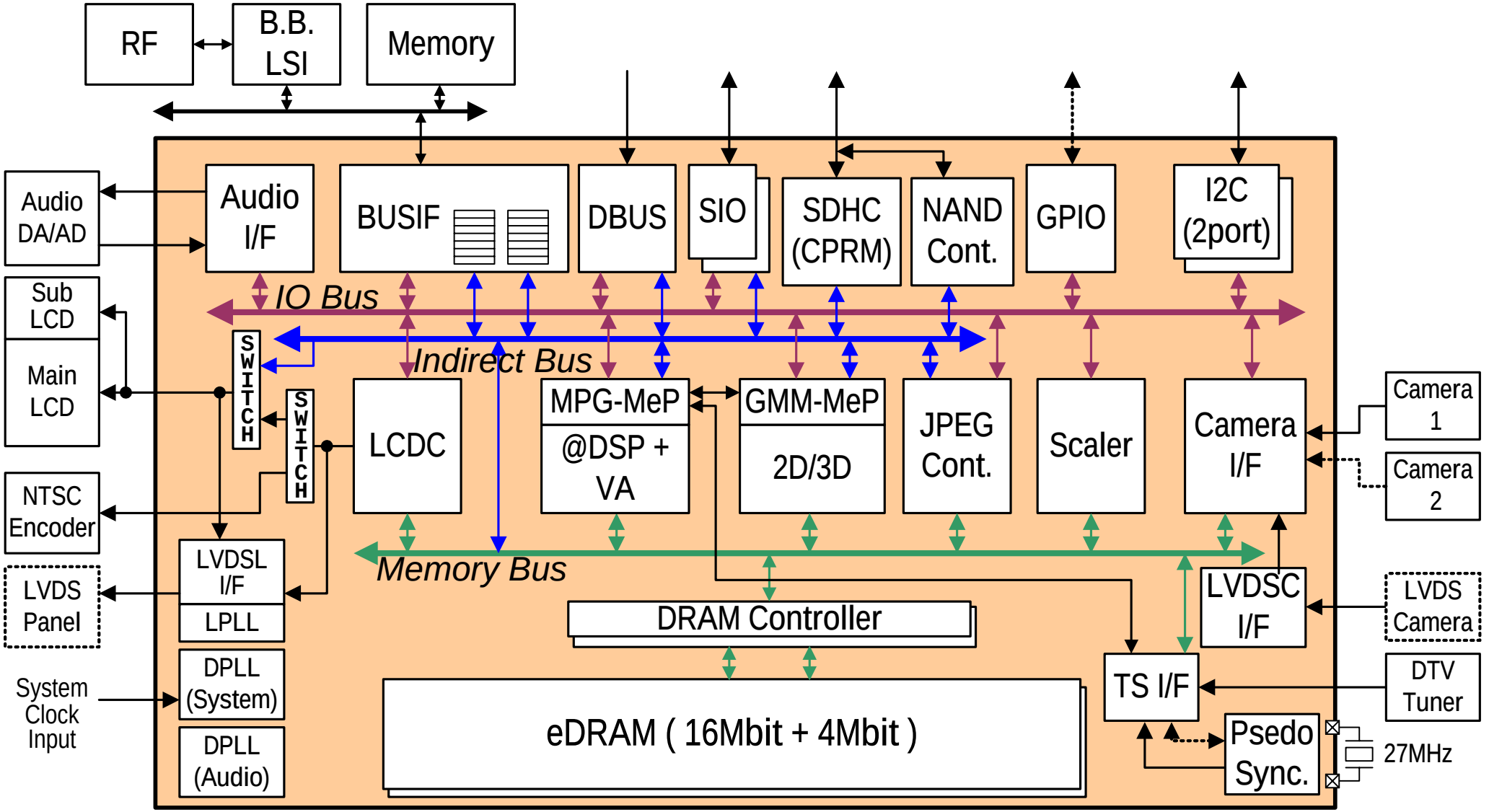
Outline

- System Overview
- Chip Specification
- Power Comparison
- Low Power Analysis
  - Multi-Vth Technique
  - Clock Gating Techniques
  - Software Architecture
- Summary

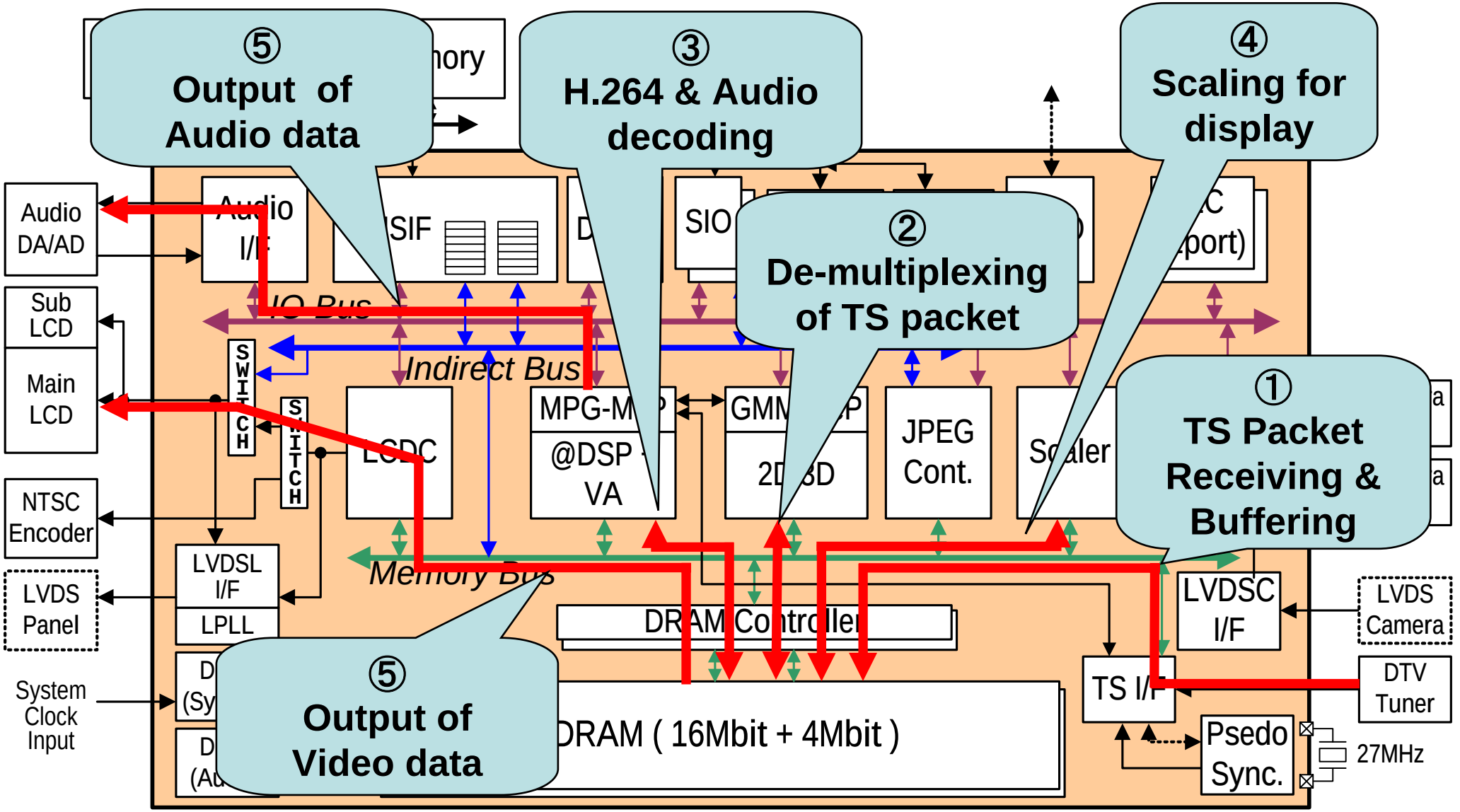
S1G in Mobile Phone System



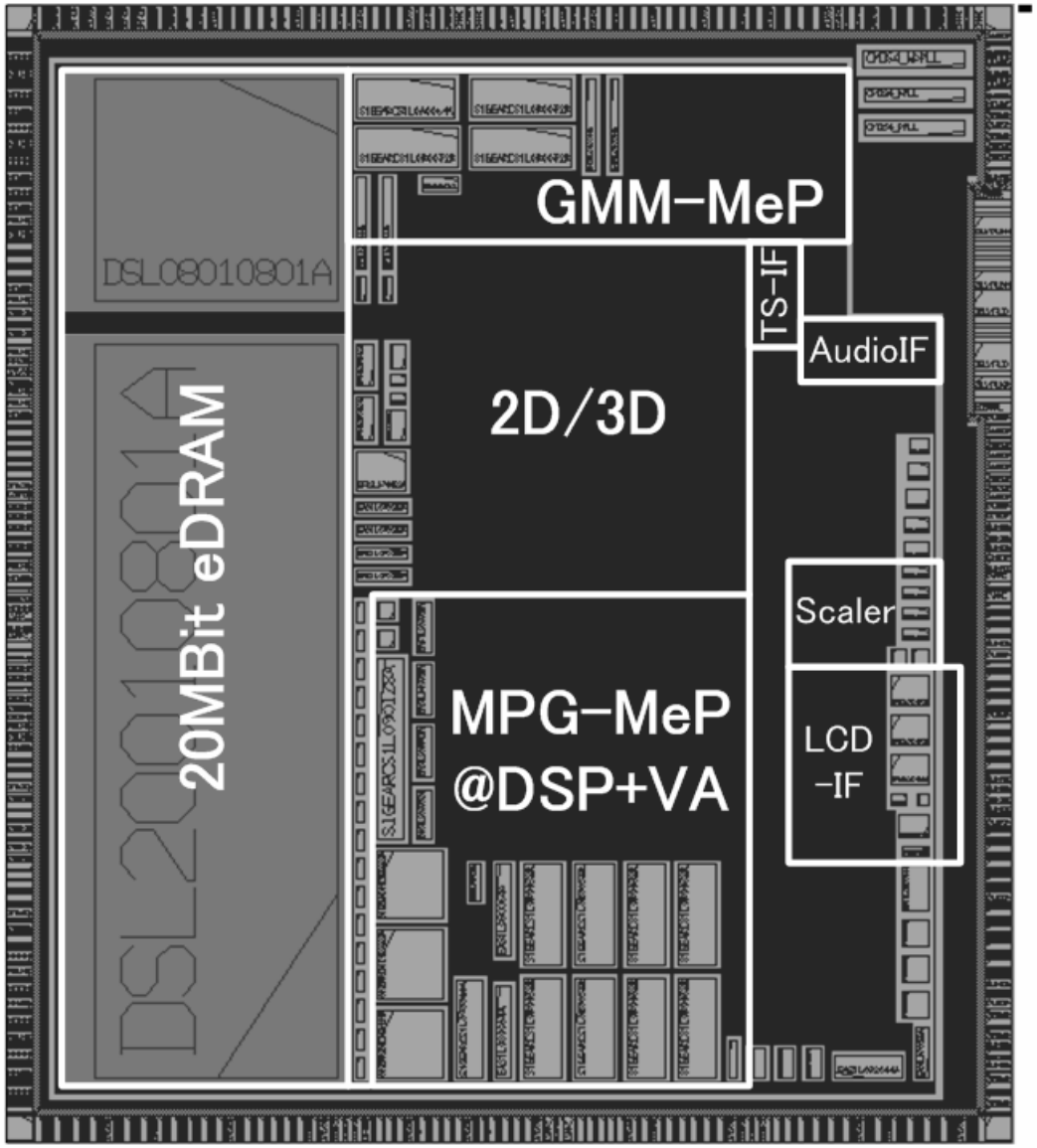
Block Diagram



ISDB-T 1-seg Data Flow



S1G Floor plan and Chip specification

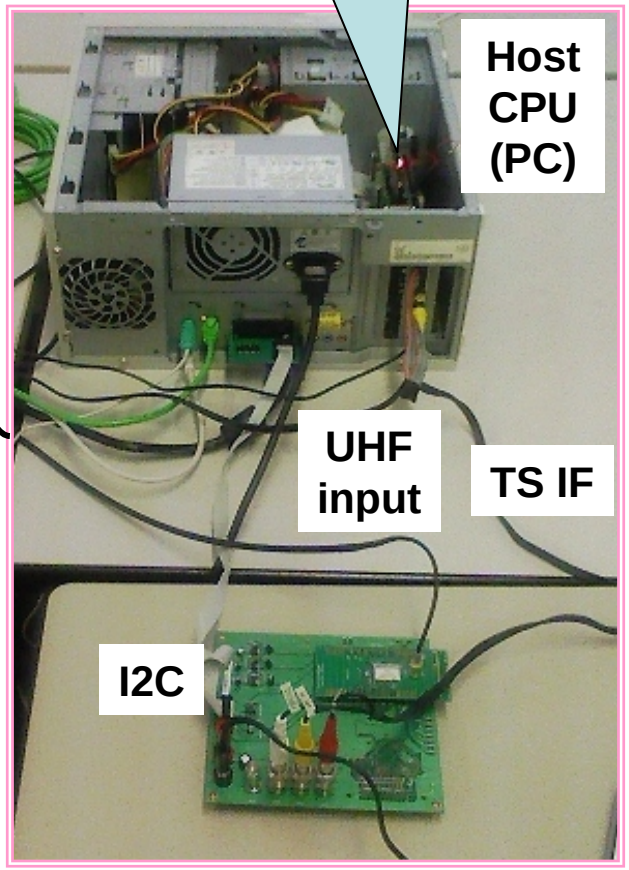


- **Technology**
  - Toshiba 90nm CMOS
  - 5 layer metal
  - Multi-Vth
  - Embedded DRAM
- **Package**
  - 289pin TFBGA
- **Logic Gate**
  - 2.7MGate
- **Memory**
  - SRAM 1.3Mbit
  - eDRAM 20Mbit
- **Supply Voltage**
  - 1.2V Core
  - 2.5V eDRAM
  - 1.8V/3.0V IO
- **Operation Frequency**
  - 162MHz

Evaluation Environment

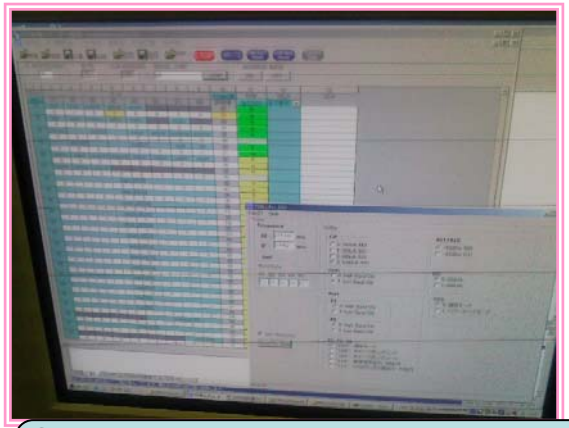
Power is measured by this environment. Not simulation

S1G PCI Board

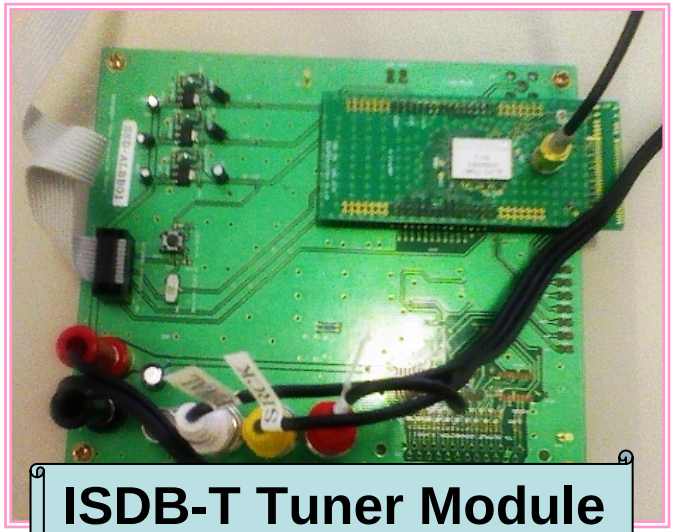


42mW ISDB-T 1-seg

ISDB-T Receiving picture

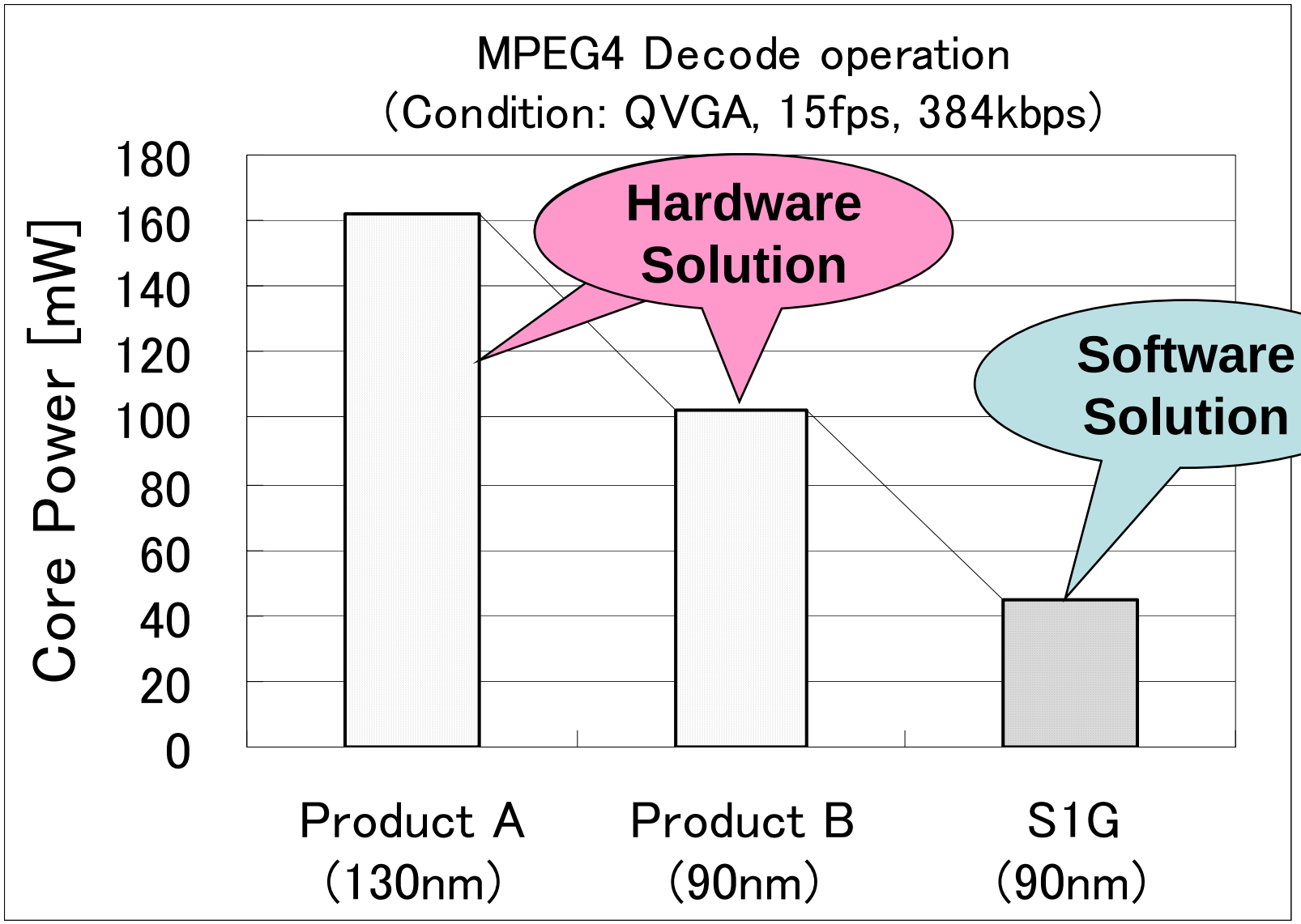


Control of ISDB-T Tuner Module by PC application

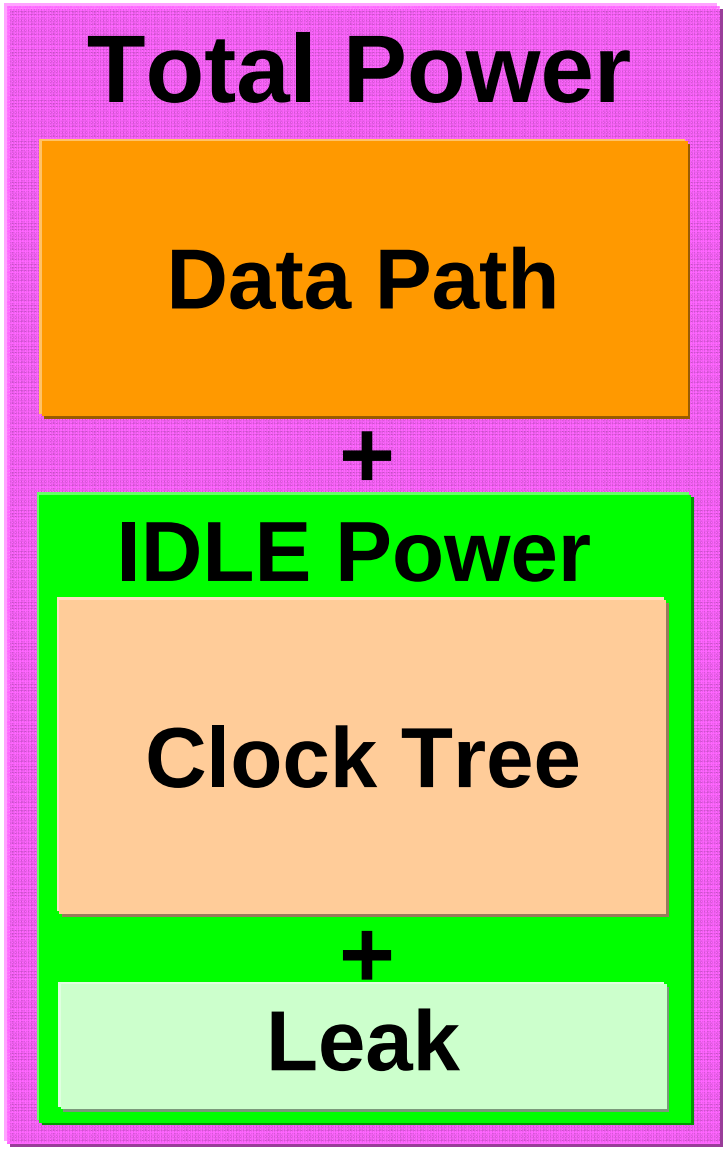


ISDB-T Tuner Module

Power Comparison



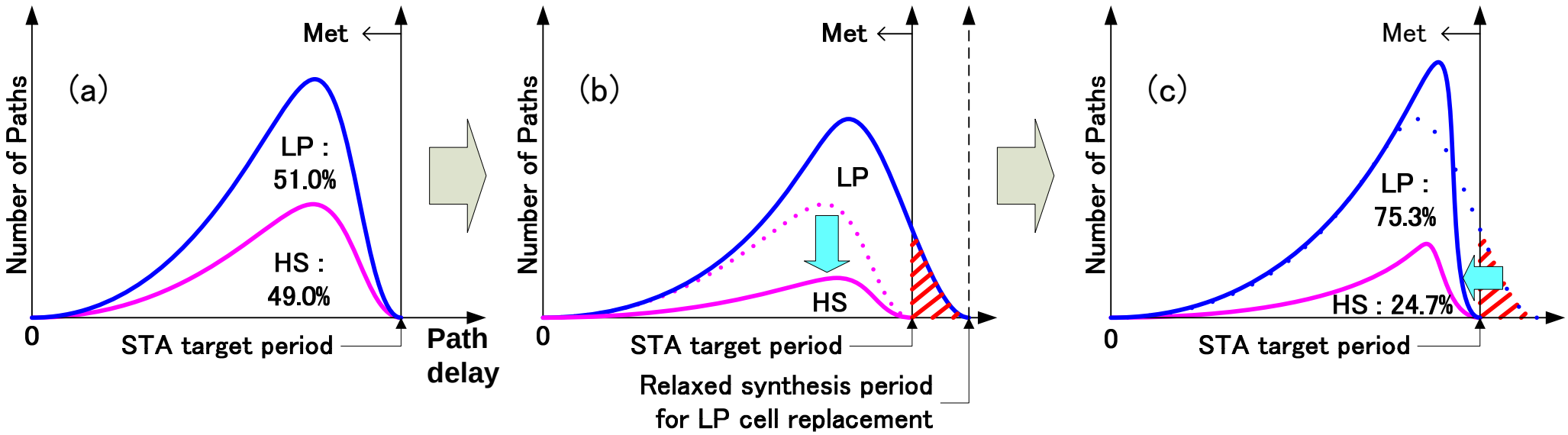
Breakdown of Power Consumption



Applied techniques for Low Power in S1G

- 90nm technology
- Low operation frequency
- Module level clock gating
- Clock gating by S/W control
- H/W Clock gating by Tool
- Multi-Vth Technique

Multi-Vth Technique for Low Leak Design



First achievement

HS ratio becomes low but timing violation occurs

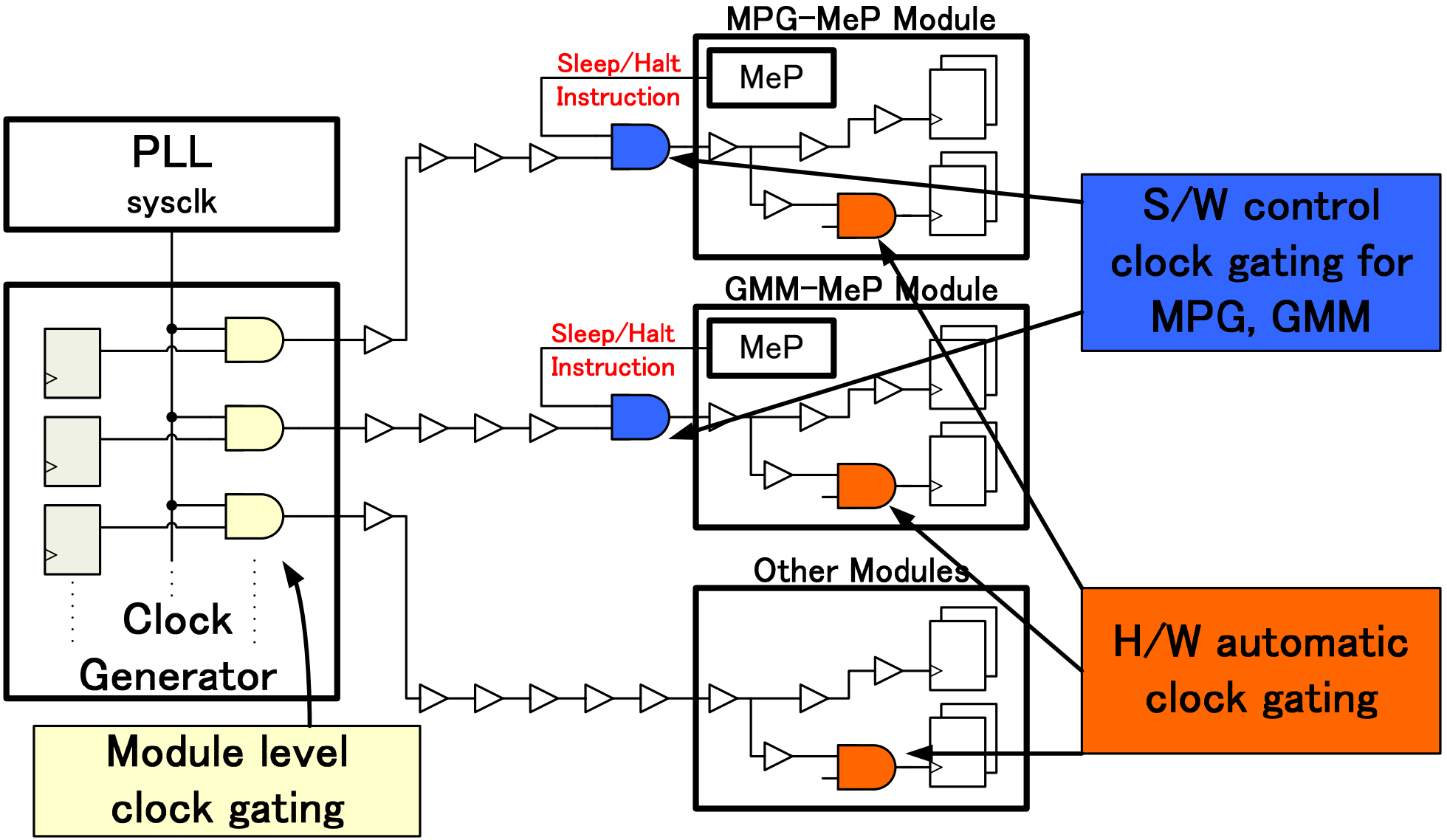
LP cells in violation paths replaced to HS cells again

LP: Low Power transistor (High Vth)

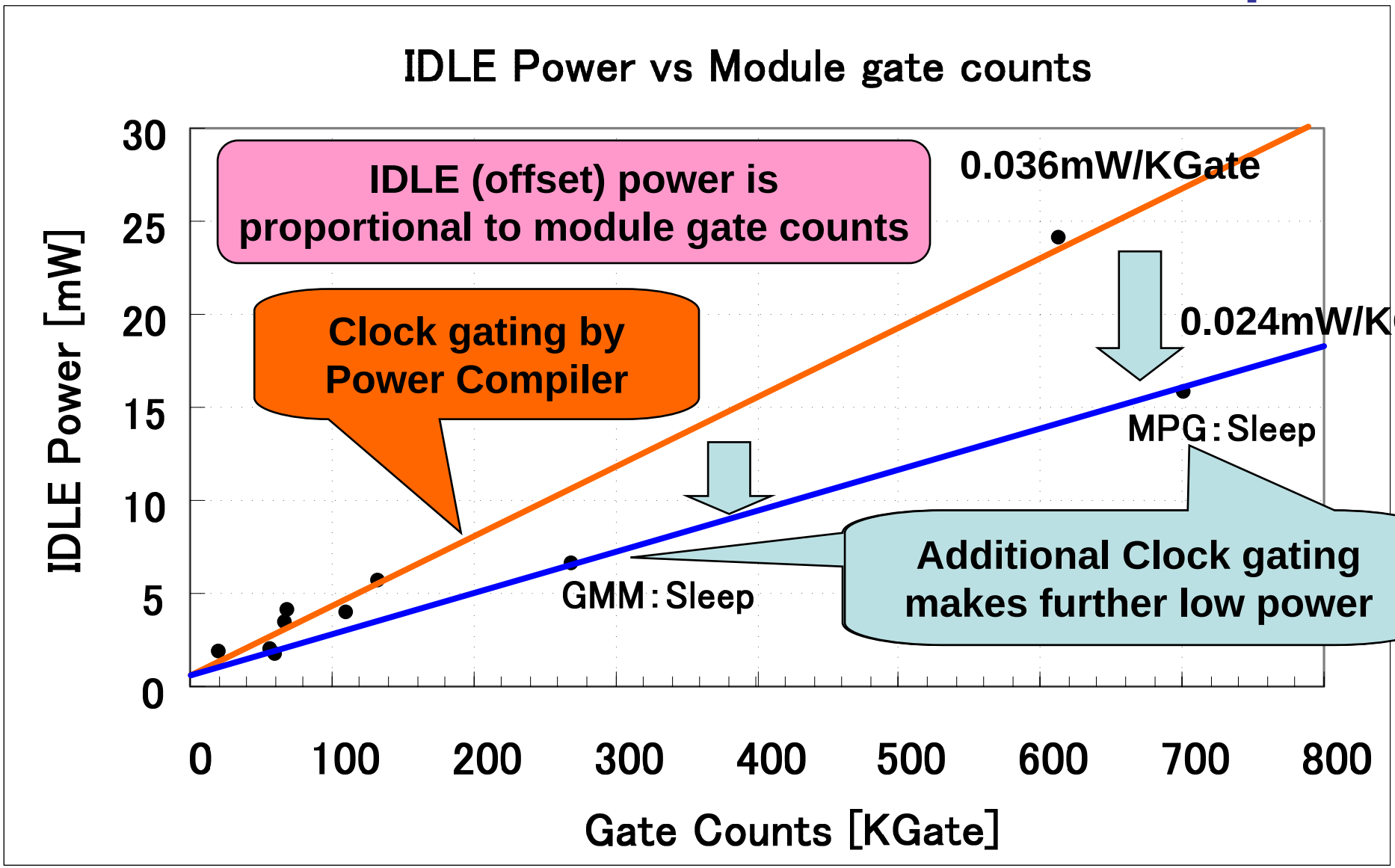
HS: High Speed transistor (Low Vth)

LP Replacement	LP ratio [%]	25℃		85℃	
		Leak Power [mW]	⊿ Leak [mW]	Leak Power [mW]	⊿ Leak [mW]
Before	51.0	1.99	0.59	13.44	4.79
After	75.3	1.39		8.65	

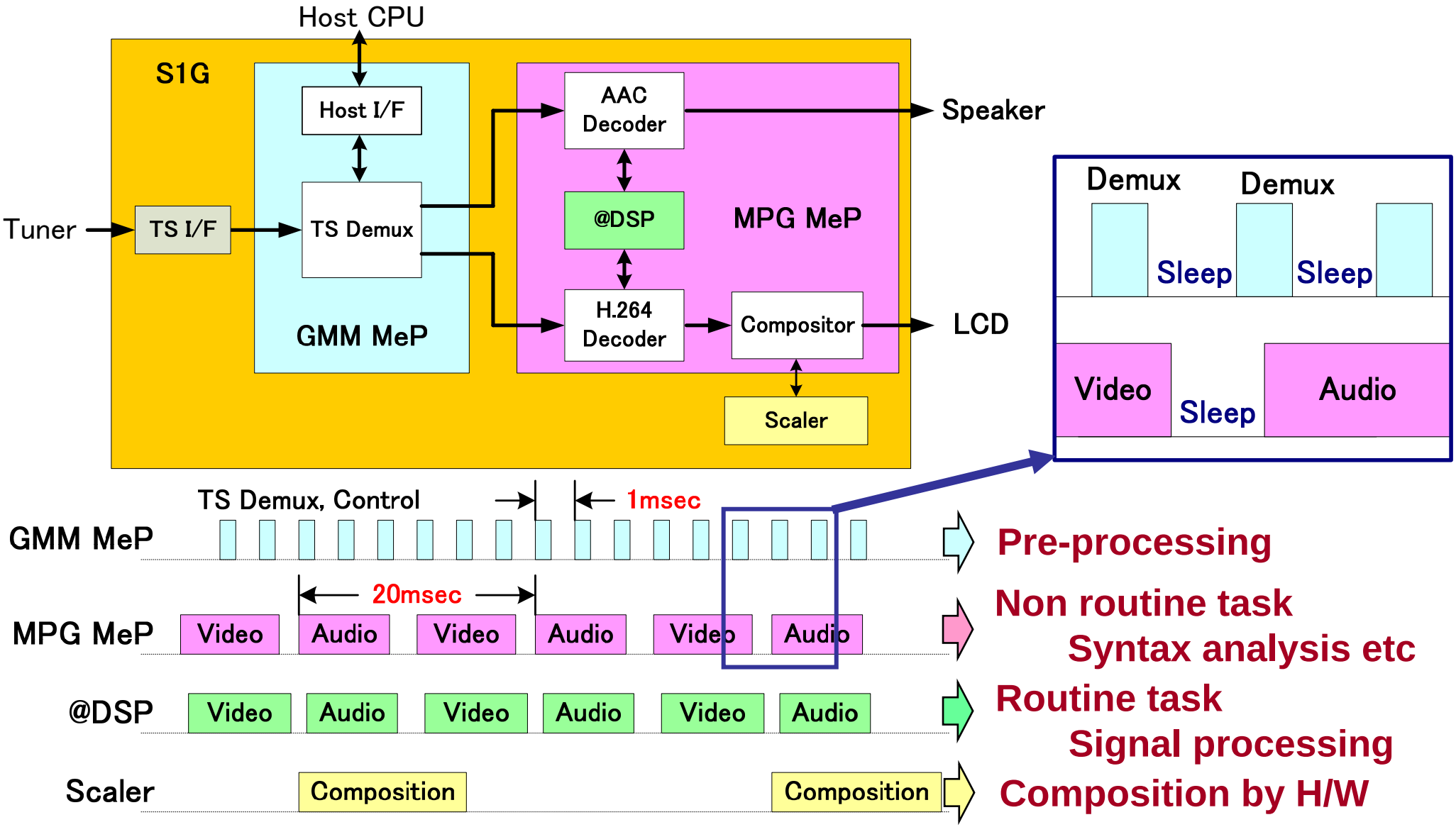
Clock Hierarchy in S1G



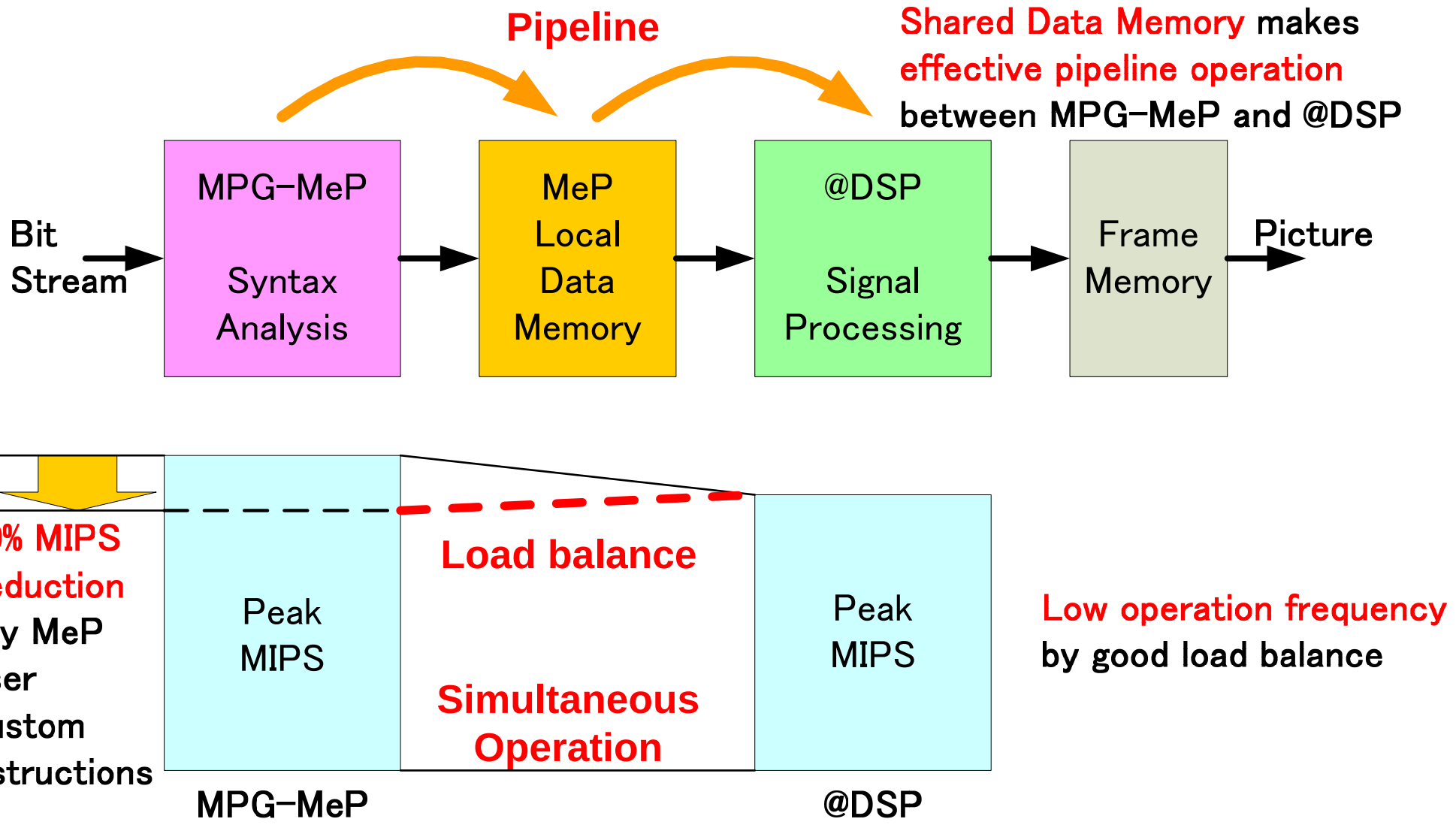
Relation between Gate counts and IDLE power



Software architecture

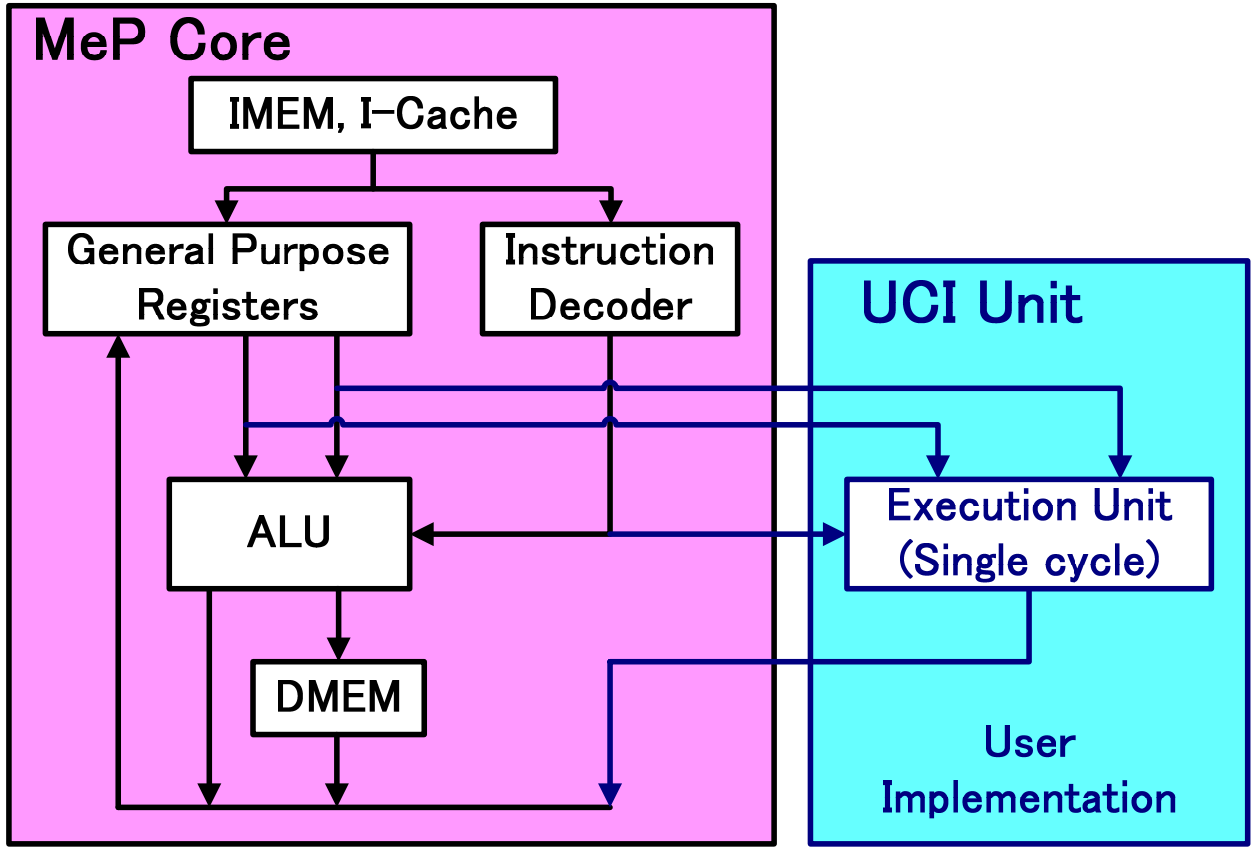


H.264 Decoder in MPG module



MeP User Custom Instruction

User can define and implement UCI to reduce operation MIPS of target application



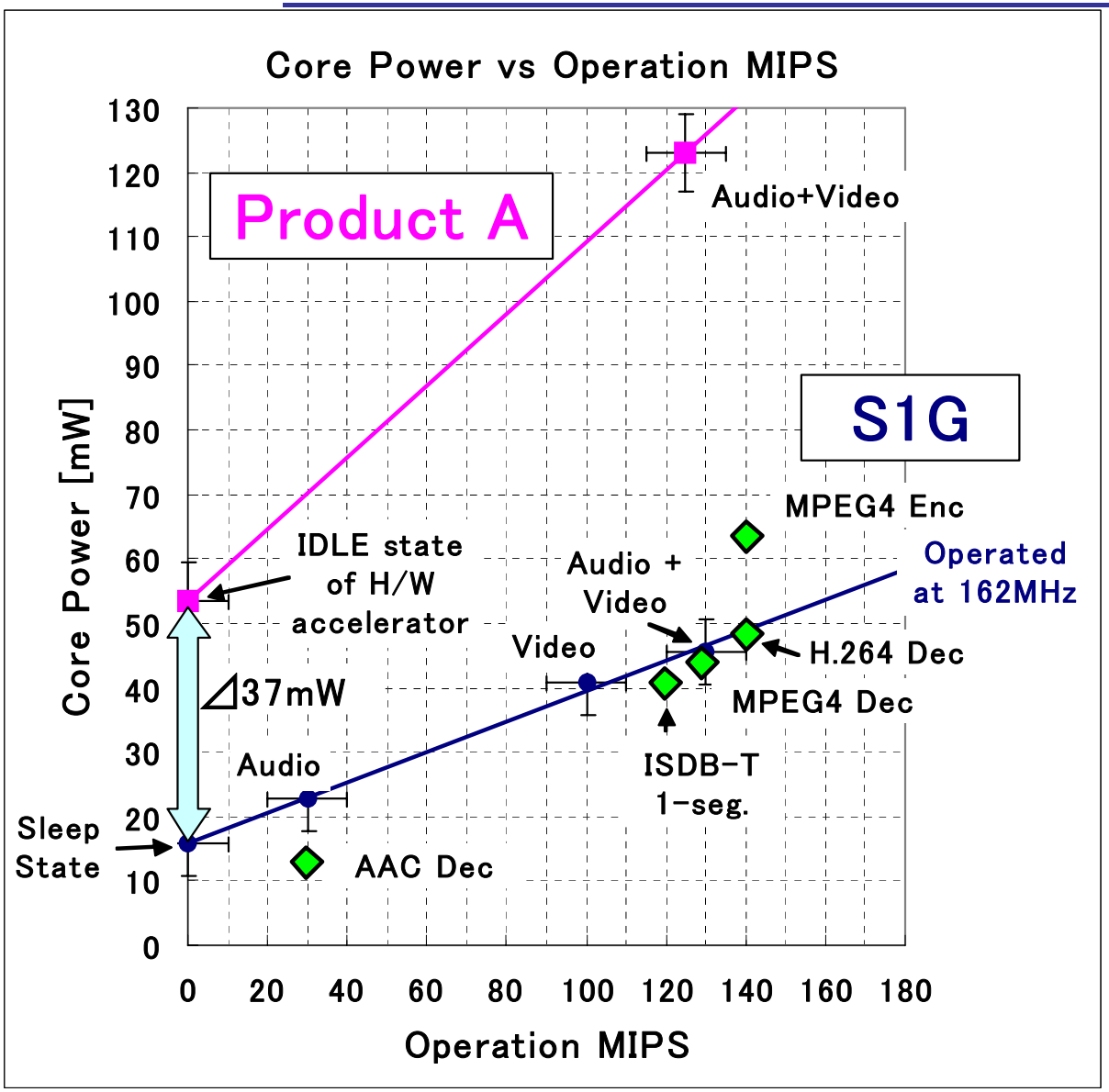
From profiling result of H.264 decoder,
1)Table search,
2)Bit manipulation
etc…
10 kinds of UCIs are implemented

10% MIPS Reduction

Summary of Application Power

Application	Video Condition				Audio Condition			Core Power [mW]
	Mode	Size [pxl*pxl]	Frame Rate [fps]	Bit Rate [Kbps]	Mode	Sampling Frequency [KHz]	Bit Rate [Kbps]	
ISDB-T 1-Seg.	H.264	320x180	15	214	AAC+SBR Stereo	48	32	42
H.264 Decode	H.264	320x240	15	384	AAC Stereo	44.1	32	49
MPEG4 Encode	MPEG4	320x240	15	384	AMR-NB	8	12.2	63
MPEG4 Decode	MPEG4	320x240	15	384	-	-	-	45
AAC Decode	-	-	-	-	AAC Stereo	48	128	13

Relation between MIPS and Power



P = DataPath + IDLE

P: Total Core Power

DataPath: Actual operation power (Frequency x Slope)

IDLE: IDLE Power (Sysclk is provided)

Summary

- Multi-Vth technique is effective for low leak design
- Additional clock gating by sleep instruction of MeP processor realizes lower IDLE power
- RUN and IDLE control in fine grain by S/W is effective for low power operation
- Good load balance between processors leads low operation frequency

We have accomplished low power ISDB-T One-segment in 42mW.