Simultaneous Control of Subthreshold and Gate Leakage Current in Nanometer-Scale CMOS Circuits

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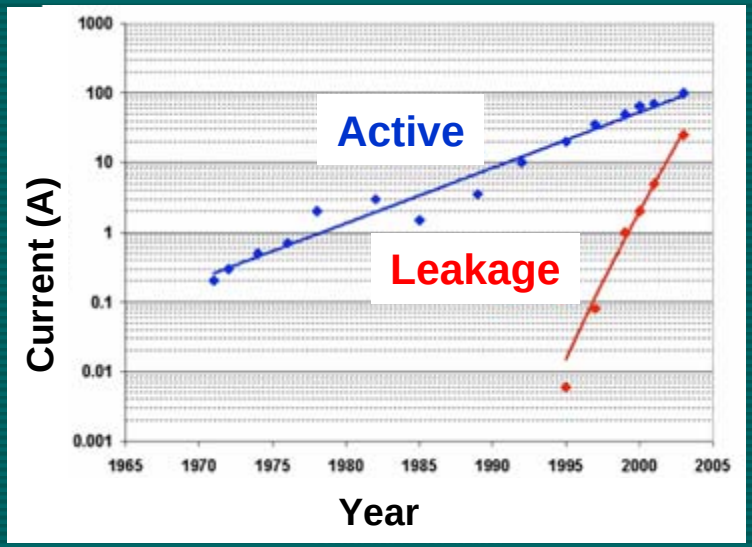
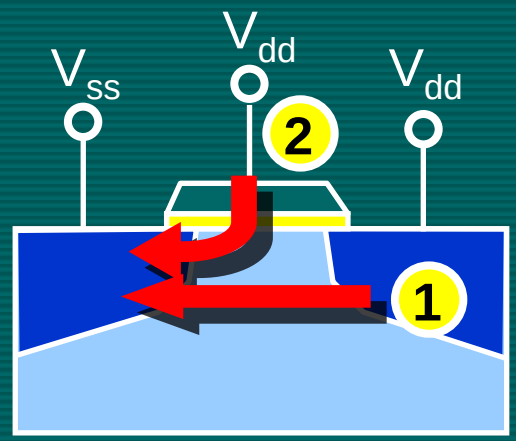
Outline

- Introduction: leakage current, power gating
- Supply switching with ground collapse (SSGC)
- Implementation of SSGC
- Experimental results
- Summary

Leakage Current

- Leakage current in nanometer regime
  - Exponential growth of leakage
    - Subthreshold leakage due to reduced V_{th} (1)
    - Gate leakage due to reduced T_{ox} (2)

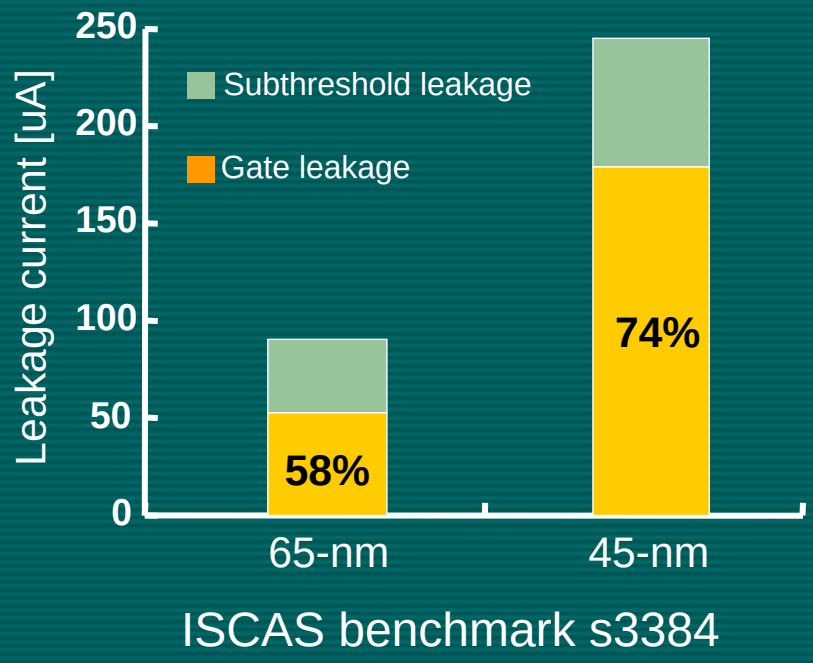




http://www.intel.com/technology/itj/2005/volume09issue04/art01_advpackagetech/p04_techtrends.htm

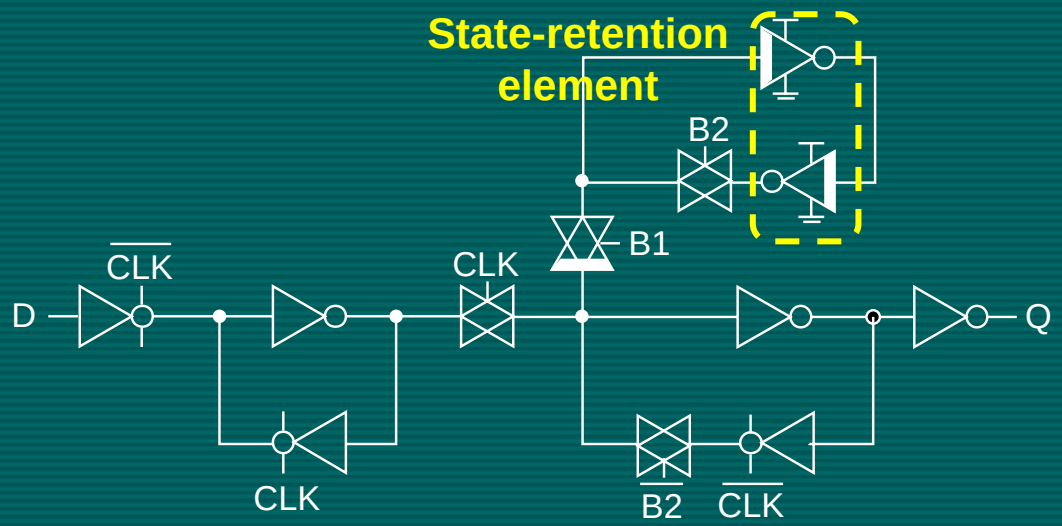
Leakage Current

- **Gate leakage current**
  - Grow faster than subthreshold leakage
  - May dictate the total leakage in future technology

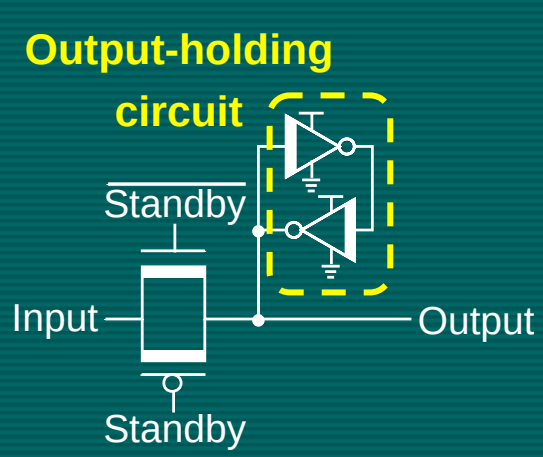


Power Gating

- Power gating
  - Widely used to suppress subthreshold leakage
  - Active mode: footer turned-on
  - Standby mode: footer cuts off power rail

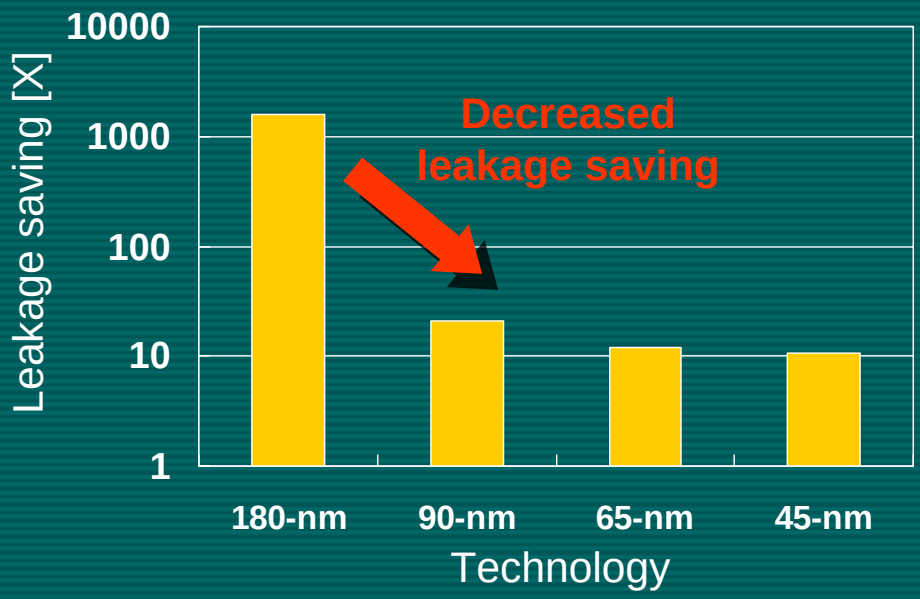


Balloon circuit [Schigematsu-JSSC-1997]



Power Gating

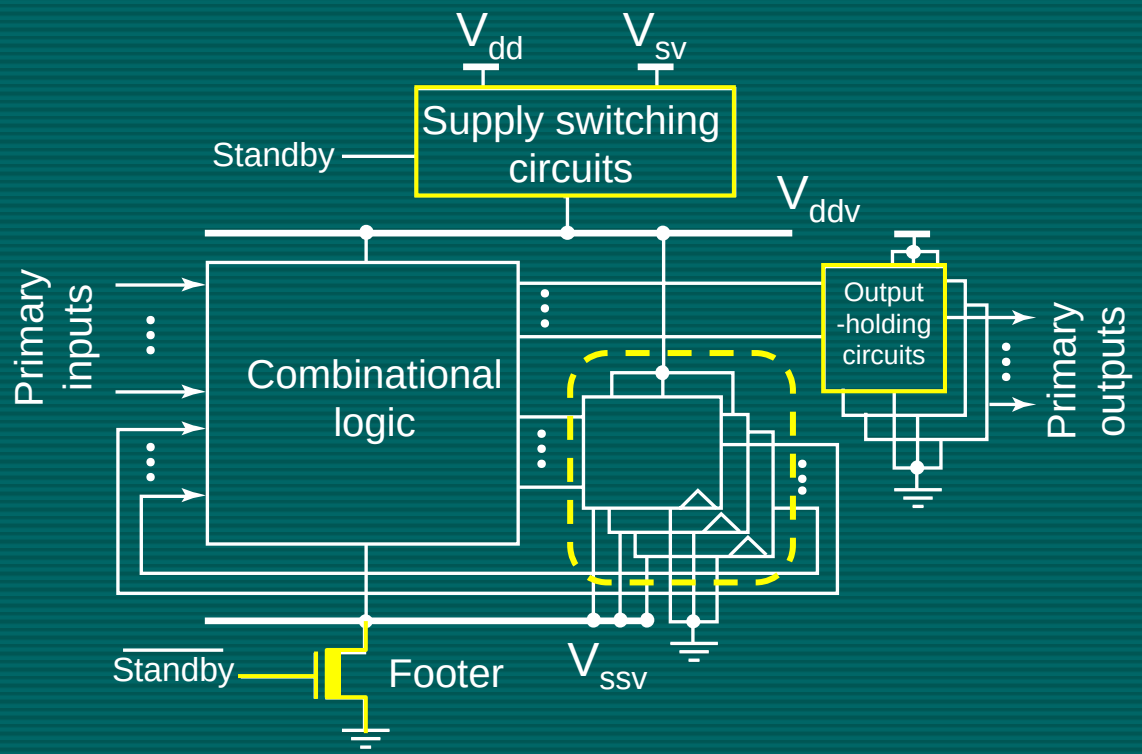
- Power gating in nanometer regime
  - State-retention and output-holding circuit leak gate leakage
  - Leakage saving from power gating greatly reduced



ISCAS benchmark s1269 w/ power gating

Supply Switching with Ground Collapse

- SSGC: supply control + power gating



Active

Supply switching circuits: V_{dd}

Footer: on

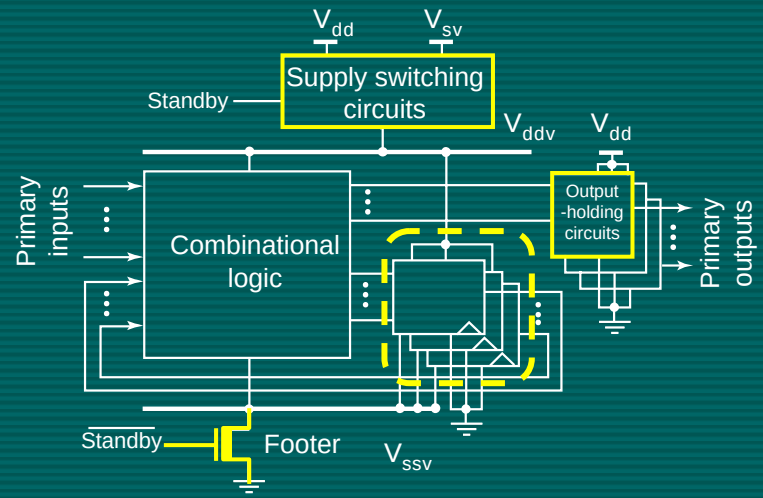
Standby

Supply switching circuits: V_{sv} ($<V_{dd}$)

Footer: off

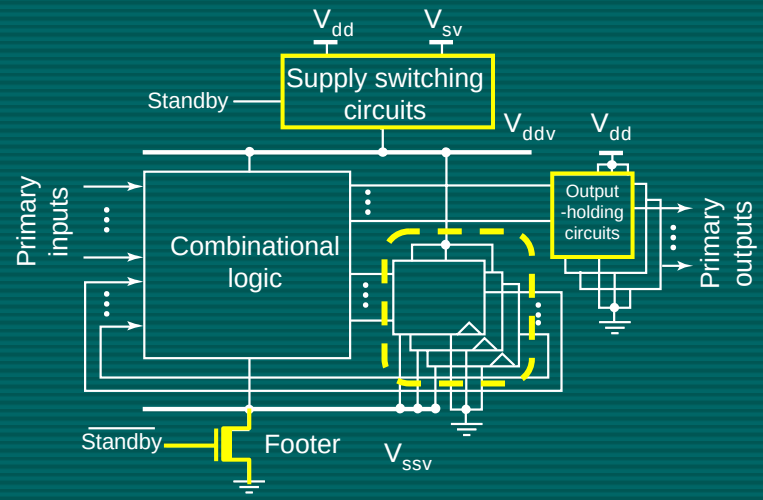
Supply Switching with Ground Collapse

- SSGC circuit
  - Reduce leakage of combinational logic through power gating (ground collapse)
  - Reduce leakage of FF through lowered voltage (supply switching) and power gating
  - No need to use state-retention FF



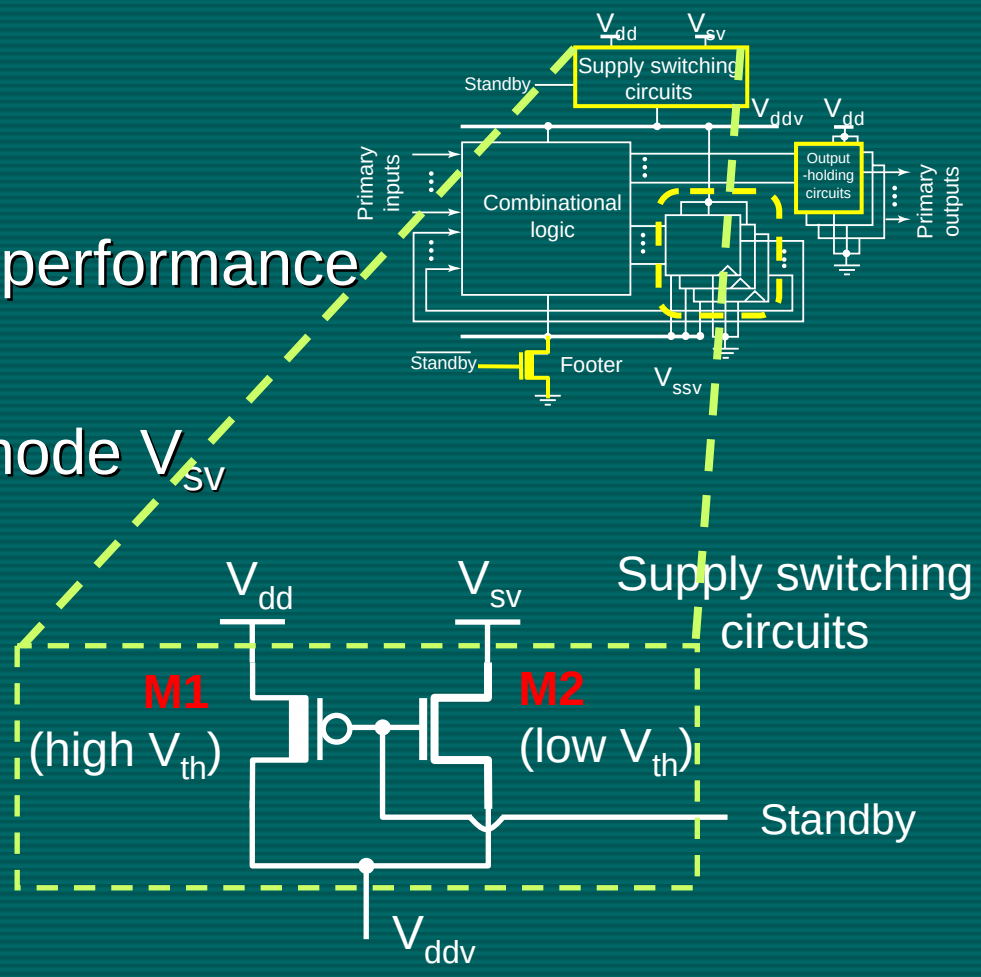
Supply Switching with Ground Collapse

- Implementation of SSGC
  - Design of supply switching circuits
  - Physical design
    - Power networks
    - SSGC flip-flop
    - Footer
    - Output-holding circuit



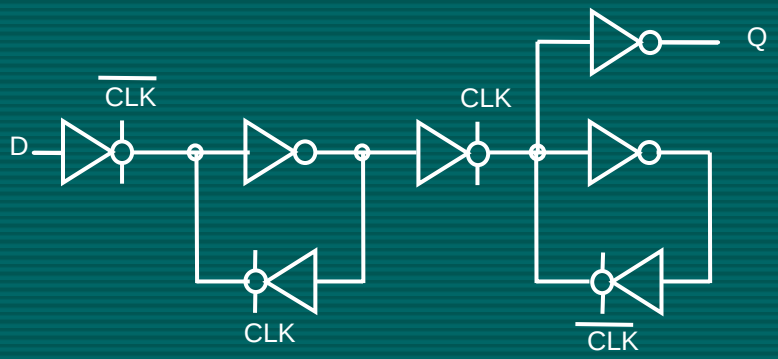
Supply Switching Circuits

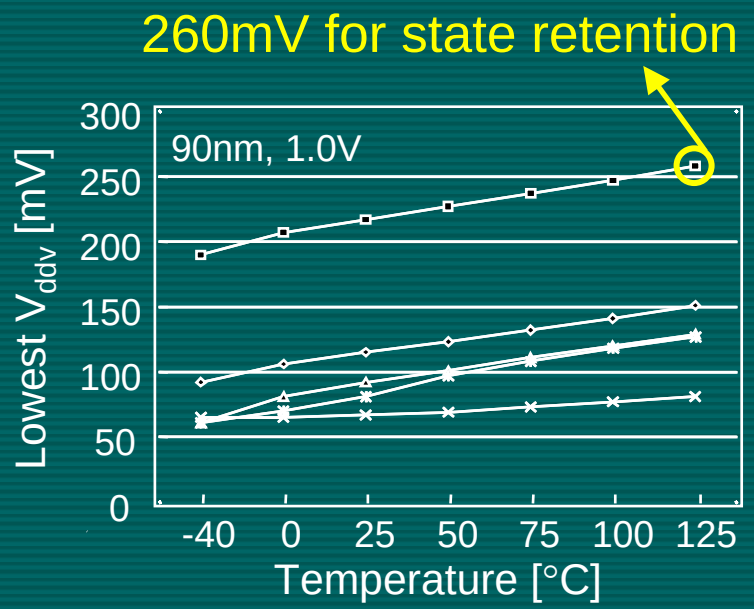
- M1 switch
  - Supplying active V_{dd}
  - High V_{th} PMOS
  - Sizing affects circuit performance
- M2 switch
  - Supplying standby-mode V_{sv}
  - Low V_{th} NMOS



Supply Switching Circuits

- V_{ddv} in standby
  - Bounded by the potential to retain states in FFs + noise margin
  - Factors: temperature, process variation, states (0 or 1), FF types

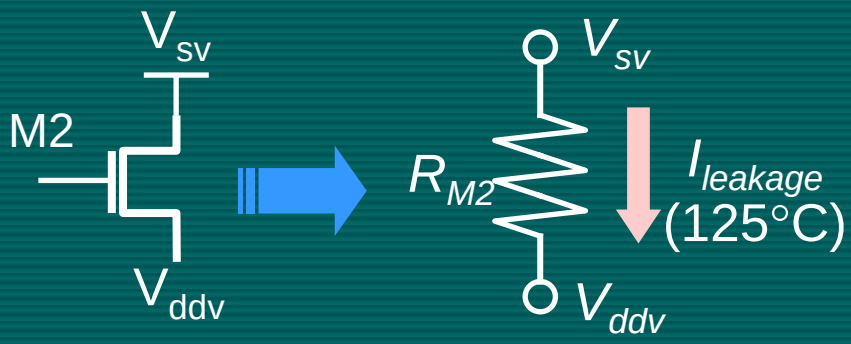




Supply Switching Circuits

- Design of M2 switch
  - Selection of M2 size and V_{sv} for
    - Efficient leakage saving
    - Lowest V_{ddv} (e.g. 260mV)
  - Voltage drop across M2 dictates V_{sv}

M2 size and V_{sv}



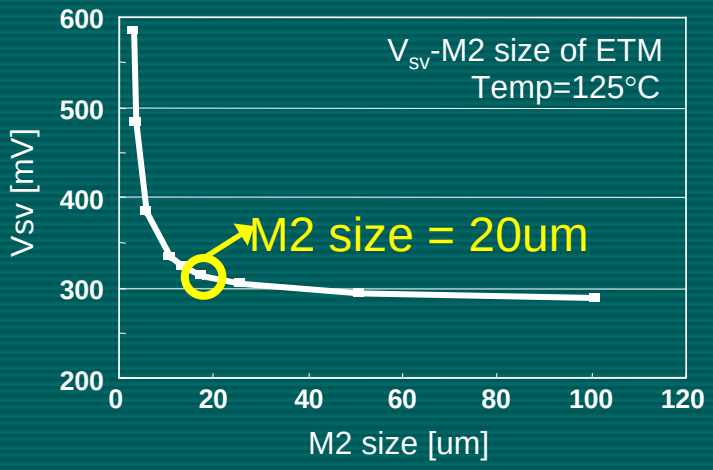
$$V_{sv} = V_{ddv} + I_{leakage} \times R_{M2}$$

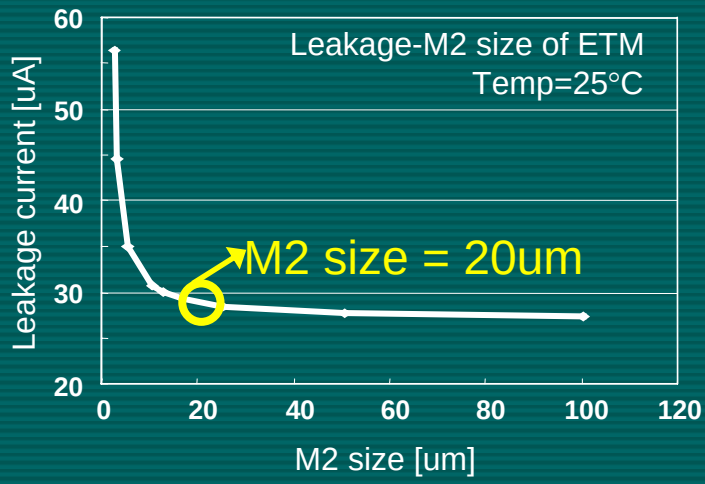
$$R_{M2} = \frac{R_{min}}{M2\ size}$$

Supply Switching Circuits

- Design of M2 switch
  - M2 size vs. V_{sv}
    - Trade-off between area overhead and leakage power

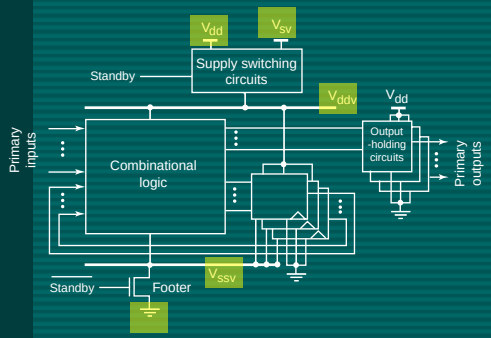
$$V_{sv} = V_{ddv} + I_{leakage} \times \frac{R_{min}}{M2\ size}$$

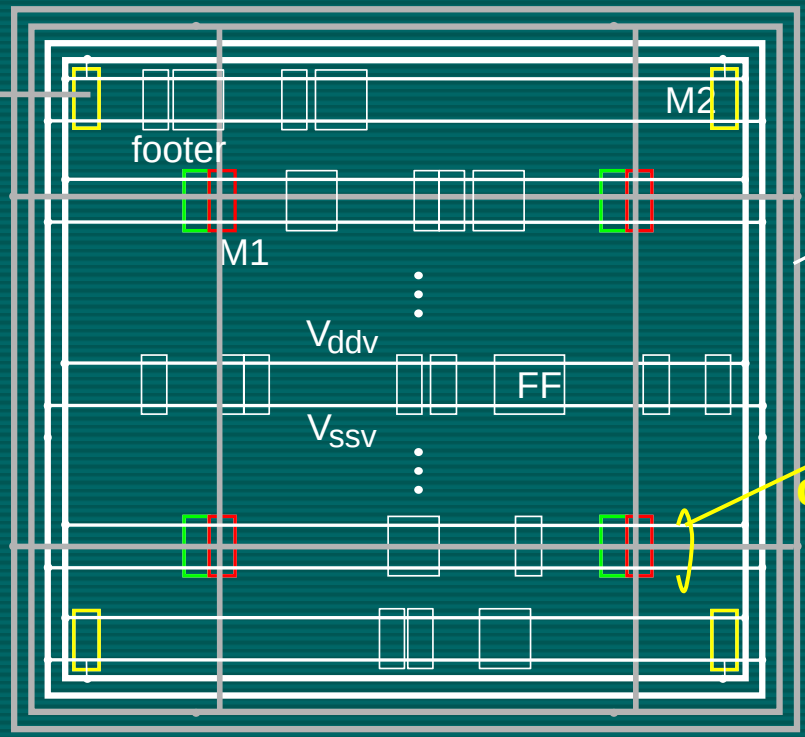




Physical Design of SSGC

- Power networks for SSGC
  - Conventional V_{dd} and V_{ss} rails as V_{ddv} and V_{ssv} rails





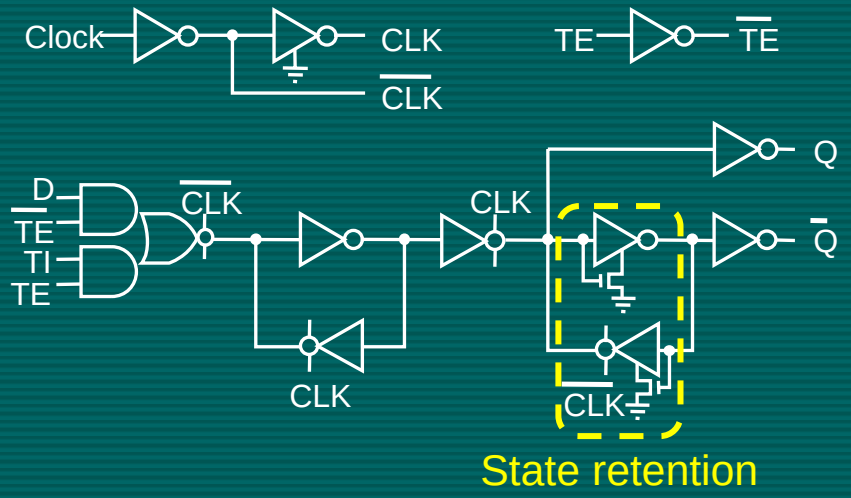
V_{dd}: vertical rails

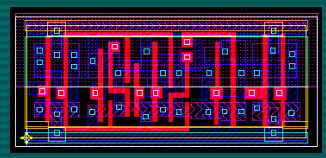
V_{ss}: horizontal rails

V_{ddv} and V_{ssv} rails for combinational logic cells

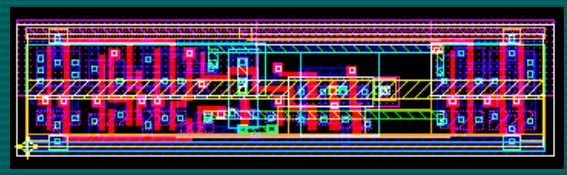
Physical Design of SSGC

- SSGC flip-flop
  - State maintained in slave latch with low V_{sv}
    - No need of state-retention element
    - Low gate and subthreshold leakage current
      - Other parts are power gated for further reduction

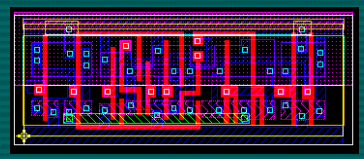




Conventional flip-flop



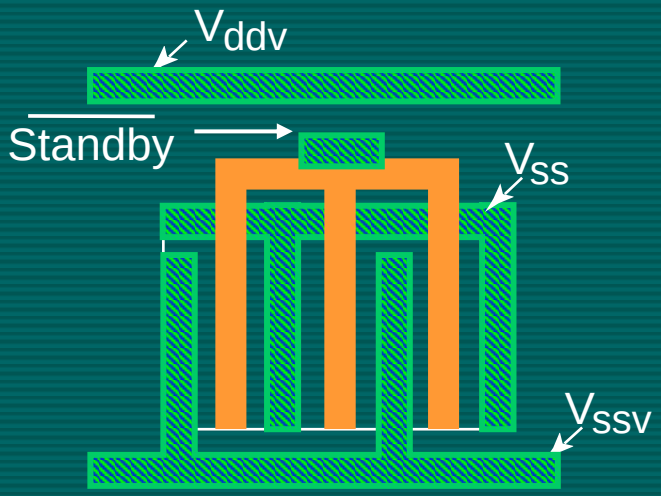
PG flip-flop

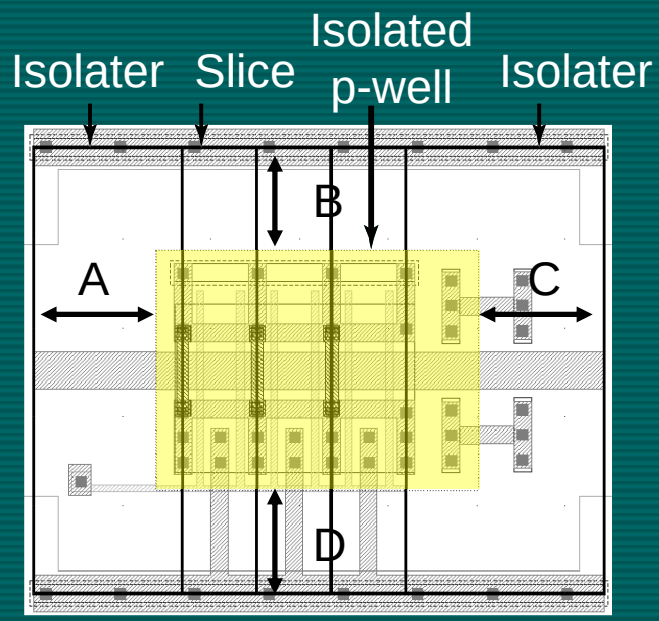


SSGC flip-flop (16% increase)

Physical Design of SSGC

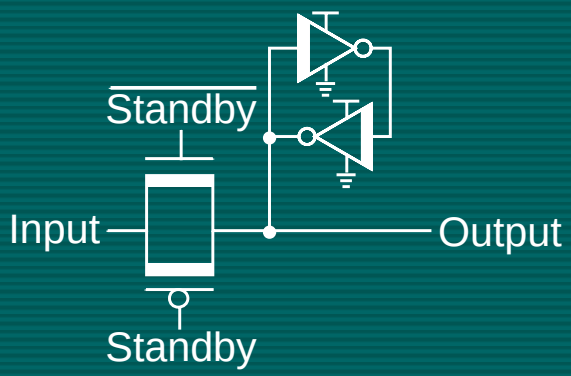
- Footer layout
  - Isolated body (body bias to V_{ss}) preferred for leakage current → area overhead due to well isolation
  - Building block-based approach: flexible placement, control of area overhead

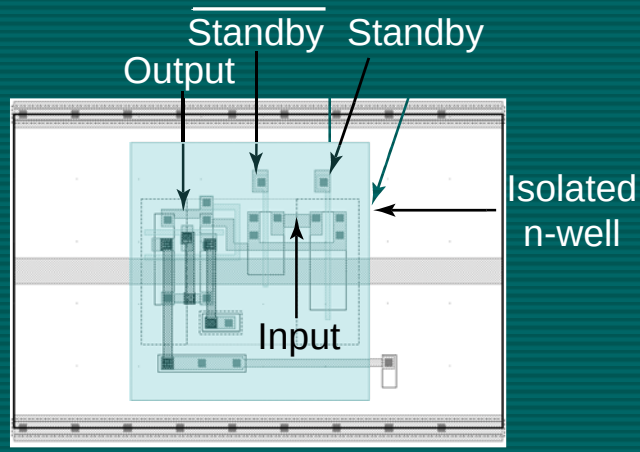




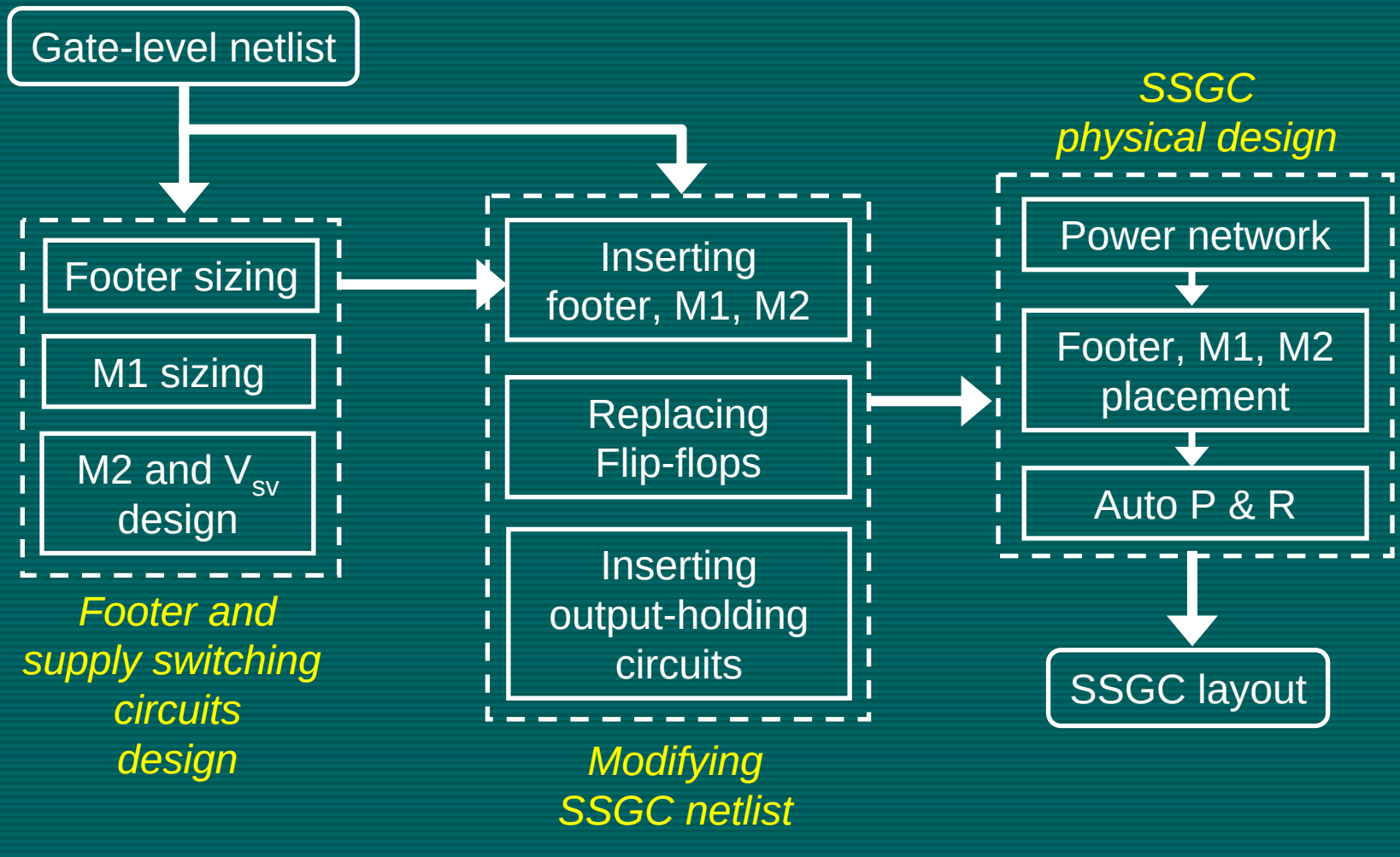
Physical Design of SSGC

- Output-holding circuit
  - Output-holding circuits are needed due to V_{sv}(<V_{dd}) in standby
  - Utilize high V_{th} to reduce subthreshold leakage



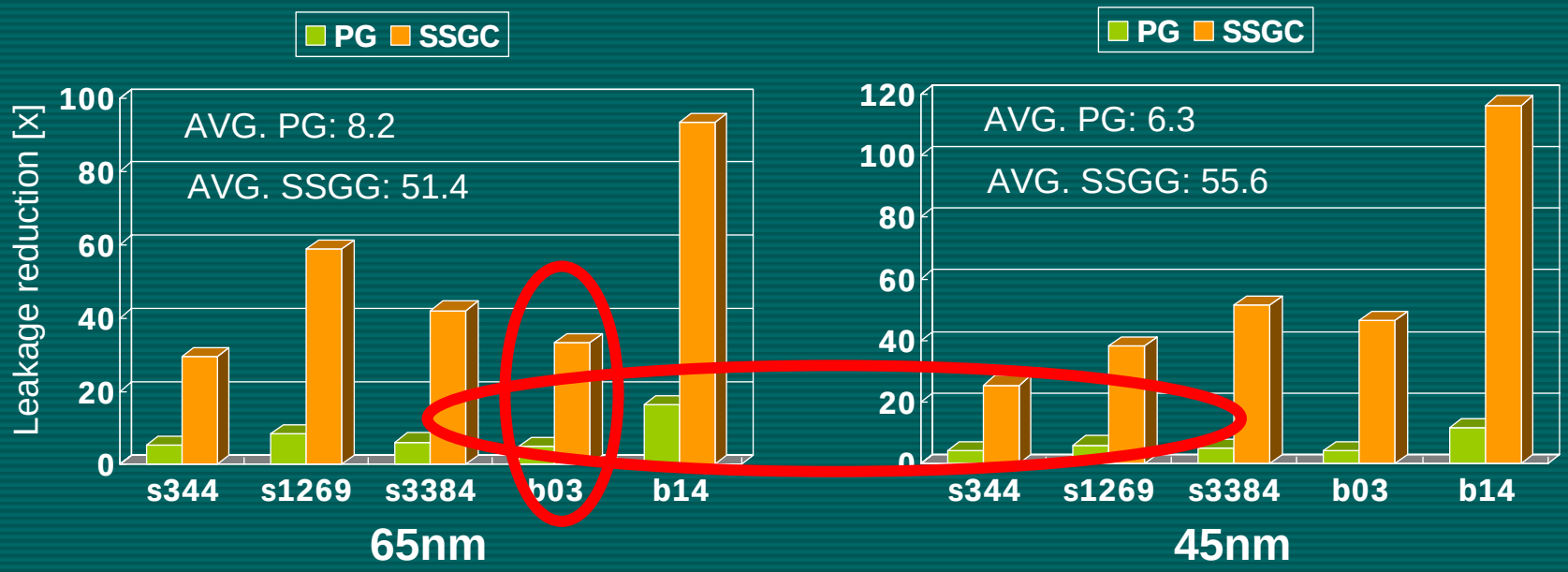


SSGC Design Flow



Experimental Results

- Test circuits
  - ISCAS and ITC benchmark circuits
  - 65- and 45-nm predictive models

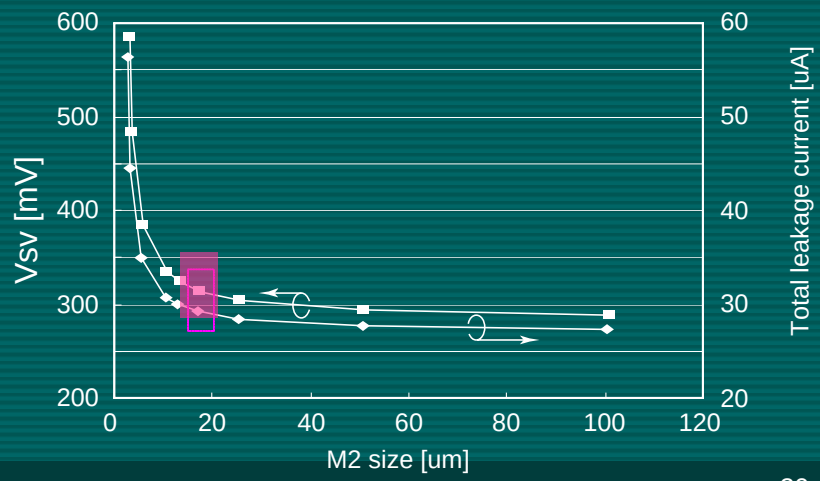


Case Study: ETM

- Embedded Trace Macrocell (ETM)
  - Debugging and tracing core for ARM
  - 90nm, 1.0V commercial process

I / Os	SEs	Gates	Leakage
320 / 124	**5,501**	**90,068**	**410uA**

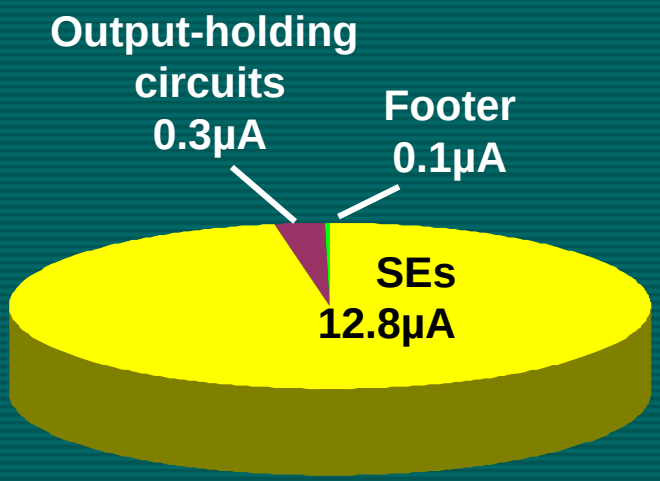
- Footer, M1, and M2 sizing
  - M1 and footer sizing for 10% delay increase
  - M2 sizing to optimize leakage at room temperature

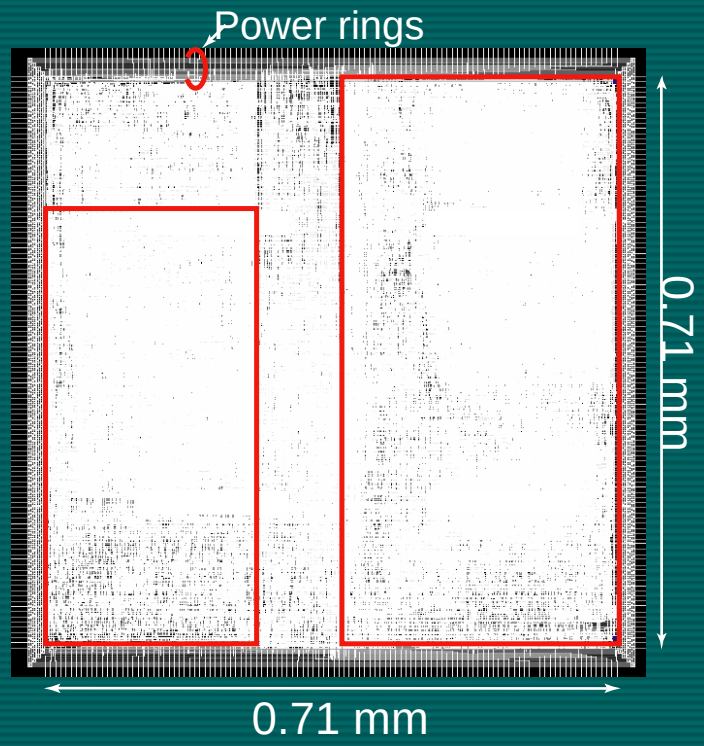


Case Study: ETM

- SSGC implementation result
  - Total leakage saving: 32× at 25°C
  - Area increase: 3%
  - Wirelength increase: 6%

Leakage current breakdown





Summary

- Power gating
  - Widely used to suppress subthreshold leakage
  - NOT efficient in nanometer technology due to gate leakage of storage elements and output-holding circuits
- Supply switching with ground collapse
  - Overcomes the limitation of power gating
  - Demonstrates cell-based semicustom design flow based on SSGC