Logic and Layout Aware Voltage Island Generation for Low Power Design

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Outline

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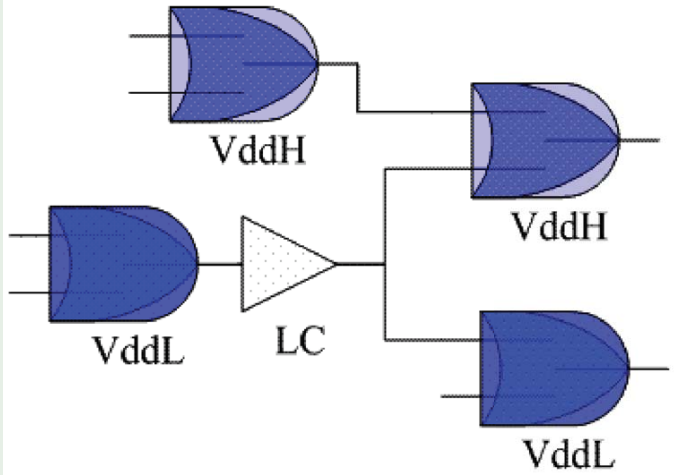
Overview of Dual Supply Voltage Design

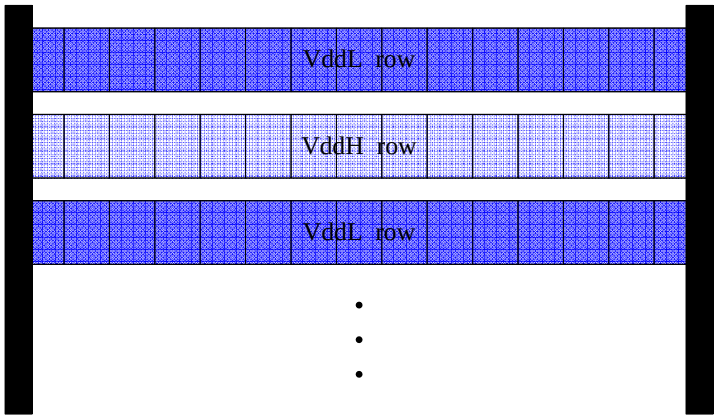
- Dual supply voltage design.
  - reduce power without degrading performance
- Level converter.
- Voltage assignment algorithms based on logic level.
  - CVS
  - ECVS
  - ...

Example

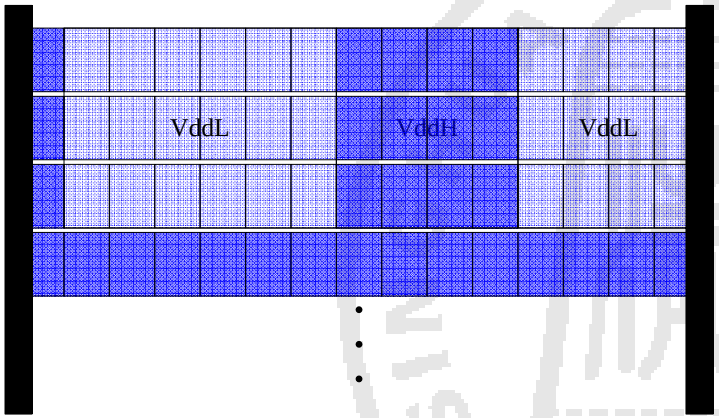


Two Design Styles.

- Physical overheads increase significantly in both 'row based' and 'region based' design style.



(a) row based



(b) region based

Outline

Ralated Work

Three very recent works introduce physical boundaries in voltage partition to generate voltage islands.

- H. Wu, Postplacement Voltage Island Generation ... in Proc. ICCAD'05.
- Royce L.S. Ching, Post-Placement Voltage Island Generation, in Proc. ICCAD'06
- Bin Liu, Power Driven Placement, in Proc. ASP-DAC'06.

Motivation

- Logical or physical boundaries have their own disadvantages:
  - logical boundaries: hard to generate voltage islands
  - physical boundaries: a lot of LCs needed to be inserted
- The objective of this work is to generate voltage islands without increasing the number of level converters.

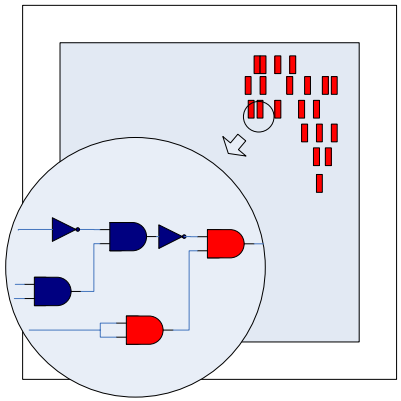


Figure: Logical boundaries

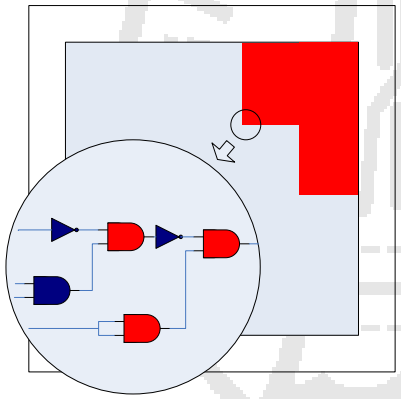


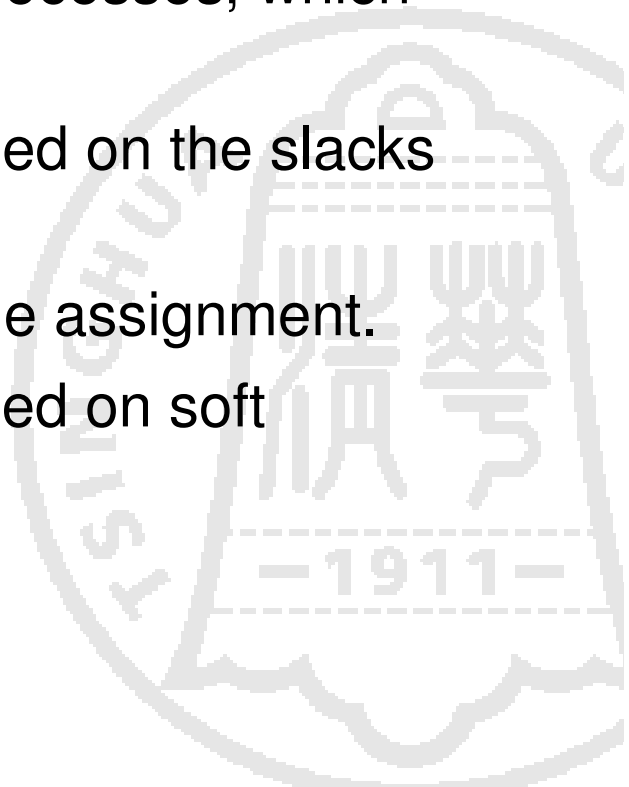
Figure: Physical boundaries

Outline

Main Processes of Voltage Island Generation.

The methodology consists of three primary processes, which could be called many times.

- **Process 1** Initial voltage assignment based on the slacks of the circuit nodes.
- **Process 2** Logic and layout aware voltage assignment.
- **Process 3** Voltage island generation based on soft clustering.



Voltage Island Generation Methodology

The voltage island generation algorithm is established upon a partition based placement platform.

Voltage Island Generation Methodology

while (!done)
  if $(m > m_t)$
    traditional placement process;
  end if
  if $(m = m_t)$
    Process 1; Process 2; Process 3;
  end if
  if $(m < m_t)$
    Process 2; Process 3;
  end if
end while

Outline

Process 1: Initial Voltage Assignment

- The objective of initial voltage assignment is to identify the cells which tend to operate at V_{ddL}.
- It is derived from an existing voltage assignment algorithm based on logic level. The key points of the initial voltage assignment algorithm:
  - The sensitive transitive closure graph $G_s = (V, E_s)$
  - The heuristic measure

$$tendency(v) = \frac{\Delta power}{\Delta delay \cdot N_n(v)} \quad (1)$$

Outline

Process 2: Heuristic Measure for Reducing the Number of LCs

- $Snk(e), e \in E$: the set of sink nodes of super edge e
- $s_e \in V$: source node of edge e
- x_v is a boolean variable indicating the voltage assignment of node v
- $LC(e)$: level converter assignment on edge e
- The expectation of $LC(e)$ could be expressed as follows:

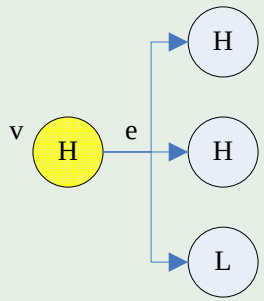
$$E(LC(e)) = 1 \cdot P(x_{s_e} = 0)(1 - \prod_{v \in Snk(e)} P(x_v = 0)) \quad (2)$$

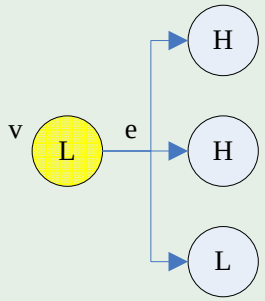
Process 2: Heuristic Measure for Reducing the Number of LCs

If we modify the supply voltage of node v, the possible level converter reduction on edge e (v is a source or sink node of e) can be obtained by calculating $E(LC(e))$ on the condition that v operates at the other voltage.

Example

if v is a source node for edge e and the voltage of v is modified from V_{ddH} to V_{ddL}, $E(LC(e))$ changes from 0 to $1-(1-p)^2p$.[a]





[a] p is the possibility for v to keep the current voltage

Process 2: Heuristic Measure for Reducing the Number of LCs

The reduction of $E(LC(e))$ when v is flipped can be expressed as follows:

$$\Delta E(LC(e)) = E(LC(e)|x_v) - E(LC(e)|\overline{x_v}) \quad (3)$$

This model has some good properties:

- $\Delta E(LC(e)) \geq 0$ when one sink is modified from V_{ddH} to V_{ddL} but some other sinks of e are still V_{ddH} (the source is V_{ddL}).
- $\Delta E(LC(e))$ is larger when the source node modified (from V_{ddL} to V_{ddH}) has more V_{ddL} sinks.

Process 2: Constrained Logic and Layout Aware Voltage Assignment

To evaluate the impact of any modification, we define the profit for a cell v as follows:

$$profit(v) = (\Delta ELC(v) + \alpha) \cdot N_v \quad (4)$$

- α is used to allow a modification with negative $\Delta ELC(v)$, thus opening possibility of uncovering better solutions.
- N_v is the number of cells with the other supply voltage in the v's bin.

$\Delta ELC(v)$ provides us the candidates of voltage modifications that decrease or keep the number of LCs and N_v gives a priority to every candidate that the modification of making a bin contain purely V_{ddl} or V_{ddh} cells can first be selected.

Process 2: Constrained Logic and Layout Aware Voltage Assignment

Constrained Logic and Layout Aware Voltage Assignment Algorithm

Require: voltage-scaled solution

calculate profit for all nodes

while (*profit* $>$ 0 and the modification does not violate timing or power constraint)

choose the gate with the maximum profit;

make the modification;

update the delay, slack;

update the profits for nodes in the vicinity;

end while

Outline

Process 3: Soft Clustering

The clustering technique helps to generate voltage islands. An effective method to cluster specific cells is adding pseudo hyperedges connecting the cells (referred to as soft clustering).

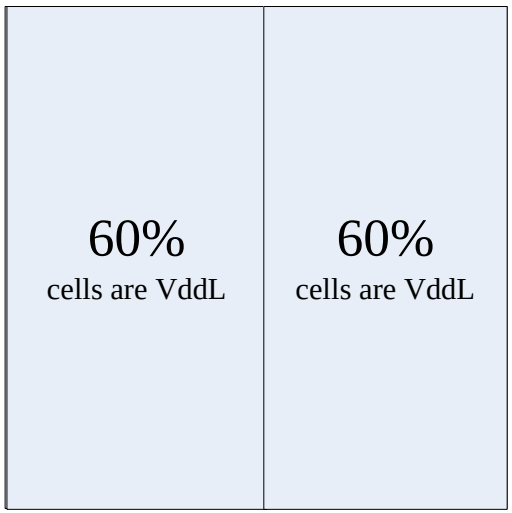


Figure: Partition without clustering.

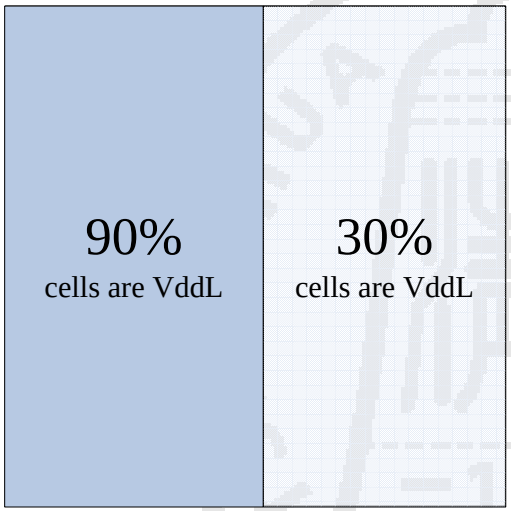


Figure: Partition with clustering.

Process 3: Soft Clustering

Add pseudo edges connecting the cells that tend to be placed together to reduce the negative impact to traditional placement goals.

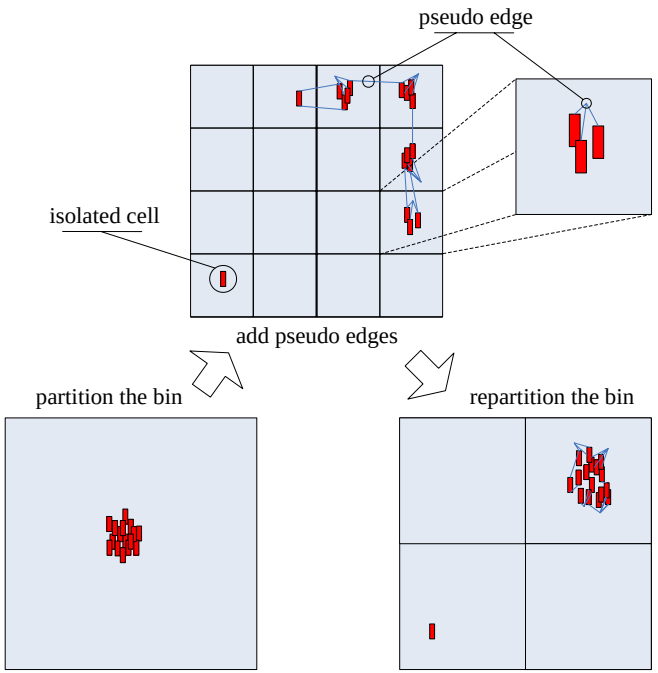


Figure: Proposed clustering strategy.

Process 3: Soft Clustering

Together with the voltage assignment, the soft clustering strategy is performed at every level after initial voltage assignment.

Voltage Island Generation Methodology

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  if $(m = m_t)$
    Process 1; Process 2; Process 3;
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    Process 2; Process 3;
  end if
end while

Experimental Results

Table: EXPERIMENTAL RESULTS.

name	period	Capo			CapoLLV		
		power	slack	HPWL	power	slack	HPWL
c880	2.4	0.022	-0.20	1.15E6	0.017	-0.211	1.19E6
c1355	3.05	0.022	0.06	1.33E6	0.015	0.068	1.33E6
c1908	4.0	0.024	-0.24	2.08E6	0.018	-0.087	2.17E6
c2670	4.0	0.046	-1.02	4.62E6	0.034	-0.768	4.68E6
c3540	5.5	0.039	-0.39	5.29E6	0.022	-0.404	5.33E6
c5315	4.8	0.067	-1.001	7.58E6	0.044	-0.618	7.94E6
c7552	5.0	0.090	-0.21	10.61E6	0.067	-0.082	11.39E6
s1488	3.9	0.022	-0.05	1.84E6	0.016	-0.025	1.88E6
s15850	8.6	0.123	-3.88	24.94E6	0.094	-3.788	27.25E6
s35932	20.6	0.107	0.44	48.74E6	0.055	0.418	50.57E6
s38417	5.6	0.433	-3.30	55.49E6	0.274	-3.384	58.33E6
s38584	10.5	0.259	-1.40	68.15E6	0.183	-0.738	70.92E6

period: clock period(ns); slack: worst slack(ns).

Experimental Results

Table: COMPARISON OF CAPOV AND CAPOLLV.

name	power bound	# of LC			HPWL	
		CapoV	CapoLLV	Reduction	CapoV	CapoLLV
c880	85%	60	33	45.00%	1.24E6	1.19E6
c1355	70%	76	38	50.00%	1.33E6	1.33E6
c1908	75%	109	45	58.72%	2.19E6	2.18E6
c2670	80%	113	33	70.80%	4.96E6	4.66E6
c3540	50%	106	67	36.79%	5.48E6	5.27E6
c5315	70%	156	66	57.69%	8.99E6	7.77E6
c7552	70%	205	85	58.54%	11.87E6	11.12E6
s1488	70%	161	48	70.19%	1.89E6	1.90E6
s15850	80%	491	217	55.80%	32.82E6	26.27E6
s35932	60%	1613	393	75.64%	62.98E6	51.17E6
s38417	60%	1667	475	71.51%	64.84E6	57.33E6
s38584	70%	836	307	63.28%	72.81E6	69.49E6

Experimental Results

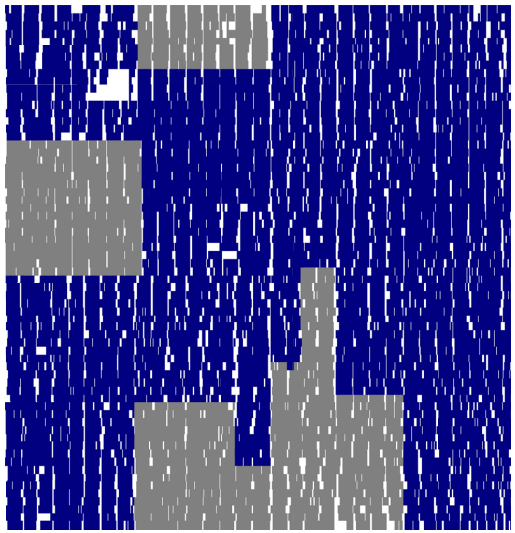

Figure: s15850

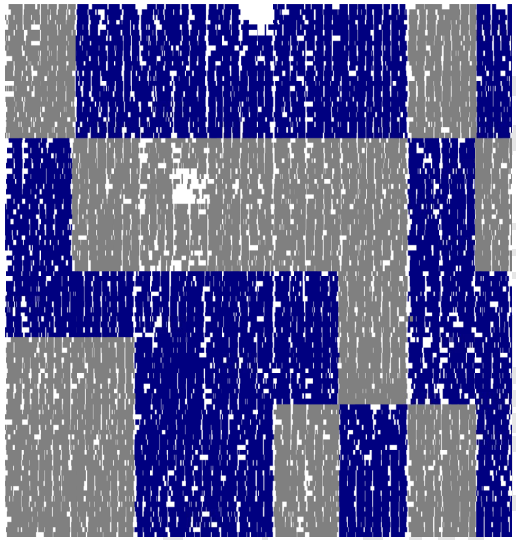

Figure: s38417

Summary and Conclusion

- In this work, we consider level converter which is ignored in related works on voltage island generation.
- The logical and physical boundaries are NOT always inconsistent. They could be optimized simultaneously by the logic and layout aware methodology.
  - The methodology is integrated with multilevel placement tool.
  - The voltage assignment algorithm considers both LCs and physical adjacency.

Thank you!