ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

UNIVERSITY of LOUISIANA Lafayette

The Center for Advanced Computer Studies

Shelf Packing to the Design and Optimization of A Power-Aware Multi-Frequency Wrapper Architecture for Modular IP Cores

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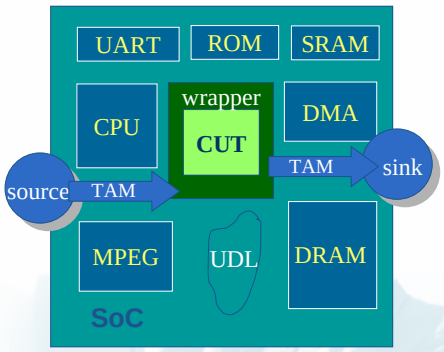
NAIST

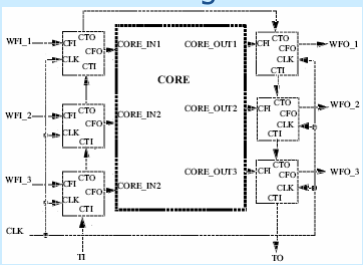
Concept View of SoC Test

- Test pattern source and sink
- Test access mechanism
  - Serves as “test data highway”
  - Trade-off between transport capacity of the mechanism and the test application cost
  - TAM configuration
- Core test wrapper
  - Switching between normal / test / interconnect mode
  - Core isolation
  - Width adaptation

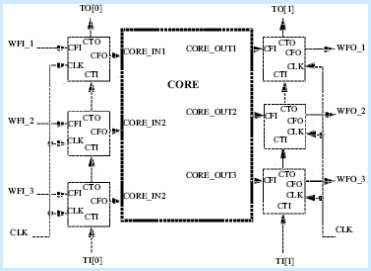


IEEE Std. 1500 Wrapper

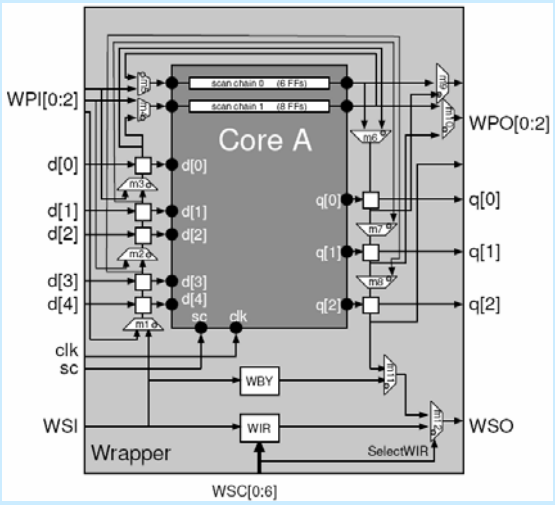
Serial configuration



Parallel configuration



- Mandatory single-bit WSP
- User-defined scalable multi-bit WPPs



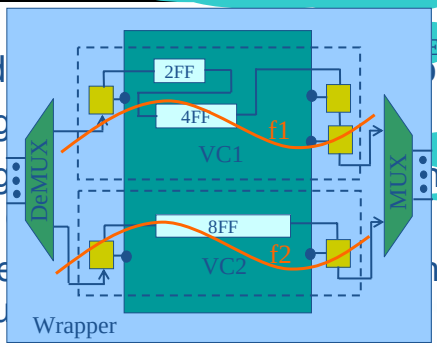
Outline

- Background
- Related work
- Proposed work
  - Time-gated multi-freq. wrapper architecture
  - TGSPW optimization algorithm
- Simulation and comparison
- Conclusion

Multi-Clock Testing Problem

[Marinissen-ITC'00, Iyengar-DAC'02]

- Testing mod… …ck SoC
  - Use a sing…
  - Use a sing… …multiple functional …
  - Use differe… …chains in different fu…

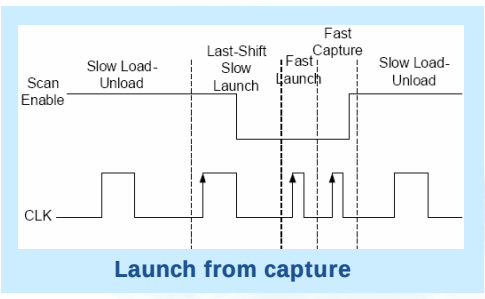


[Xu-DAC'05]

- Minimize clock skew during shift — scan chain grouping into virtual cores
- Virtual TAM is constructed to connect a virtual core to the external TAM via bandwidth matching interface

Facilitate At-Speed Testability

- At-speed/ beyond at-speed test becomes the major component of the SoC test framework
  - Generate at-speed/ beyond-at-speed launch and capture clocks on chip
  - *Slow shift and fast or beyond functional operation*
    - Load/unload test data at a rate much slower than the launch-n-capture clock
    - At-speed testing ability is not affected by the shift rate
    - Only test time is affected by the shift rate

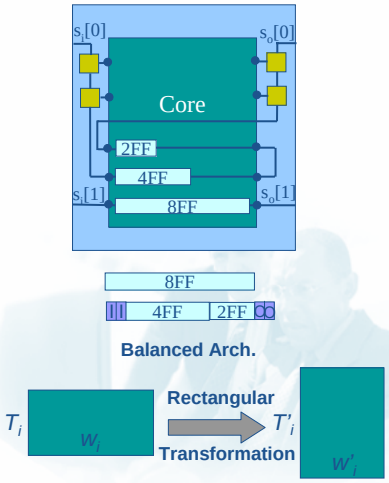


Single Freq. Wrapper Design

- Balanced wrapper scan chain (WSC) design
- Test transformation through serial-parallel or parallel-serial conversion
- Construct a set of rectangles representing different test time for core C_i at width of w_i

  $\boldsymbol{R_i(w_i, t_i(w_i))}$
- Study the trade-off between assigned TAM width and corresponding test time

$$T = \frac{\{1+\max(s_i, s_o)\}\cdot n_v + \min(s_i, s_o)}{f}$$



Multi-Freq. Wrapper Design

- Slower scan-clock frequency results in higher pattern shifting time

$$t_i = \frac{\max(s_i, s_o)\cdot n_v + \min(s_i, s_o)}{f_{s_i}} + n_v \cdot t_c \approx \frac{L^i_{\max}(w_i)}{f_{s_i}} \times n_v$$

- Higher scan-clock frequency results in higher power consumption

$$p_i = \frac{Pow_i \times f_{s_i}}{F_{\max}}$$

- Bandwidth matching requirement

$$\sum_{i=1}^{N}(w_i \times f_{s_i}) = W_{TAM} \times f_t$$

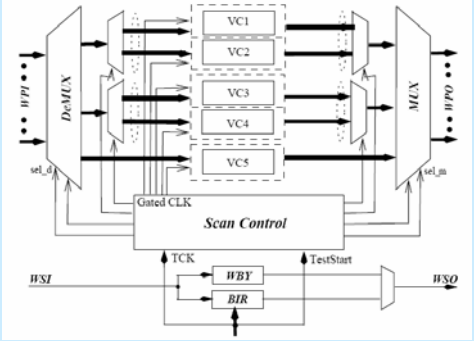
- A balance among test freq. and WSC width is required for minimizing the overall test time

Major Contributions of Our Work

- Propose a new time-gated multi-freq wrapper arch. design
  - *Basic idea*: serial shifting of VCs by clock gating
  - Save ave. power consumption by serial shifting
  - Reduce peak power by multiple shift freq.
  - Develop high-speed clock generation techniques
  - Facilitate at-speed/ beyond at-speed testability
- Propose fast heuristic to optimize wrapper architecture
  - Minimize overall test time under BW_{ext} and P_{ave} constraints
  - 3-D bin packing for serial-parallel architecture

Time-Gated MFSP Architecture

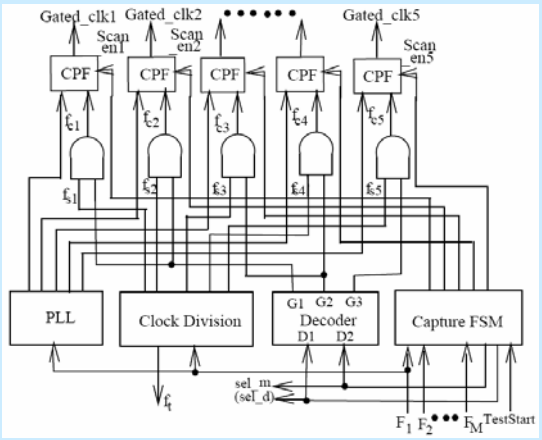
- Serialize shifting of groups of VCs while the VCs within each group are shifted in parallel
  - In the same group, different VCs have different scan-clock freq.
  - External BW is distributed among one group of VCs at a time
- DeMux – Mux bandwidth matching interface
  - Outer level for serial shifting
  - Inner level for parallel shifting



Serial-parallel Architecture

Clock Generation & Controlling

- Serial shifting is controlled by a decoder
  - Generate gating signals and De*MUX-MUX* control signals
  - Activate one group of shift clocks at a time
- Reuse functional on-chip PLL to generate at-speed/ beyond at-speed pulses
  - f_{ci} is filtered out of *gated* f_{si} using CPF
  - CPF is controlled by the *scan_en* signal



Gated Multi-frequency Shifting

TGSPW Optimization Algo.

- *Problem Statement* :

  Find an optimal schedule of VCs, and for each VC select a optimal virtual TAM design and the shift frequency so as to minimize the test time $T_c = \Sigma_{i=1}^{N_c} T_{G_i}$, $T_{G_i} = \max\{ t_i \}, (VC_i \in G_i)$, while satisfying $P_{Gi} \le P_{ave}$ and $BW_{Gi} \le W_{TAM} \times f_t$ constraints

- Propose a 3-D bin packing based approach
  - A VC is defined as a cube VC_i (BW_i, p_i, t_i)
  - Divide the bin into several shelves
  - Cubes are allocated in parallel within a shelf
  - Minimize the height (T_c) of the bin while meeting length BW_{ext} and width P_{ave} limitations

A Test Case – Core *hCADT01*

Test parameters for 7 virtual cores

num	f_{func} (MHz)	N_{in}	N_{out}	N_{bi}	Pow	N_{sc}
1	200	109	32	72	2572	16
2	533	144	67	72	450	3
3	120	89	8	72	930	10
4	750	111	31	72	1314	6
5	500	117	224	72	2605	5
6	330	146	68	72	576	11
7	250	15	30	72	40	4

num	L_{sc_j}
1	{168 168 166 166 163 163 163 163 162 162 162 162 151 151 151 151}
2	{150 150 150}
3	{93 93 93 93 93 93 93 93 93 93}
4	{219 219 219 219 219 219}
5	{521 521 521 521 521}
6	{82 82 82 81 81 81 18 18 17 17 17}
7	{10 10 10 10}

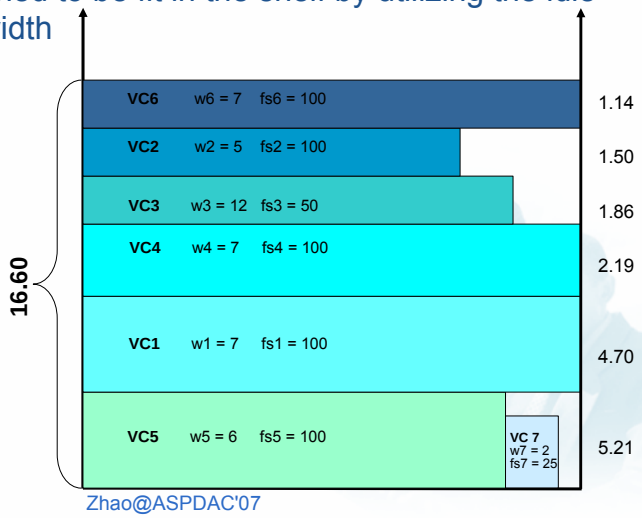
Step1 – Sorting

- Sort VCs in descending order according to their minimum shifting times
  - Assuming that
    1) Each VC can consume up to full bandwidth
    2) Power consumed by the VC is the maximum allowable under the ave power constraint
  - Find the best combination of scan clock frequency and virtual TAM width for each VC
- Use the ordered list to initiate scheduling
- For example core *hCADT01*:
  L_{VC}={*VC5, VC1, VC4, VC3, VC2, VC6, VC7*}

Step2 – Initial Packing

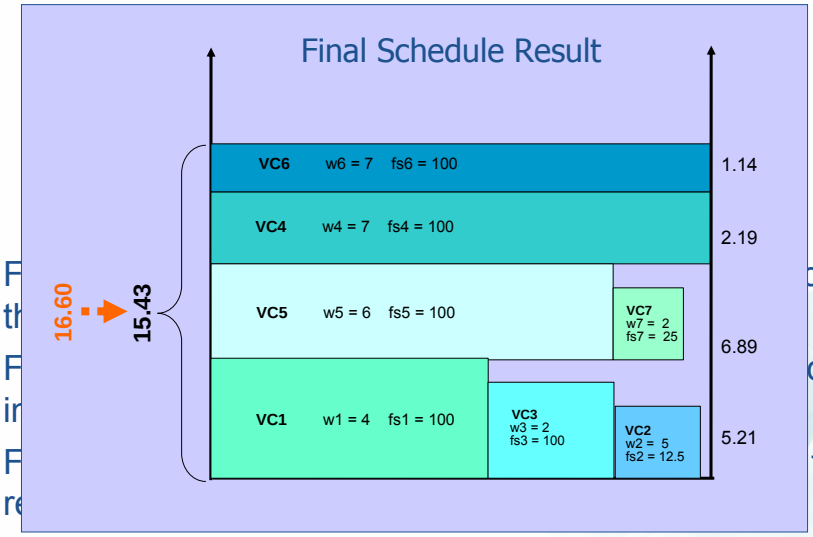
- The height of each shelf is determined by the tallest cube contained in it
- Other cubes are tried to be fit in the shelf by utilizing the idle power and bandwidth

$f_{ATE} = 100$ MHz
$W_{ext} = 7$
$P_{ave} = 4500$



Step3 – Cube Merging

- Merge only when $H_{new}(S_i)+H_{new}(S_j)<H_{merge}$



- F… of th…
- F… d in…
- F… the re…

Simulation & Comparison

- *TGSPW* approach outperforms the parallel architecture as in *MFP* [Xu-DAC'05]

F_{ATE} = 100MHz, Trial freq. = {100 -12.5}MHz

W_{tam}	$P_{ave} = 1500$			$P_{ave} = 3000$			$P_{ave} = 4500$			$P_{ave} = \infty$		
	T [21]	T_{new}	$\delta T(\%)$	T [21]	T_{new}	$\delta T(\%)$	T [21]	T_{new}	$\delta T(\%)$	T [21]	T_{new}	$\delta T(\%)$
16	20.84	16.90	18.90	10.42	9.13	12.38	7.44	6.94	6.72	7.44	7.53	-1.21
15	20.84	16.90	18.90	10.42	10.42	0	8.76	8.33	4.90	7.49	8.33	-11.21
14	20.84	16.90	18.90	10.42	10.42	0	8.88	8.79	1.01	8.88	8.79	1.01
13	20.84	16.90	18.90	10.42	10.53	-1.05	10.42	8.93	14.29	9.59	8.79	8.34
12	20.84	16.90	18.90	10.42	10.53	-1.05	10.42	9.75	6.42	10.42	9.15	12.18
11	20.84	16.97	18.57	11.62	11.12	4.30	10.42	9.75	6.42	10.42	9.75	6.42
10	20.84	17.07	18.09	12.08	11.24	6.95	11.62	10.58	8.95	11.62	10.58	8.95
9	20.84	17.46	16.20	13.00	12.56	3.38	12.78	11.83	7.43	12.78	11.83	7.43
8	20.84	17.57	15.69	14.48	13.50	6.76	14.88	13.50	9.27	14.88	13.50	9.27
7	20.84	19.29	7.40	17.76	16.57	6.70	15.63	15.43	1.27	15.63	15.43	1.27
6	20.84	19.60	5.95	20.84	17.19	17.51	19.20	17.19	10.46	19.18	17.19	10.38
5	25.04	23.38	6.60	23.24	21.81	6.15	23.24	21.81	6.15	23.24	21.81	6.15
4	29.76	26.16	12.09	29.76	24.84	16.53	29.01	24.84	14.37	29.01	24.84	14.37
3	41.68	34.06	18.28	38.36	34.06	11.21	38.36	34.06	11.21	38.36	34.06	11.21
2	59.88	51.61	13.80	58.02	50.36	13.2	58.02	50.36	13.2	58.02	50.36	13.20
1	116.04	100.70	13.22	116.04	98.44	15.16	116.04	98.44	15.16	116.04	98.44	15.16

Conclusion

- Proposed a novel time-gated multi-freq. wrapper design
  - Gate off certain virtual cores to allow the remaining pulsed at higher frequency
  - Bandwidth is efficiently utilized by only activating a group of VCs at a time
- Presented the circuitry for at-speed/ beyond at-speed clock generation and time-gated controlling
- Proposed a 3-D bin packing-based optimization technique