Core-Based Testing of Multiprocessor System-on-Chips Utilizing Hierarchical Functional Buses

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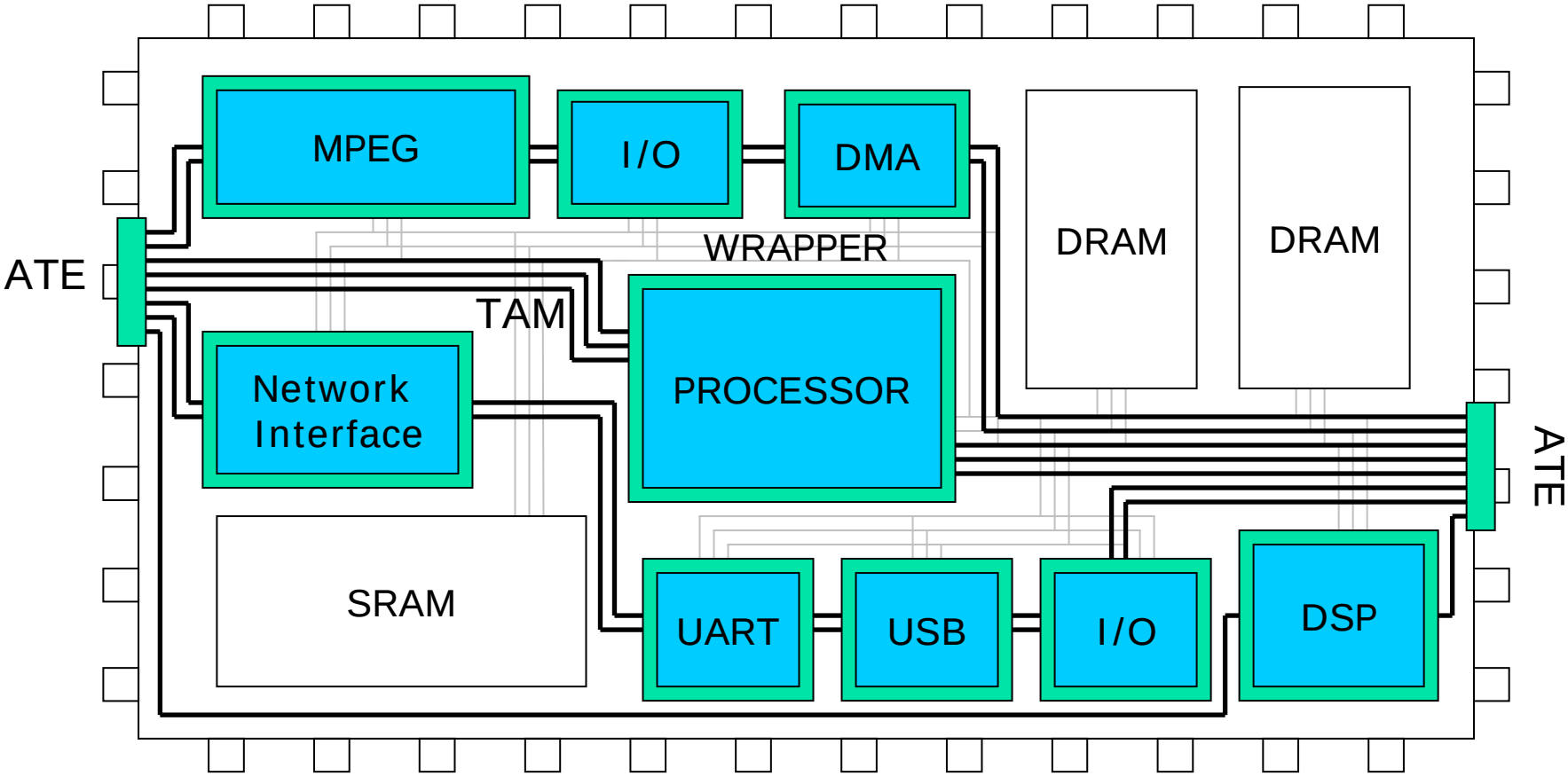
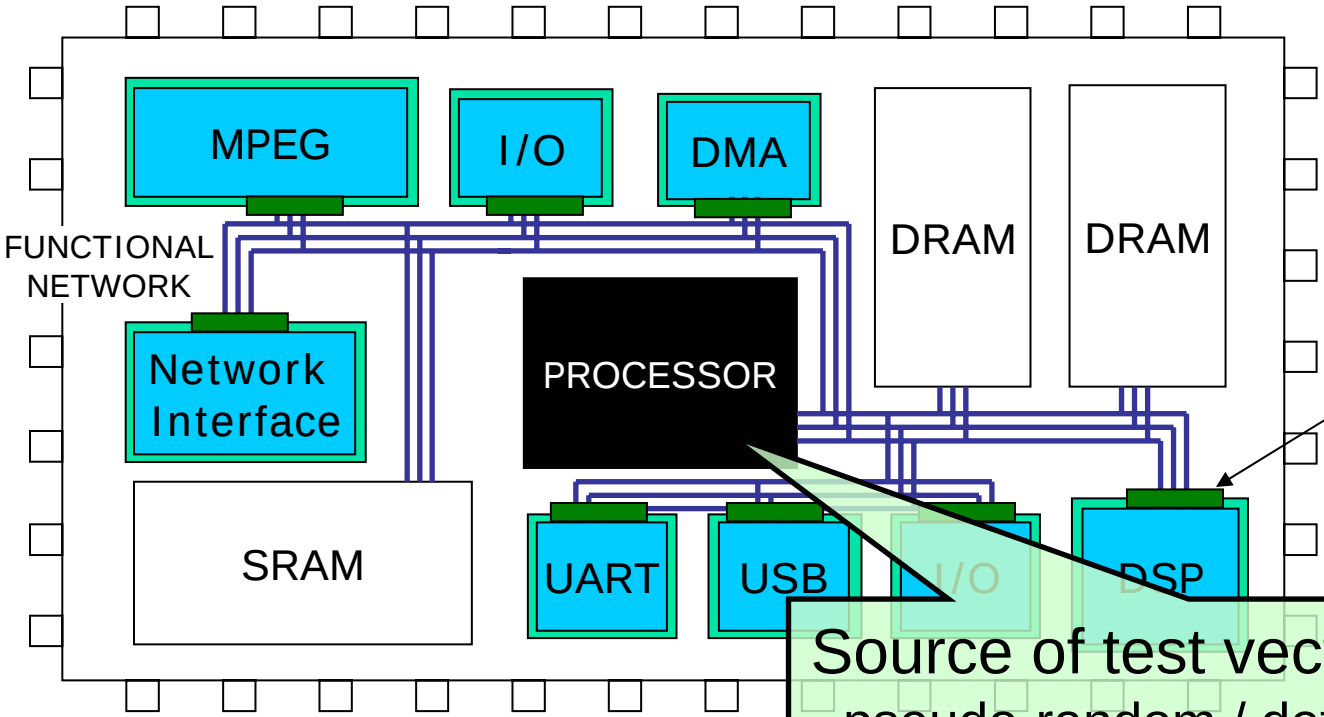
SoC Testing with a Dedicated Test Access Mechanism (TAM)



Functional Bus as a TAM

Bus-based System-on-Chip



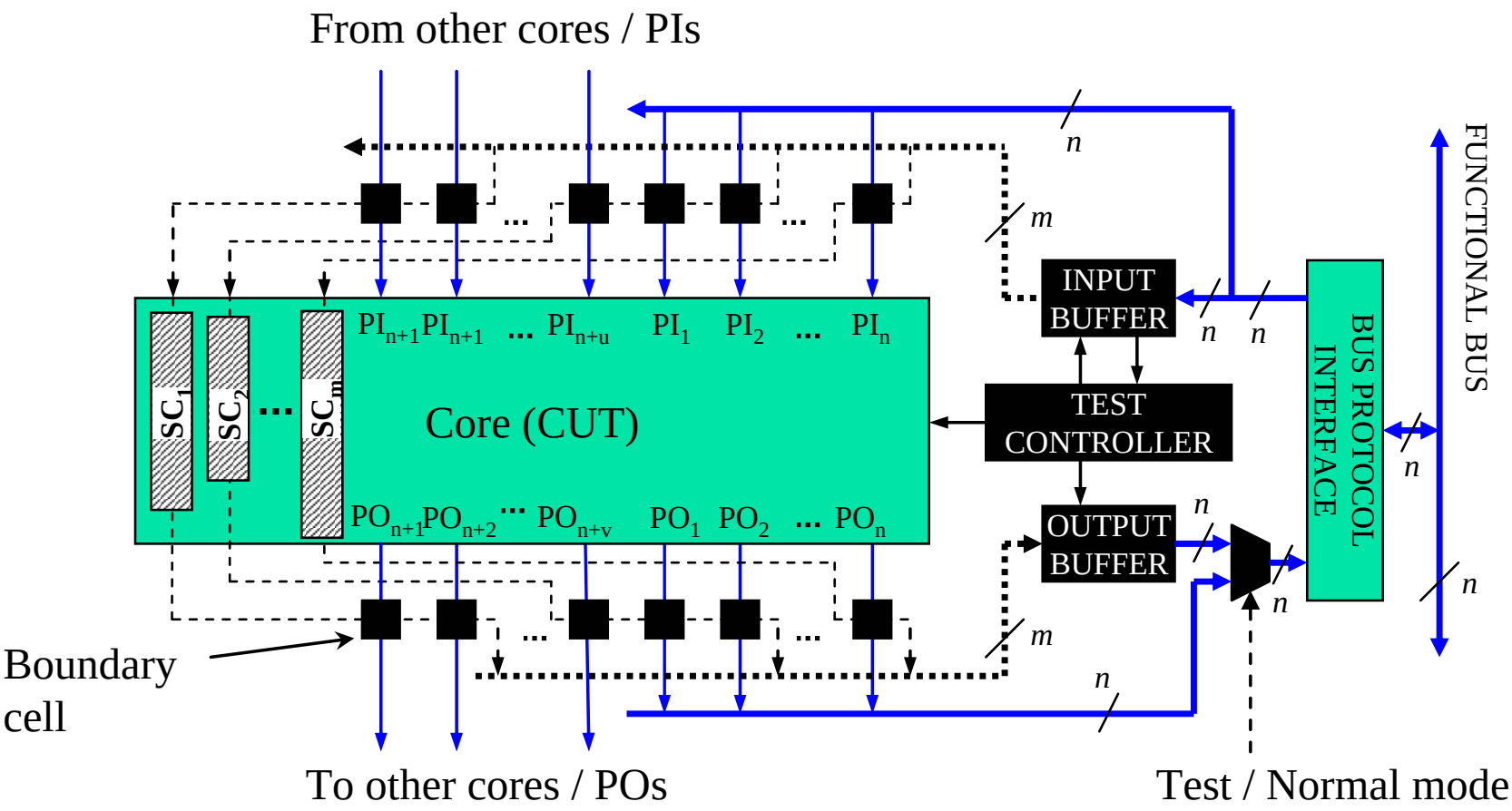
Source of test vector/response:
- pseudo-random / deterministic SBTG
- loaded progressively through a dedicated memory bus and a DMA

Hussin, et al., ICCD 2006
"PAcket Set Scheduling (PASS)"

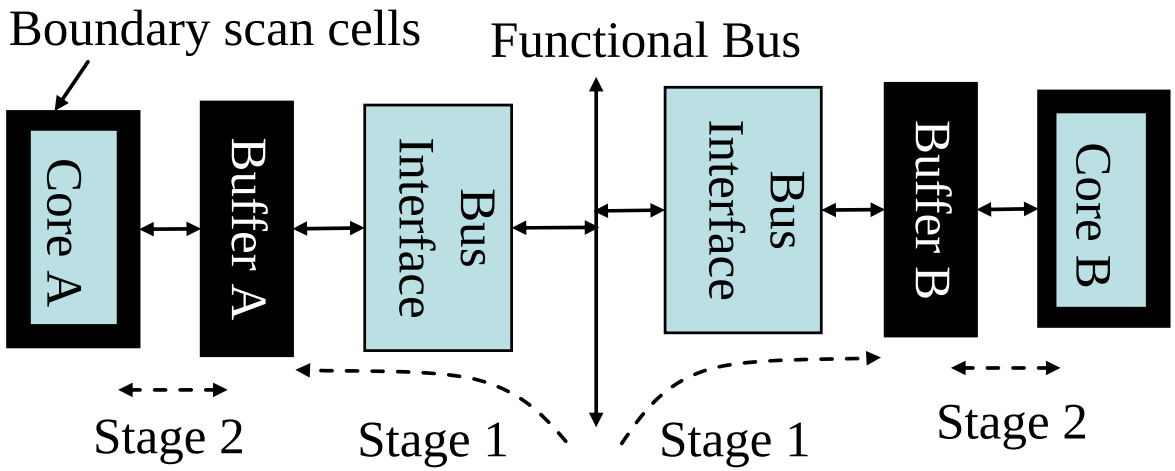
Presentation Outline

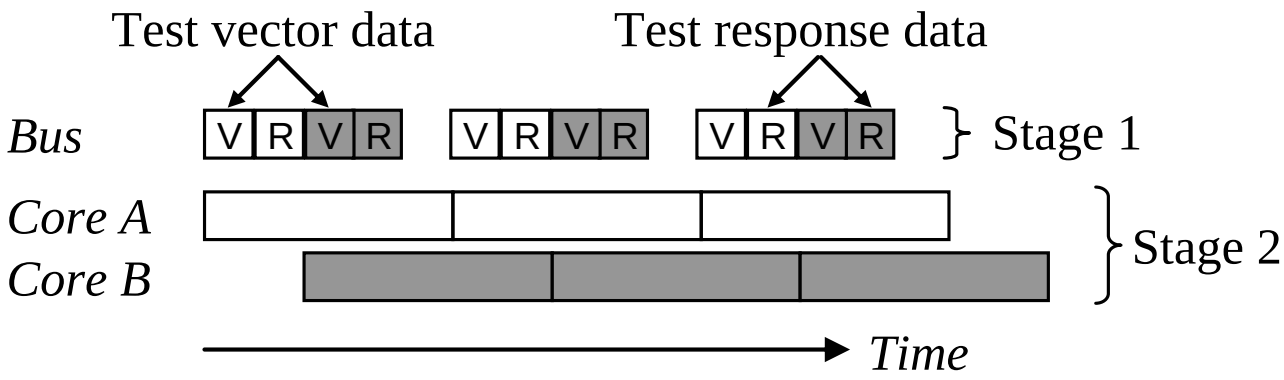
- Buffer-based test support architecture
- Hierarchical bus consideration
- Power-constrained test scheduling
- Packet set scheduling (PASS)
- Multiprocessor PASS (MPPASS)
- Experimental results
- Conclusion

Buffer-based Test Architecture

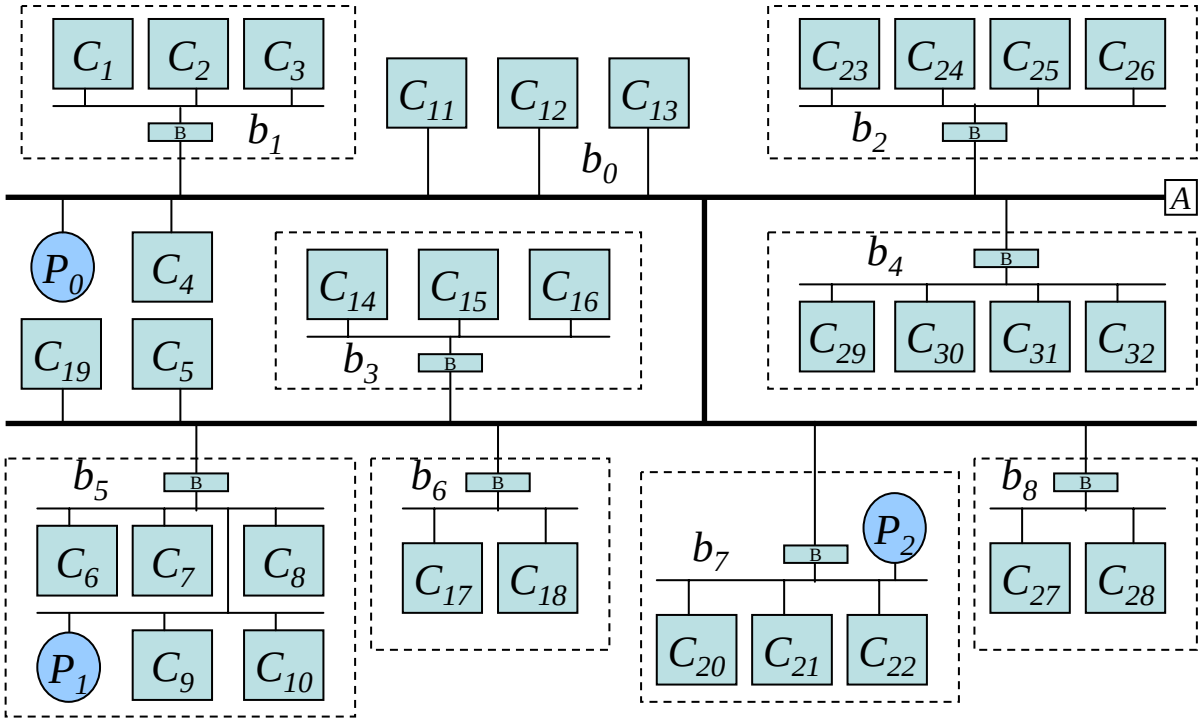


Packet Based Test Data Transportation





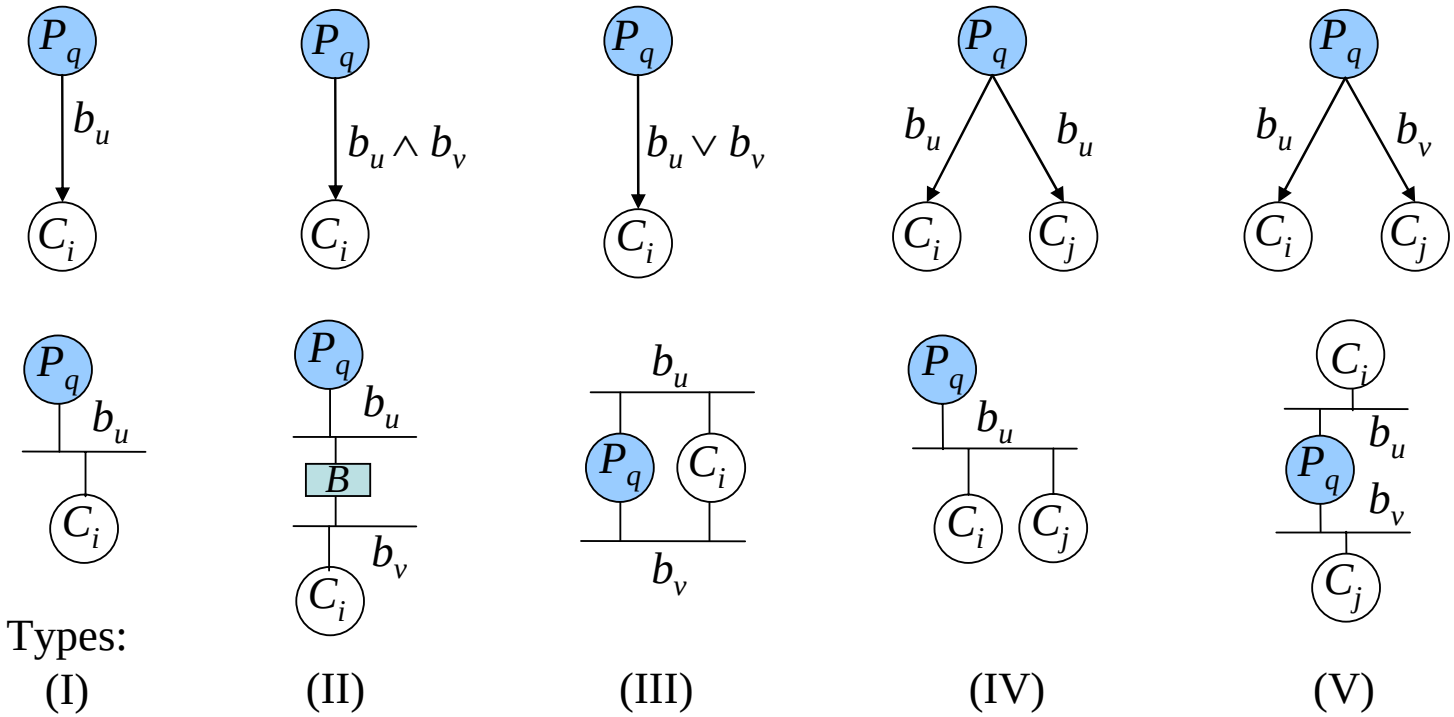
Hierarchical Bus-based MPSoC



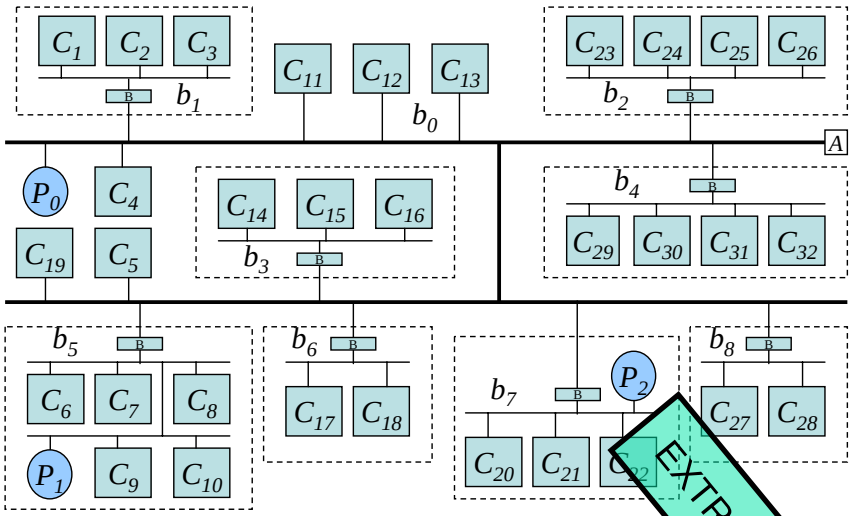
- Which processor tests which core?
- What is the test data delivery schedule for each processor?
- How much buffer is needed for each core?

Test Configurations Graph

- A ***Test Configuration Graph* (*TCG*)** is a processor [test source] – core [test sink] pair that indicates the delivery path on the functional bus(es) for the test data transportation.

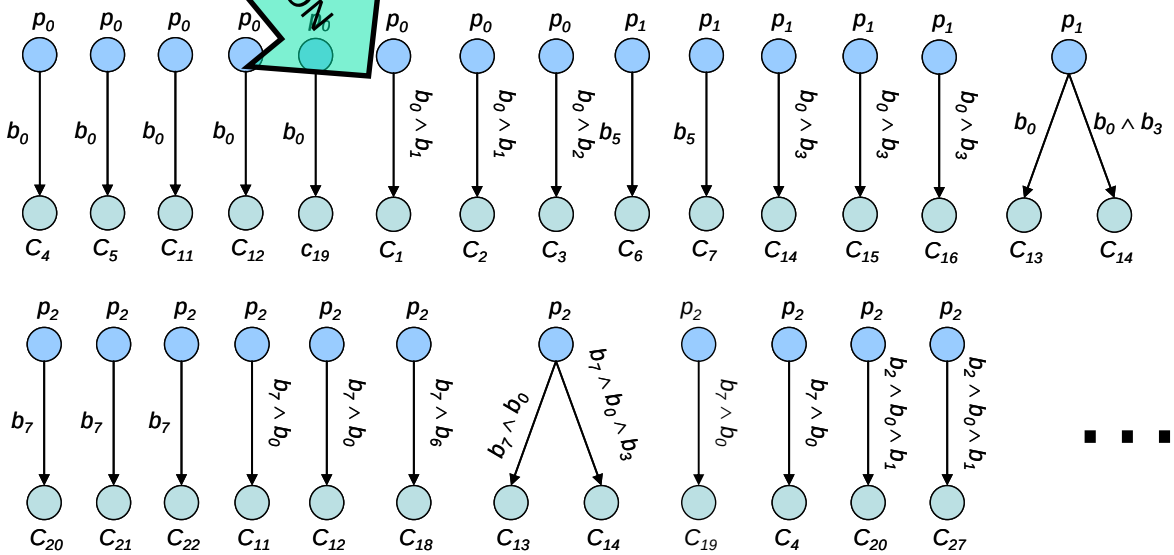


Power-Constrained Scheduling (1/2)

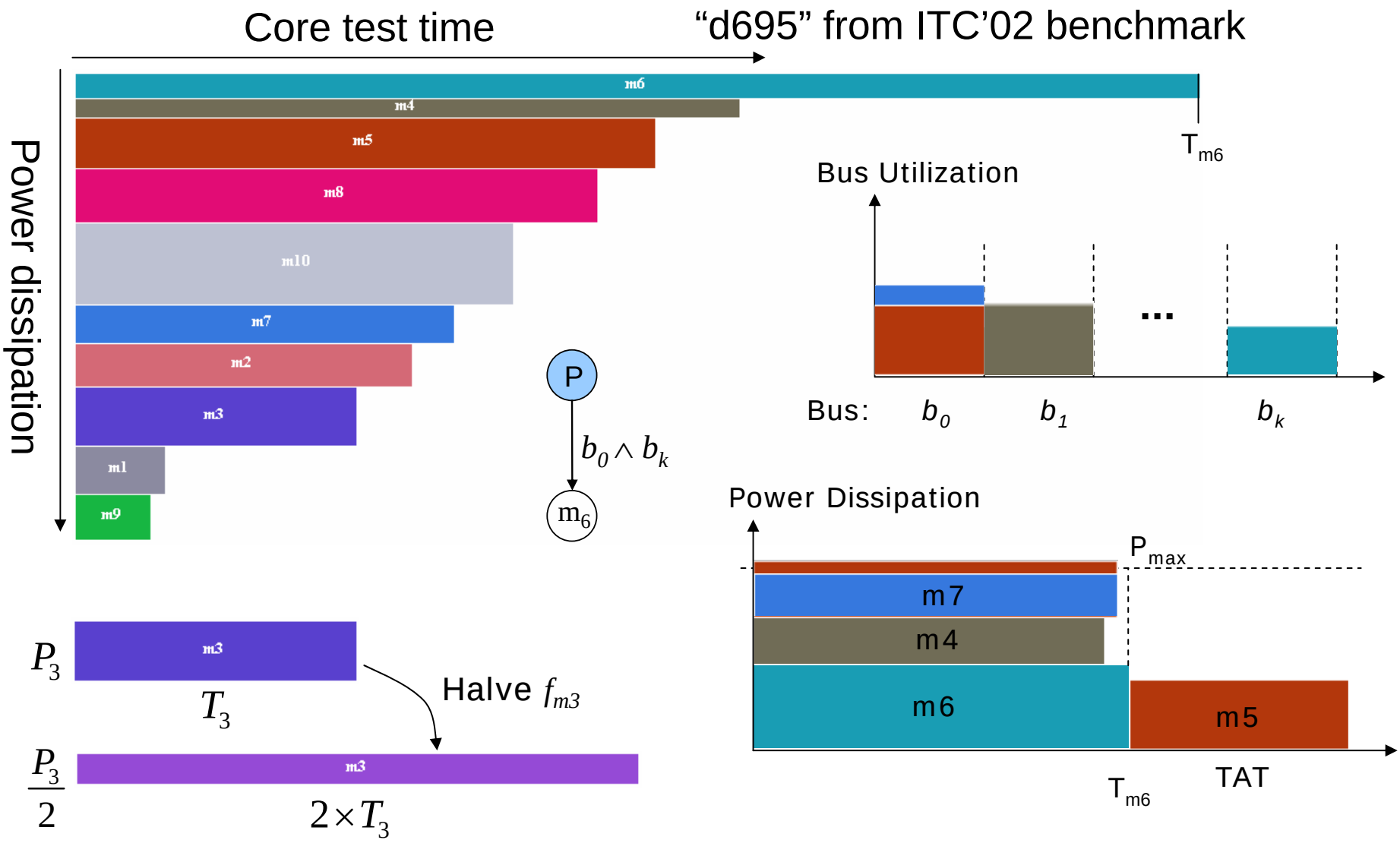


SoC Architecture

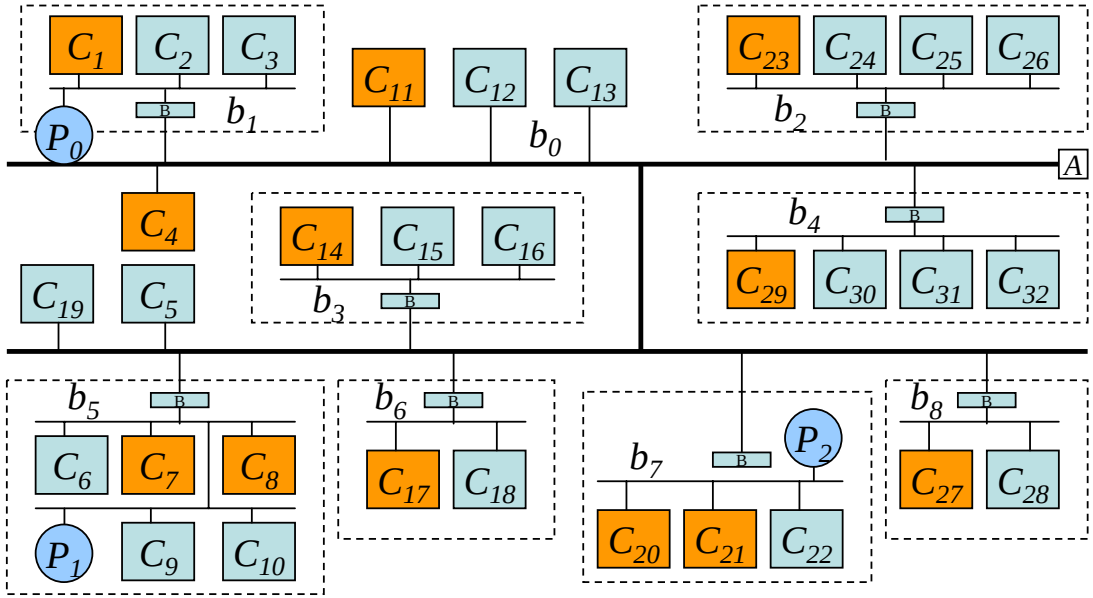
TCGs



Power-Constrained Scheduling (2/2)



Test Groups and Subgroups



$G_0 = \{C_1, C_4, C_7, C_8, C_{11}, C_{14}, C_{17}, C_{20}, C_{21}, C_{23}, C_{27}, C_{29}\}$

$G_{P00} = \{C_1, C_4, C_{11}, C_{14}\}$

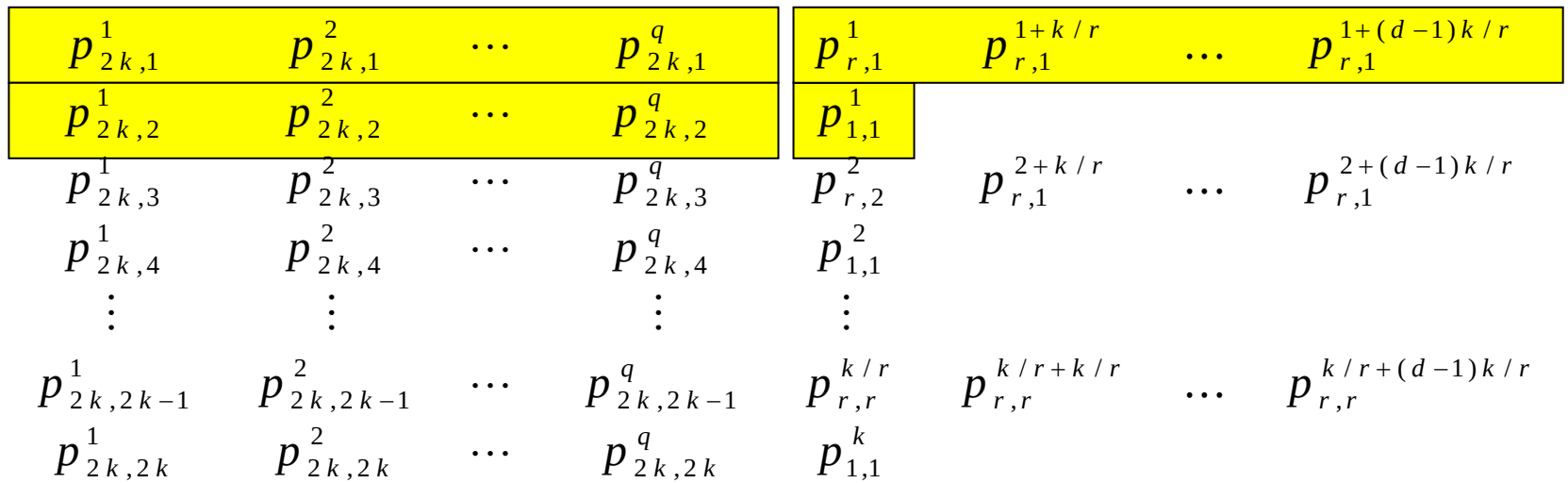
$G_{P10} = \{C_{20}, C_{21}, C_{23}, C_{27}, C_{29}\}$

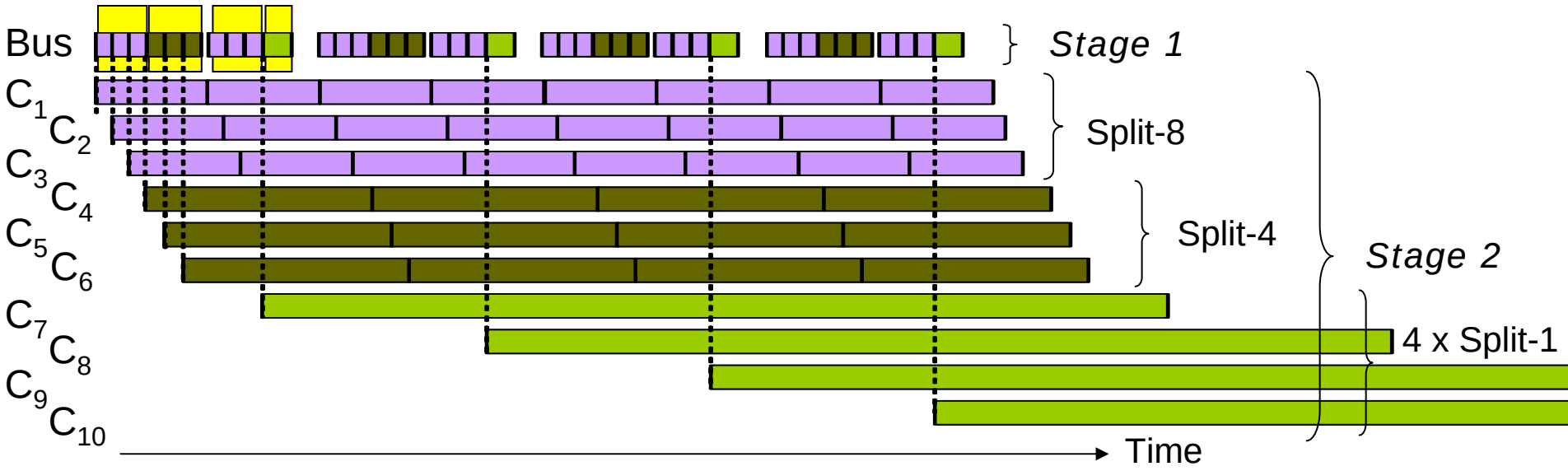
$G_{P20} = \{C_7, C_8, C_{17}\}$

Delivery schedule?
Use PASS for each subgroup

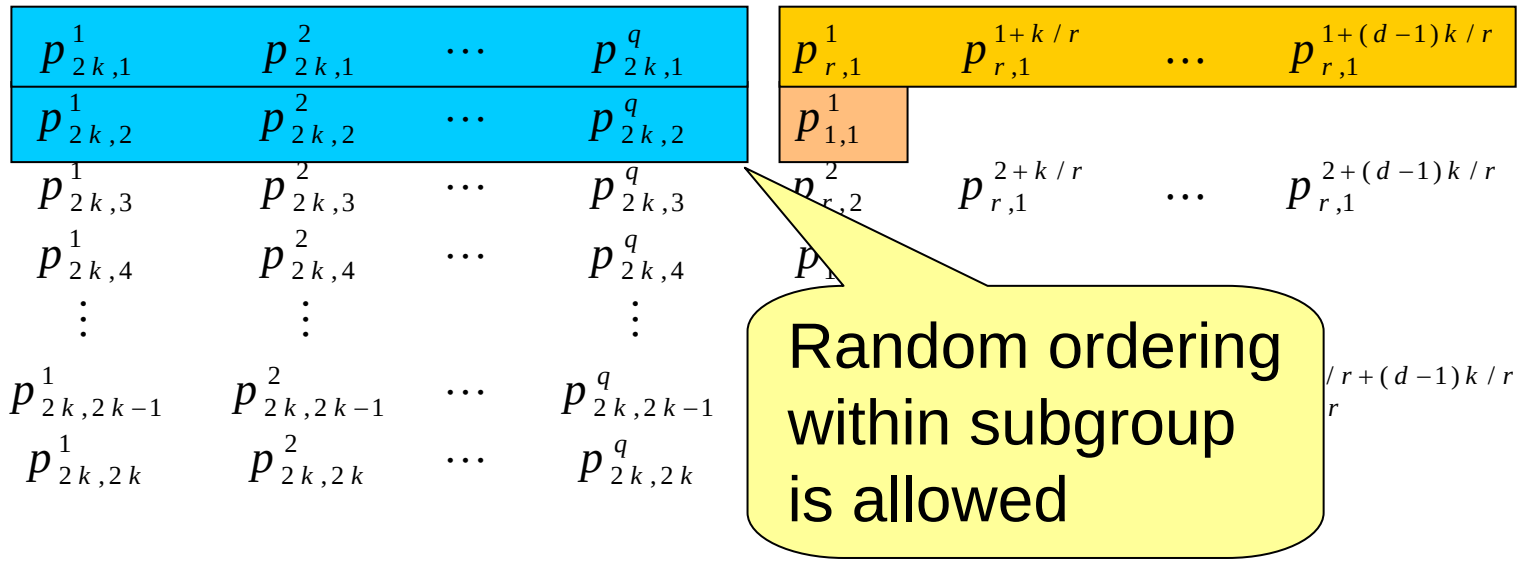
Packet Set Scheduling (PASS)

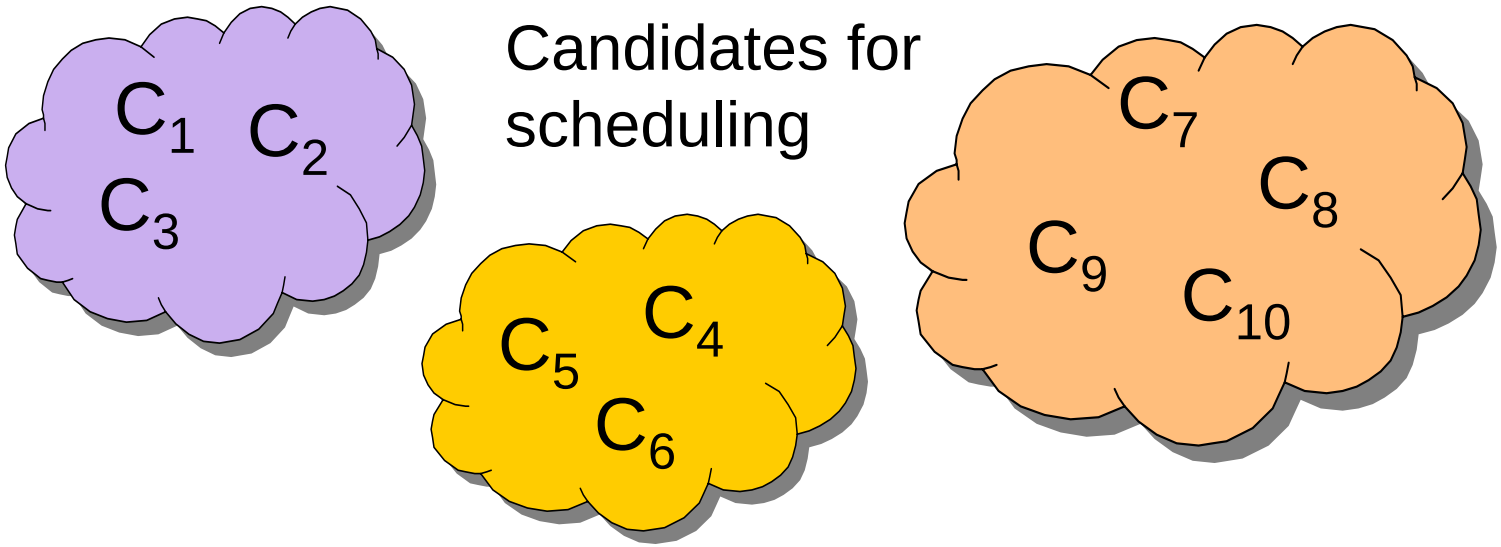
Hussin, et al., ICCD 2006
"PAcket Set Scheduling (PASS)"



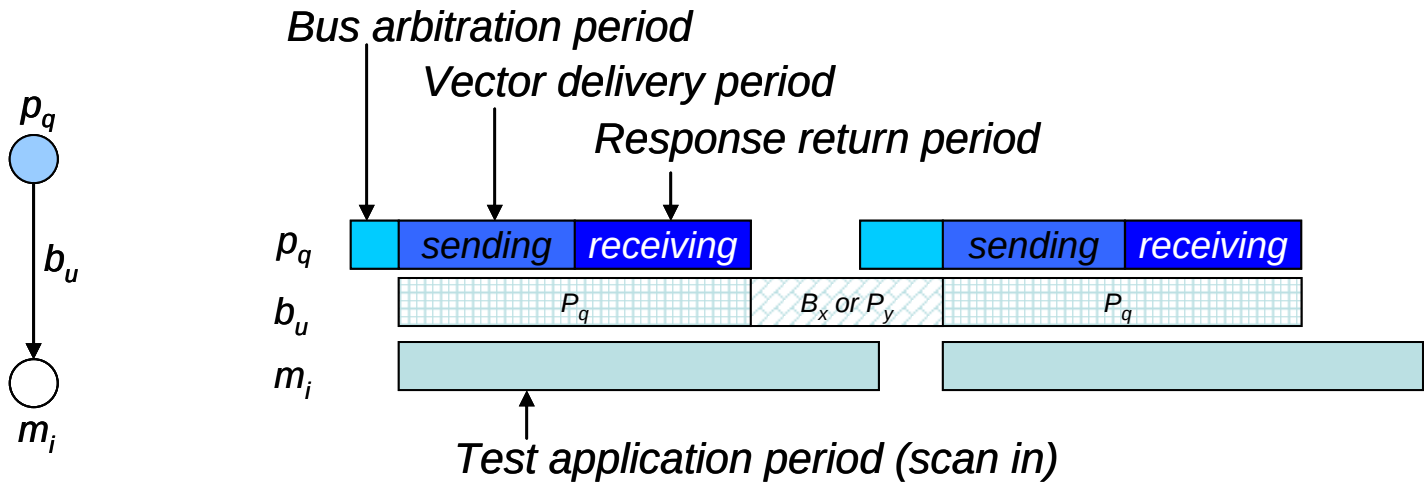


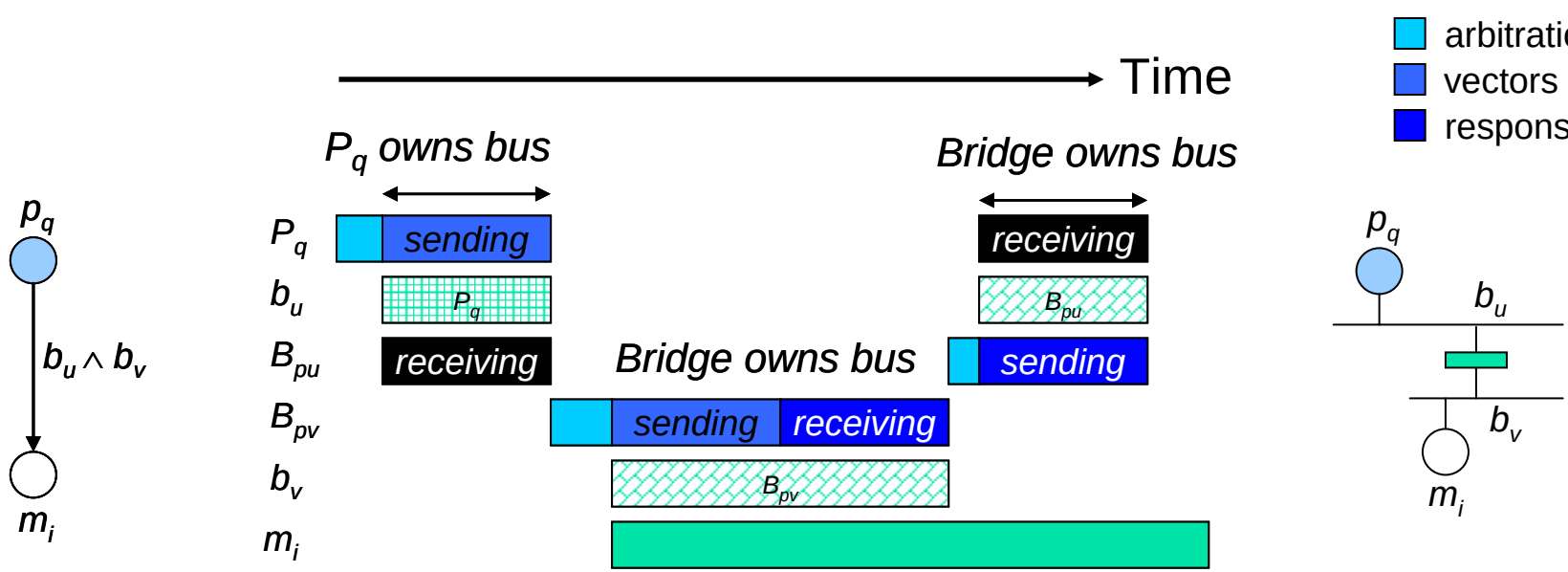
Optimizing PASS → MPPASS



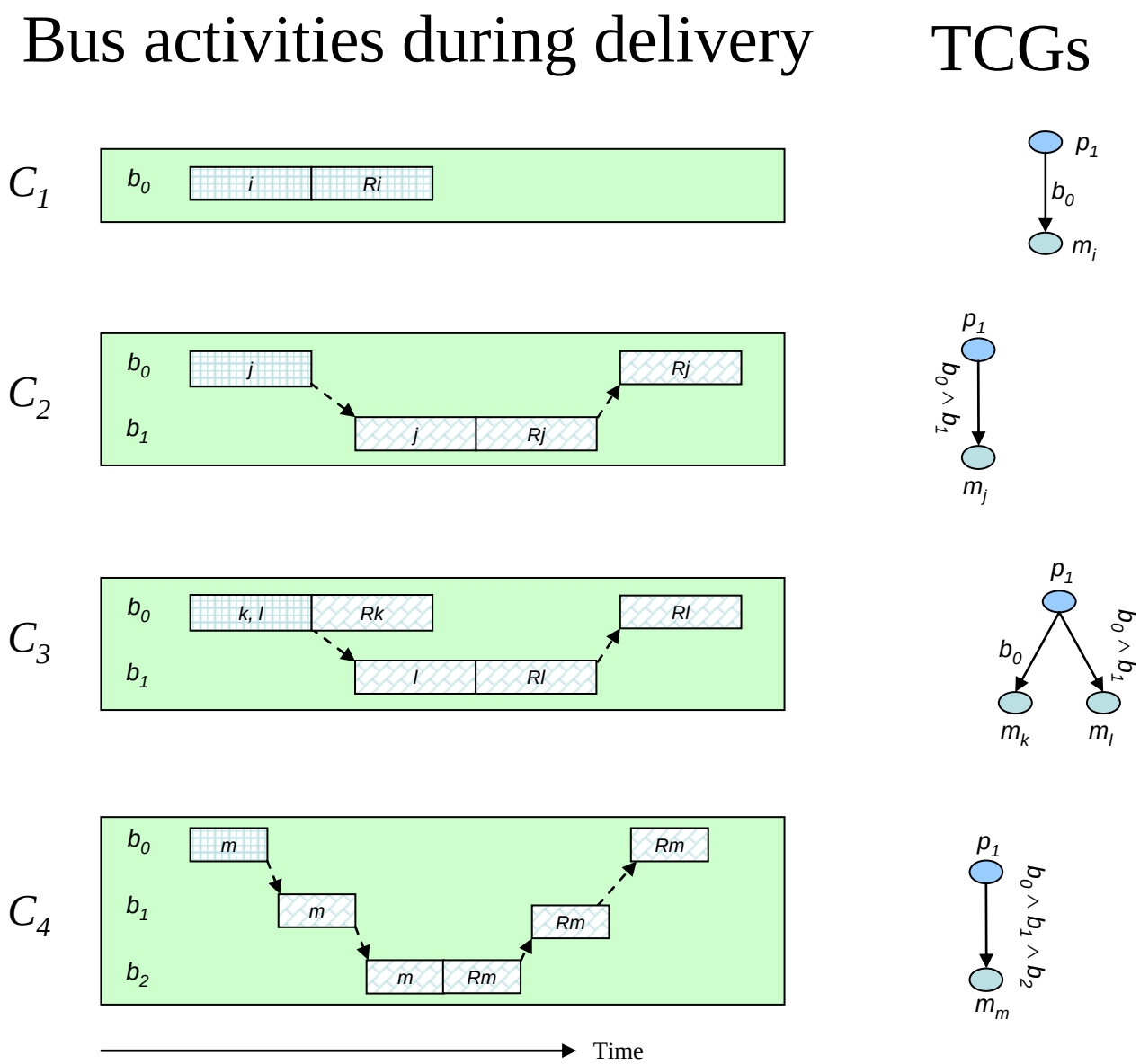


Packet Delivery (Timing Diagram)

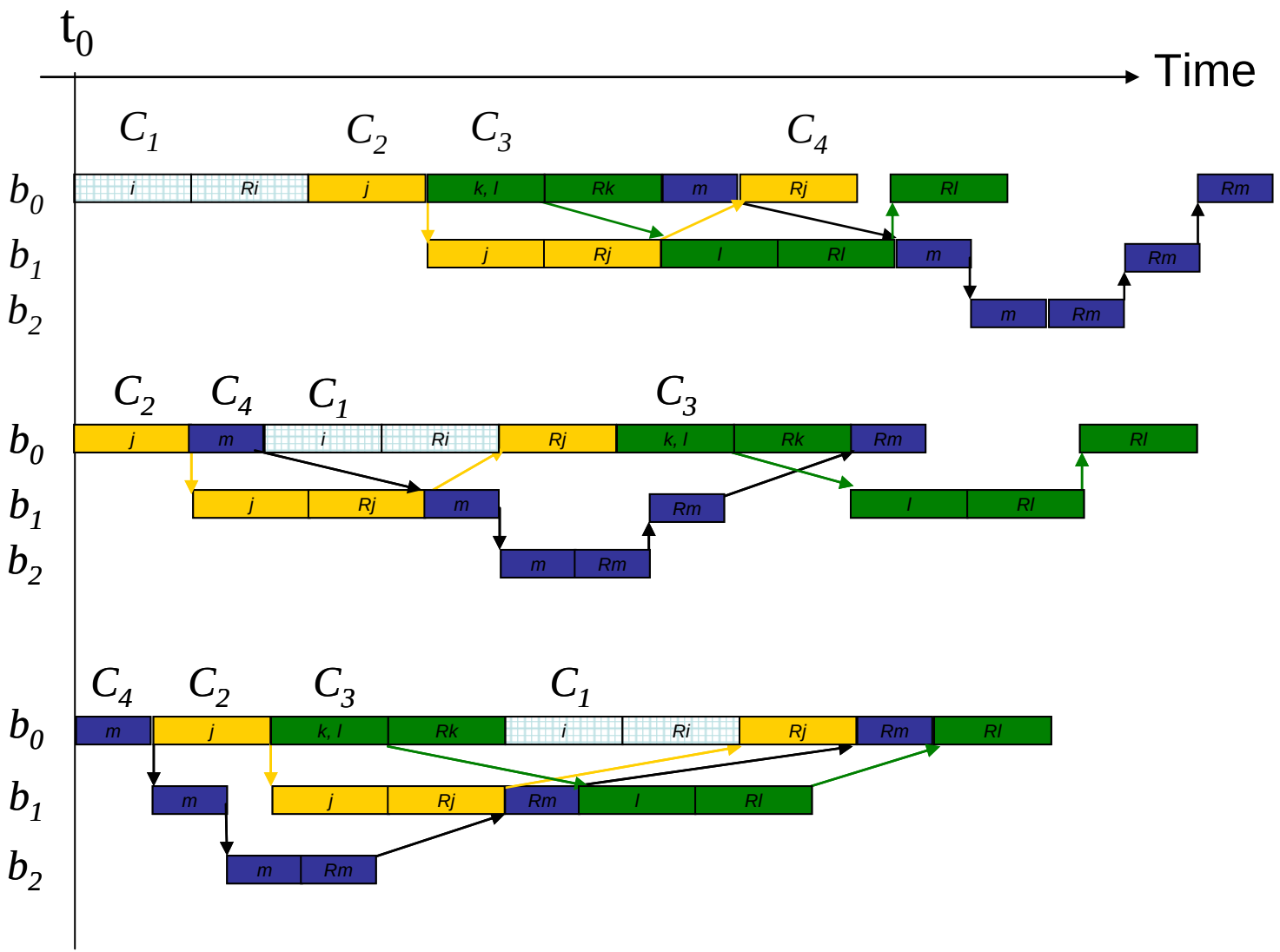




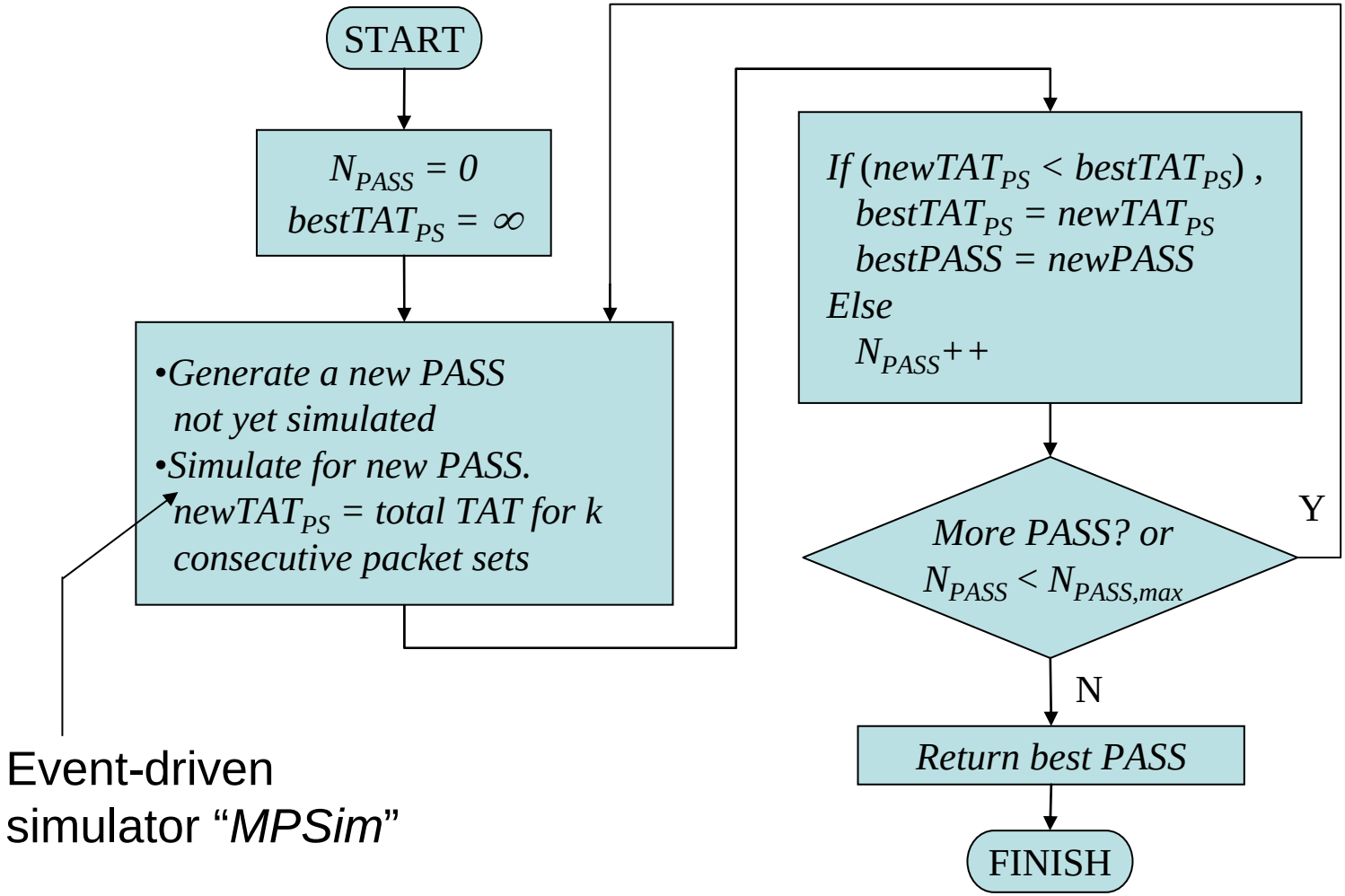
Packet Delivery and Forwarding



Hierarchical Data Delivery (Timing Diagram)



MPPASS Algorithm Flowchart



Experimental Setup

- ITC'02 benchmark circuits

		Scan frequency	Bus frequency
TAM-based		$f_s = F_s$	$f_b = f_s < F_b$
IPASS	**$f_b = f_s$**	$f_s = F_s$	$f_b = f_s < F_b$
	$f_b = 2 * f_s$	$f_s = F_s$	$f_b = 2 \times f_s < F_b$

F_s = Maximum scan frequency (100 MHz)
F_b = Maximum bus frequency

f_s = Selected scan frequency
f_b = Selected bus frequency

Experimental Results

p93791h1 flat-bus	BW = 32			BW = 64		
	$f_b = f_s$		$f_b = 2*f_s$	$f_b = f_s$		$f_b = 2*f_s$
P_{max}	Pouget	IPASS	IPASS	Pouget	IPASS	IPASS
10,000	18.28	18.44	9.04	11.17	8.94	5.34
15,000	18.28	17.34	8.85	10.15	8.85	4.70
20,000	18.28	17.35	8.89	9.58	8.93	4.59
25,000	18.28	17.63	9.07	9.65	9.05	4.75
30,000	18.28	17.78	9.08	9.45	9.07	4.67

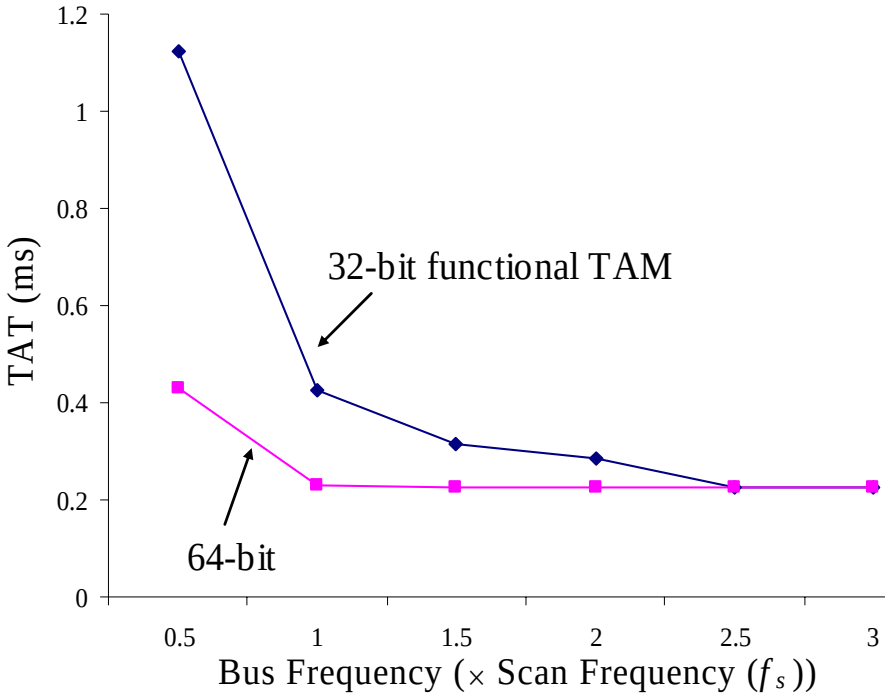
*TAT in milliseconds

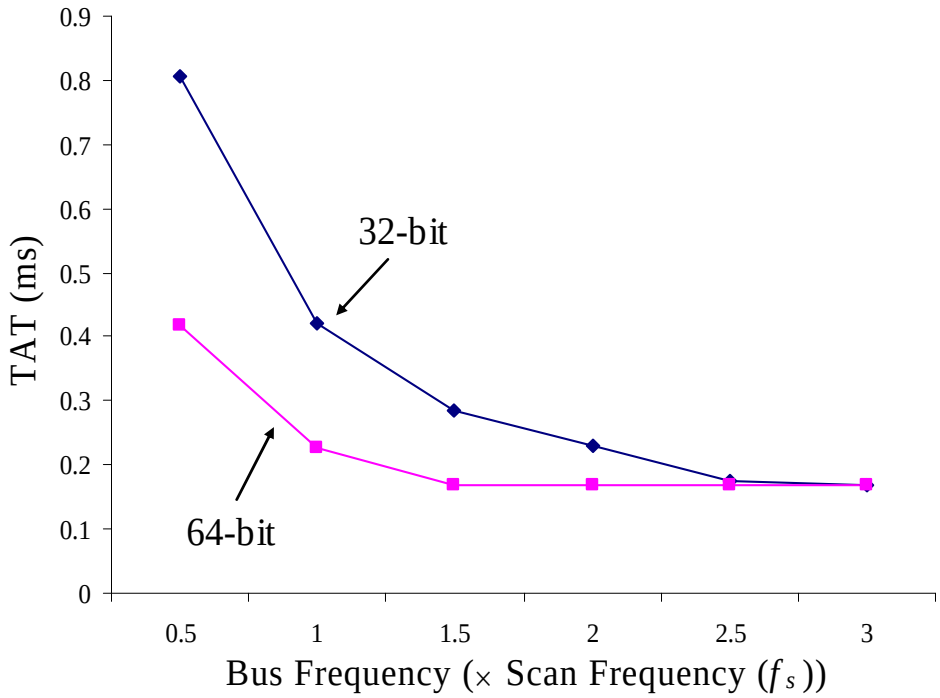
[1] Pouget, et al. (JETTA'05) "Hierarchy constraint"

p93791h2 hierarchy	BW = 32					BW = 64				
		$f_b = f_s$		$f_b = 2*f_s$			$f_b = f_s$		$f_b = 2*f_s$	
	Pouget	IPASS		IPASS		Pouget	IPASS		IPASS	
P_{max}		P@b0	P@All	P@b0	P@All		P@b0	P@All	P@b0	P@All
10,000	18.28	26.97	15.51	13.47	7.83	11.17	13.47	7.83	7.13	5.69
15,000	18.28	20.15	9.51	10.07	4.83	10.15	10.07	4.83	5.05	3.79
20,000	18.28	20.39	7.37	10.20	4.27	9.58	10.21	4.23	5.11	3.51
25,000	18.28	18.95	5.31	9.47	3.24	9.65	9.50	3.20	4.72	2.82
30,000	18.28	18.89	5.31	9.44	3.24	9.45	9.44	3.20	4.78	2.82

(a) P@b0 – one processor in level-0 bus
(b) P@All – one processor in every bus region

Test Time Minimization





Area Overhead (Buffer)

- Buffer sizes per SoC core (#FF) averaged over all P_{max}
- Bus width = 32 bits

Circuit	p93791h1	p93791h2	p22810h1	p22810h2
Min.	99.20	89.79	106.06	107.65
Max.	99.39	98.00	112.00	113.15

Conclusions

- An integrated test scheduling for flat-bus and hierarchical bus SoC
- Offers a test methodology for SoCs with
  - multiple embedded processors
  - flat or hierarchical buses
- Experimental results illustrate the potential of the proposed approach
  - Relax dedicated TAM requirements
  - Minimize TAT