

RunBasedReordering: A Novel Approach for Test Data Compression and Scan Power

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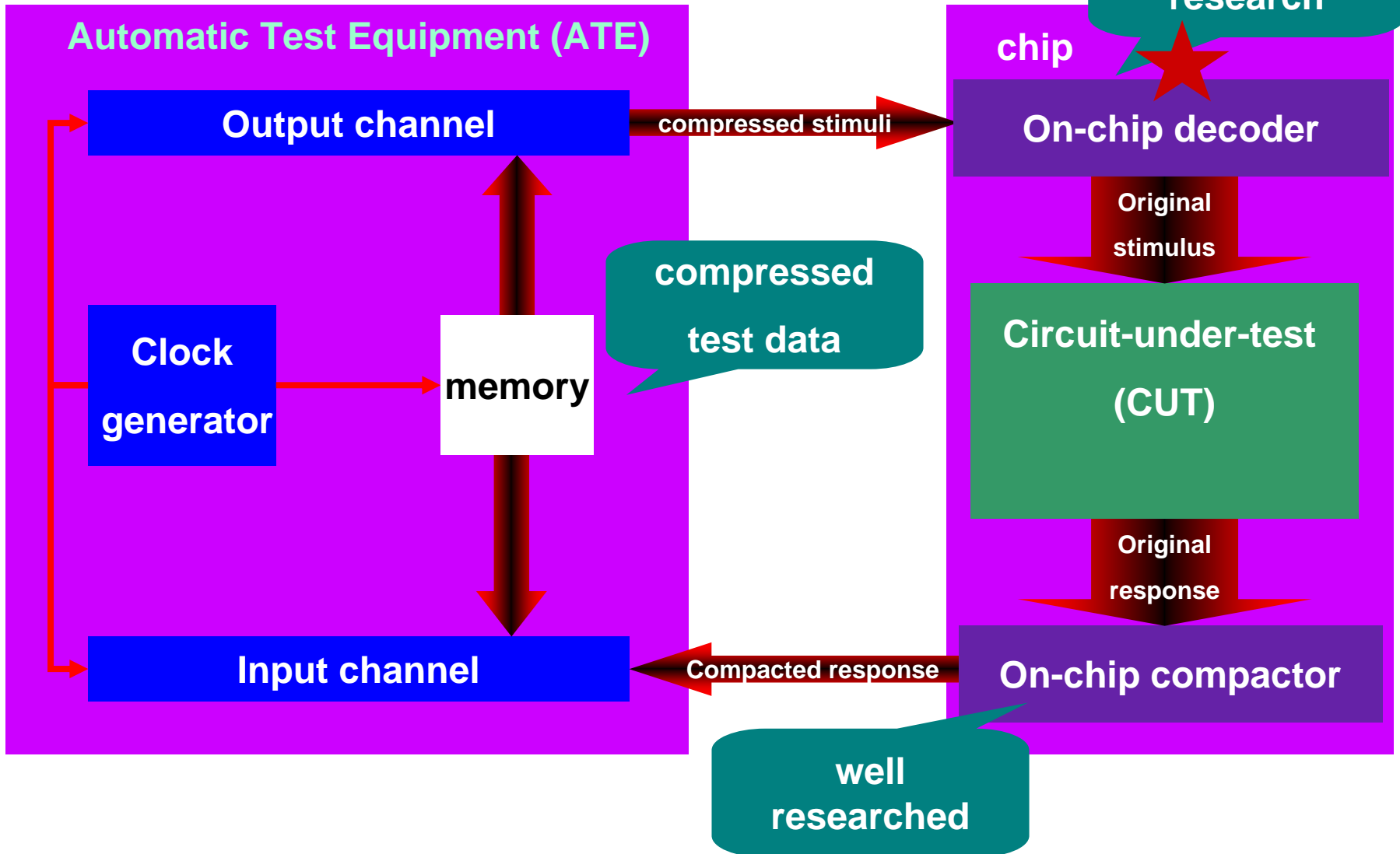
January 30, 2007

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Background: Test Difficulties

- Large Test Data Size
 - 100~1000M bits
 - Automatic Test Equipment
 - small memory
 - cutting down patterns sacrifices fault coverage
- Long Test Time
 - Relative small number of pins
 - 1~2 \$ for 1 minute
- High scan power
 - More flipping registers in test mode vs. work mode
 - Usually 2~3 times

Test Pattern Compression



Compression Methods

- Run length
 - conventional run-length
 - Golomb
 - EFDR: Extended Frequency Directed Run-length
- LFSR based
 - linear expansion
- Dictionary based
 - on-chip memory
 - index instead of data
- Selective Coding
 - encode specified bits
- Hybrid

EFDR Encoding

■ Run

- a sequence of 0s or 1s ended by their complement: 00001, 1110
- test set: a sequence of runs

■ EFDR codes

- run type (1-bit)
- group prefix:
run length based grouping
- group tail:
length encoding within group

Group	Run Length	Group Prefix	Tail	Code Word Runs of 0's	Code Word Runs of 1's
A1	1	0	0	000	100
	2		1	001	101
A2	3	10	00	01000	11000
	4		01	01001	11001
	5		10	01010	11010
	6		11	01011	11011
A3	7	110	000	0110000	1110000
	8		001	0110001	1110001
	9		010	0110010	1110010
	10		011	0110011	1110011
	11		100	0110100	1110100
	12		101	0110101	1110101
	13		110	0110110	1110110
	14		111	0110111	1110111

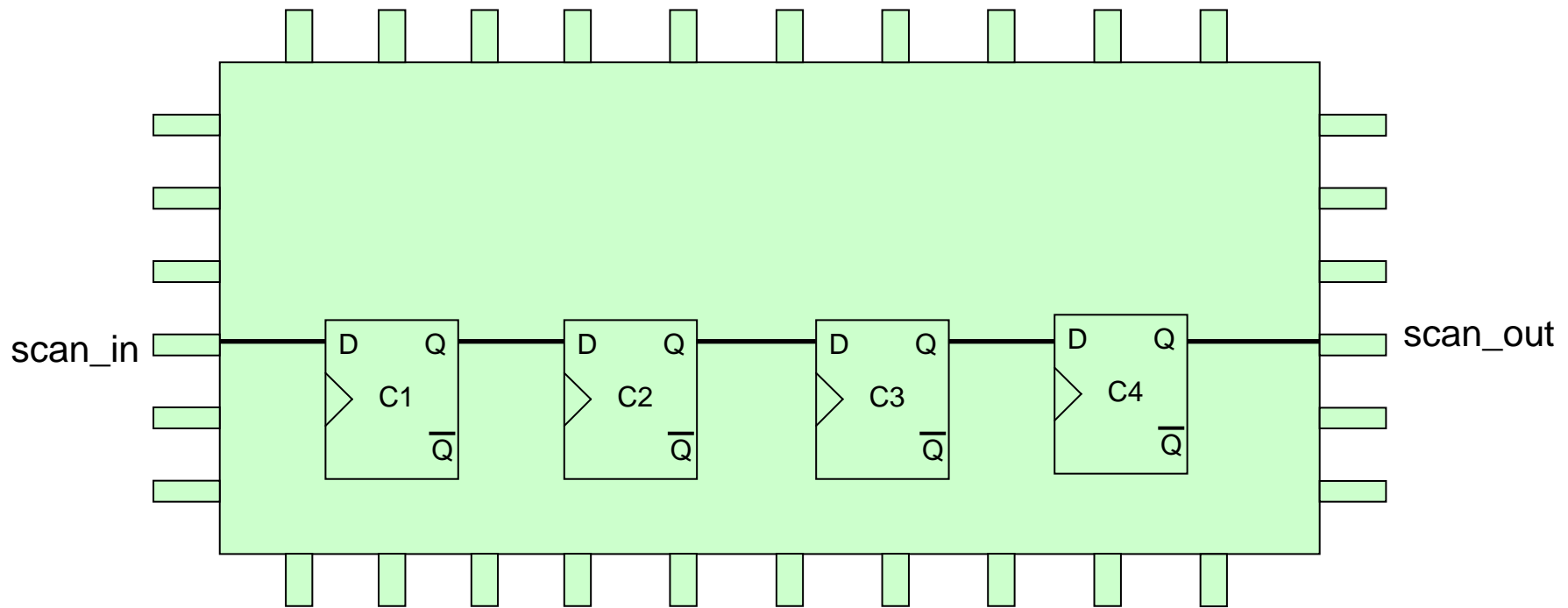
TD = 0000001111110001

Runs: (0)6(1)5(0)2

TE = 0101111010001

Scan Chain Reordering

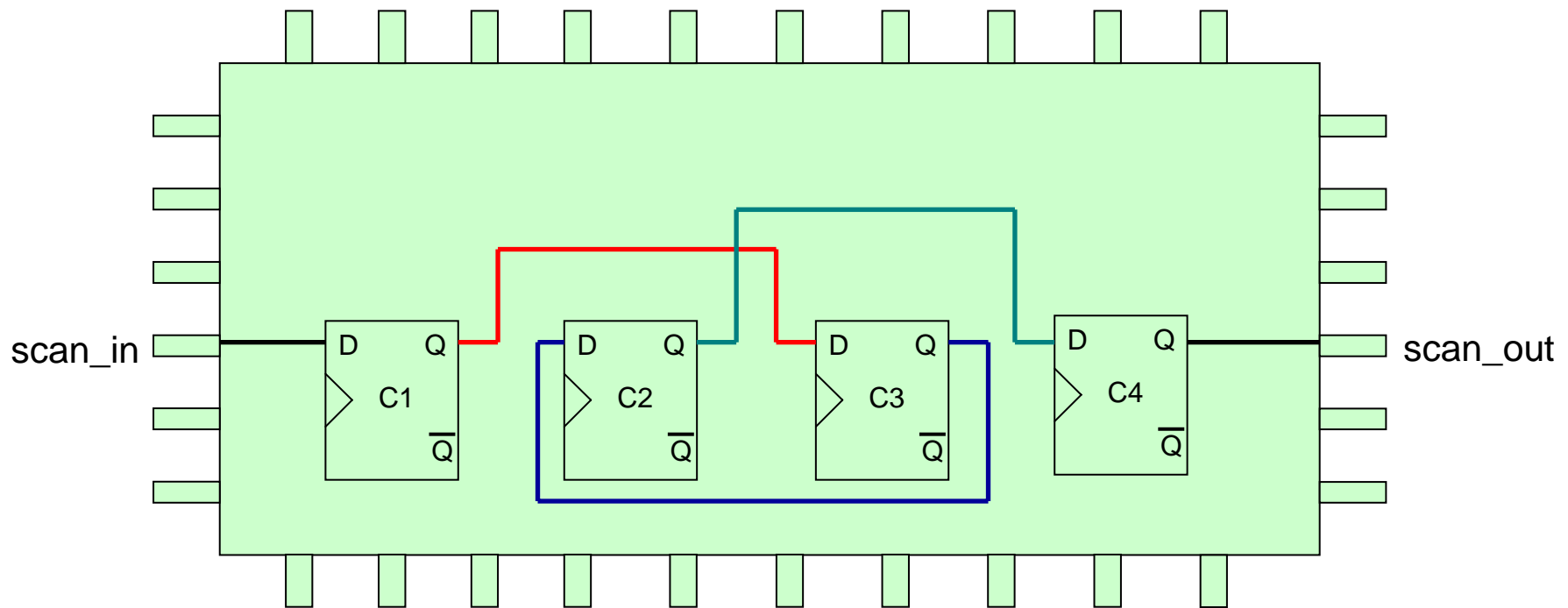
- Idea: reduce the number of runs in the test data
 - exchange pattern bits **without** changing the pattern's functionality



test pattern: 0101

Scan Chain Reordering

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test pattern: 0101

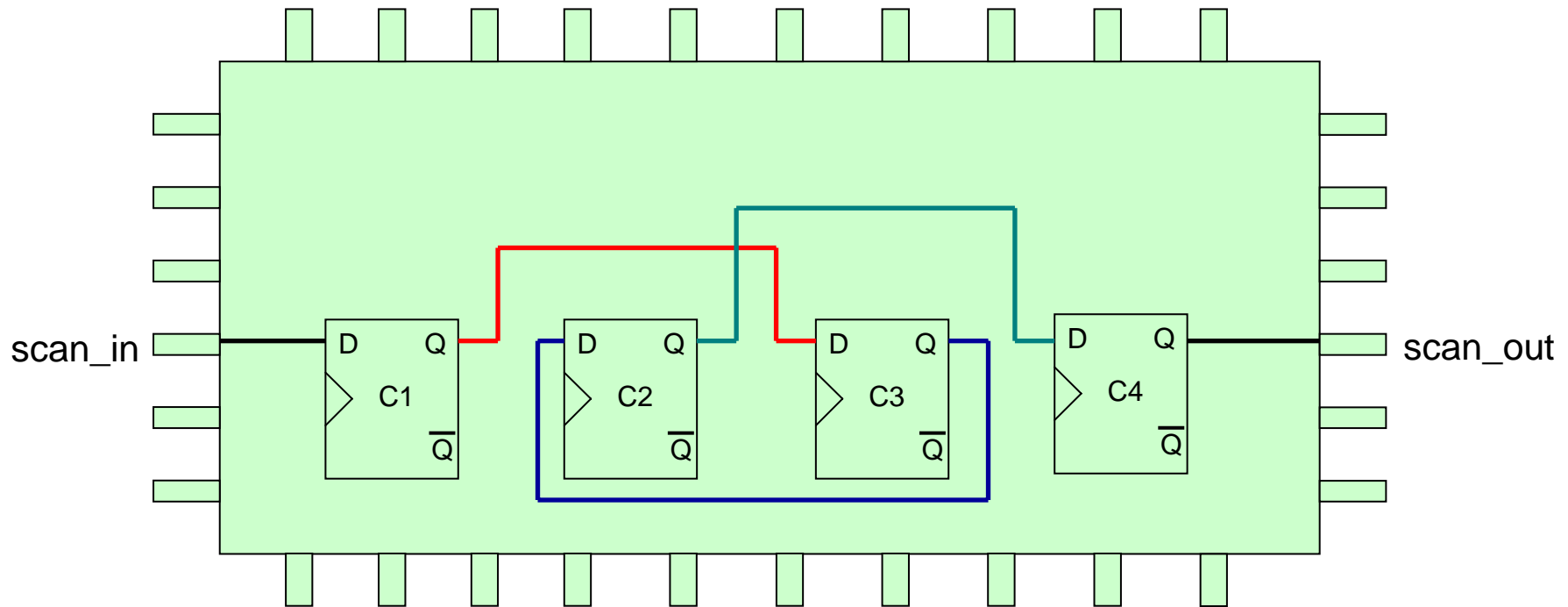
(original form)

test pattern: 0011

(new form)

Scan Chain Reordering

- Idea: reduce the number of runs in the test data
 - exchange pattern bits **without** changing the pattern's functionality



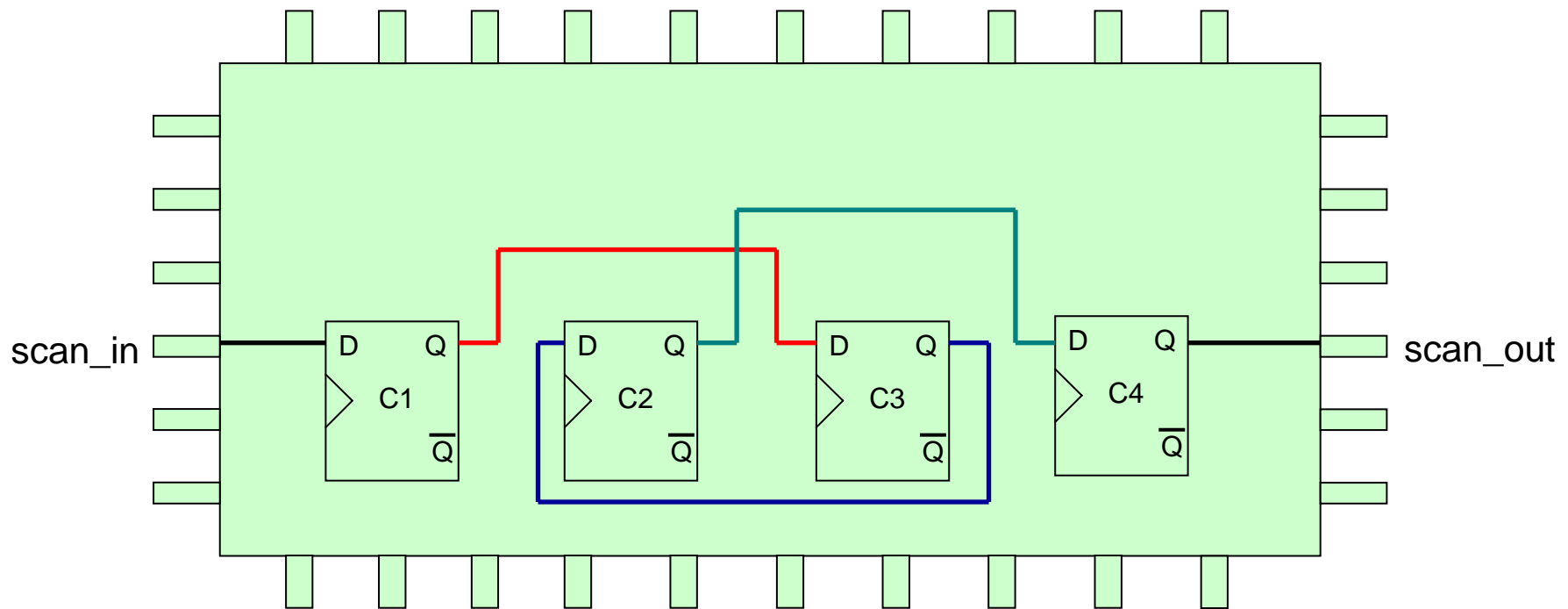
(old)
test pattern1: 0101
test pattern2: 1100

test pattern1: 0011
~~test pattern2: 1100~~

(new)

Scan Chain Reordering

- Idea: reduce the number of runs in the test data
 - exchange pattern bits **without** changing the pattern's functionality



(old)
test pattern1: 0101
test pattern2: 1100

test pattern1: 0011
test pattern2: 1010

(new)

Definition: Frame and Distance

- Frame: a vector of inputs applied to the same scan cell
 - Frame width = # of test patterns
 - # of Frame = # of scan cells
- Distance between 2 frames:
 - extended hamming distance

	F[1]	F[2]	F[3]	F[4]	F[5]
T[1]	1	0	1	X	X
T[2]	X	0	1	0	1
T[3]	0	1	X	0	0

Total Distance Minimization

- Minimize the total distance of the test data
- Method
 - Compute distances between every two frames
 - Construct a complete, simple, undirected graph
 - Vertex: frame
 - Distance: Distance between Vertexes
 - Solve Hamilton Path
 - The shortest path that passes through every vertex just one time
 - NP-hard
 - Greedy algorithm

Algorithm 1 – Scan Chain Reordering (A Simplified Version)

- Input: original frames ($F[1]$, $F[2]$, $F[3]$, ...)
- Output: reordered frames ($F[1]'$, $F[2]'$, $F[3]'$, ...)

- Step 1:
 - $F[1]' \leq F[1]$, and remove $F[1]$ from the original set
- Step n :
 - chose a frame $F[m]$ closest to $F[n-1]'$ from the rest of the original set
 - $F[n]' \leq F[m]$, and remove $F[m]$ from the original set

- Problems:
 - don't-cares in frames will be eventually decided as 0s or 1s
 - frame distance calculated at step n might be inaccurate

Algorithm 1 – Scan Chain Reordering (An Improved Version)

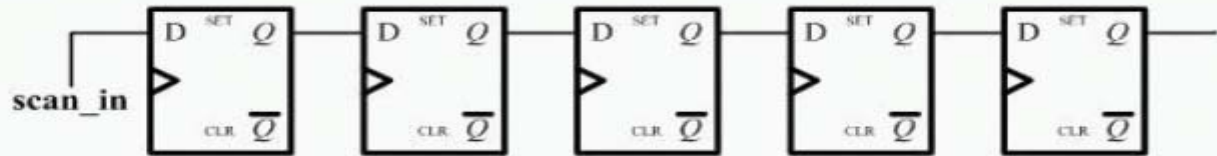
- Idea:
 - maintain a reference frame FR for selecting the closest frame from the original set
 - $FR = f(FR, F[n-1]')$
- Step n:
 - chose a frame $F[m]$ closest to FR from the rest of the original set

		F[n-1]'		
		0	1	X
F R	0	0	X	0
	1	X	1	1
	X	0	1	1

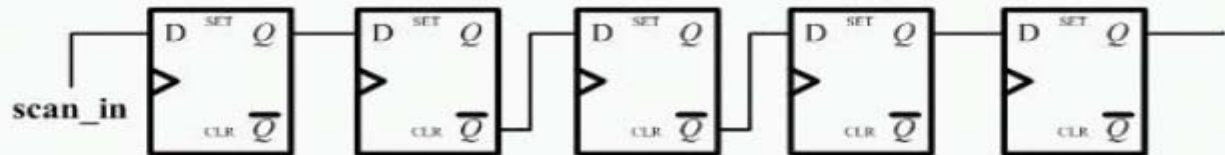
Algorithm 2 -- Scan Polarity Adjustment

- Flip a frame
 - no area overhead, no influence on timing
- Double the original frame set with flipped frames

	i1	i2	i3	i4	i5
t1:	0	0	1	0	0
t2:	1	0	1	0	1
t3:	0	0	0	1	1



	i1	i2	i3	i4	i5
t1:	0	0	0	0	0
t2:	1	0	0	0	1
t3:	0	0	1	1	1



Algorithm 3 – Test Pattern Reordering

- Reorder patterns to reduce runs
- A directed graph
 - vertexes: ZERO, ONE
 - edges:
 - source: last bit of pattern i
 - sink: first bit of pattern i+1
- Minimize ZERO->ONE or ONE->ZERO edges

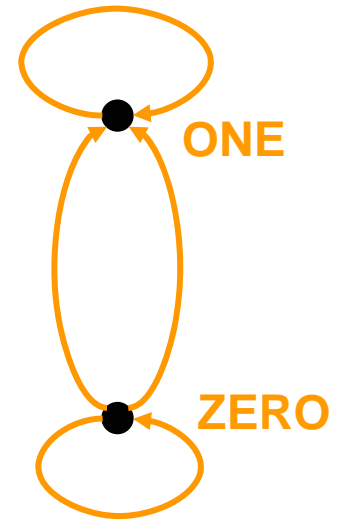
Patterns

011100

010101

001111

100101



Final Algorithm -- RunBasedReordering (RBR)

- Scan chain reordering
- Scan polarity adjustment
- Test pattern reordering

Comparison on Compression Ratio

- Compression Ratio(CR) = $(1-TE/TD)*100\%$

Circuits	TD	# of SC	# of TP	EFDR		SPA		RBR		
				bits	CR(%)	bits	CR(%)	bits	CR(%)	time(s)
s5378f	23754	214	111	11006	53.67	8502	64.21	7469	68.56	0.03
s9234f	39273	247	159	20162	48.66	10608	72.99	11727	70.14	0.07
s13207f	165200	700	236	28932	82.49	18518	88.79	11847	92.83	0.28
s15850f	76986	611	126	24127	68.66	15900	79.35	11477	85.09	0.16
s35932f	28208	1763	16	5415	80.80	13880	50.79	1250	95.57	0.14
s38417	164736	1664	99	62568	62.02	57118	65.33	24746	84.98	0.83
s38584f	19104	1464	136	71121	64.28	53774	72.99	39099	80.36	1.14
Average	-	-	-	-	65.80	-	70.64	-	82.50	-

Comparison on Power consumption

circuits	EFDR		RBR		Power Saving	
	Peak	Avg	Peak	Avg	Peak(%)	Avg(%)
s5378f	11522	3525	3661	717	68.23	79.66
s9234f	14103	4022	4717	899	66.55	77.65
s13207f	94886	7892	9379	590	90.12	92.52
s15850f	70894	13659	12092	1839	82.94	86.54
s35932f	108957	40214	5780	2696	94.70	93.30
s38417f	437935	118077	47399	12292	89.18	89.59
s38584f	481171	86305	115917	18942	75.91	78.05
Average	--	--	--	--	81.09	85.33

Related Work on Scan Chain Reordering

- Conventional
 - save routing resource
 - make adjacent scan cells physically closer
 - check of hold violations of timing
 - adjacent scan cells not too close
- Our purpose
 - data compression
 - power saving

Summary

- The test problem
- A new test data compression technique (RBR)
 - Scan chain reordering
 - Scan polarity adjustment
 - Test pattern reordering
- Experimentation
 - superior than the state-of-the-art
 - compression ratio
 - power consumption

Thank you