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# Systematic Scan Reconfiguration

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# Scan Test Challenges

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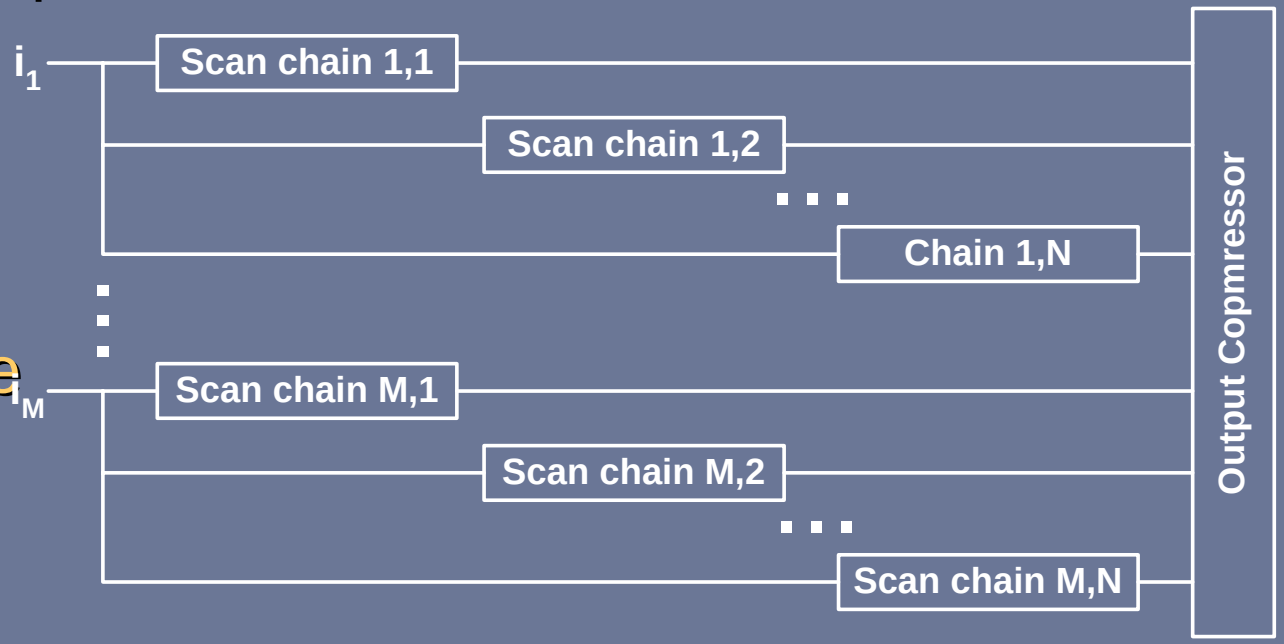
- Test data volume challenge
  - Limited IOs & unlimited increase in transistors
  - Exponential increase in test data volume
- Tester pin count challenge
  - Tester cost is almost linear in number of pins
    - Full accessibility is needed with limited pin count
- Test time challenge
  - Critical path
  - Hard to parallelize test loading massively
    - Limited pin count (accessibility problem)
    - Wiring problem (area/performance constraint problem)
- Test power challenge
  - High activity leading to high power consumption.
    - Circuit may be damaged

# Illinois Scan Architecture

- Segments within a scan chain are compatible
  - load them in parallel
- Otherwise
  - Serially
- Evaluation
  - Data volume
  - Pin count
  - Test time
  - Power consumption



# Limitation

- Illinois Scan
  - Reduction if and only if ALL SEGMENTS ARE COMPATIBLE
- Examples
  - Pattern 1 : 00X10XXX0001XX
    - 1st segment: 00X10
    - 2nd segment: 0XXX0
    - 3rd segment: 001XX

    } COMPATIBLE ⇒ 5 bits only
  - Pattern 2 : 00X10XXX0011XX
    - 1st segment: 00X10
    - 2nd segment: 0XXX0
    - 3rd segment: 011XX

    } NOT COMPATIBLE ⇒ 15 bits

# Segmented Addressable Scan

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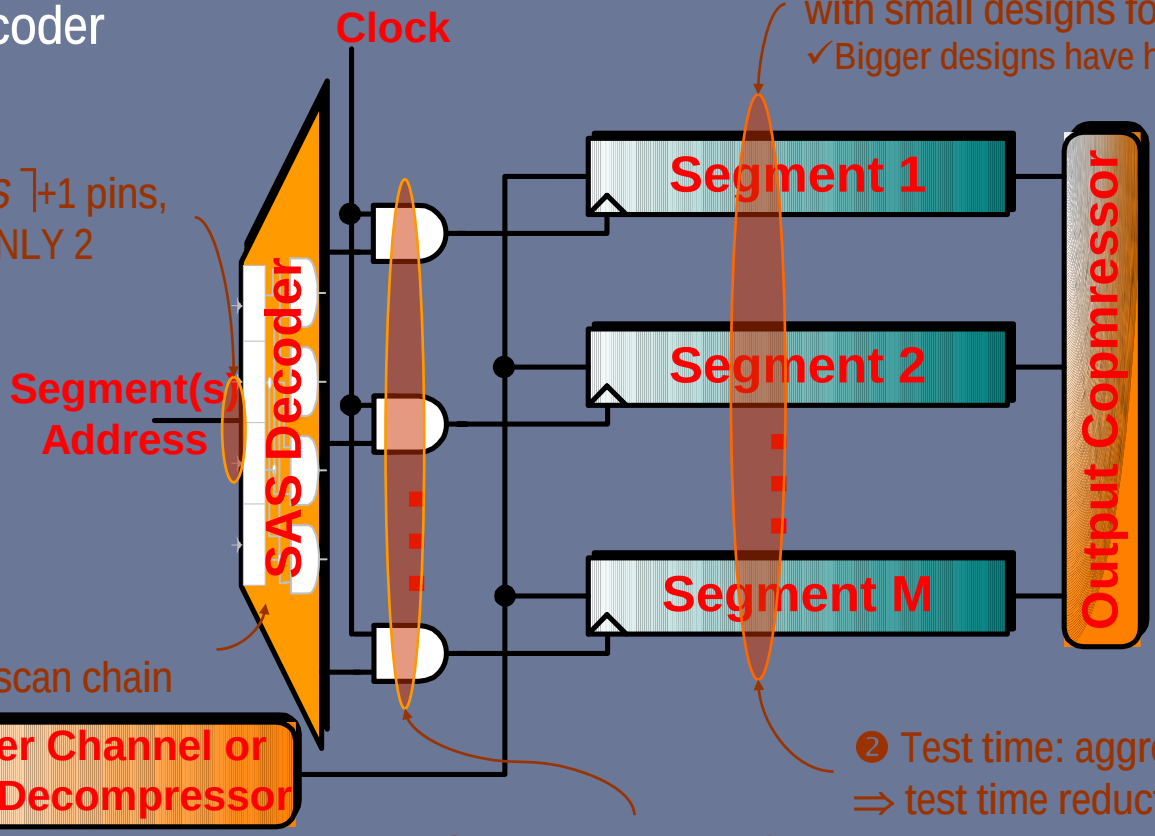
- Aggressive parallelization of scan chains
- Reconfigurable partial compatibilities
- Special SAS decoder

❶ Data volume: 10x ~ 20x compression with small designs for both SAF and TDF
✓Bigger designs have higher compression




❸ Pin count: $2\times\lceil \log_2 S \rceil+1$ pins,
✓can be reduced to ONLY 2

❹ Overhead:
✓few gates per scan chain

❷ Test time: aggressive parallelization
⇒ test time reduction

❺ Power consumption
✓selective clocking

# Avoiding clock gating!

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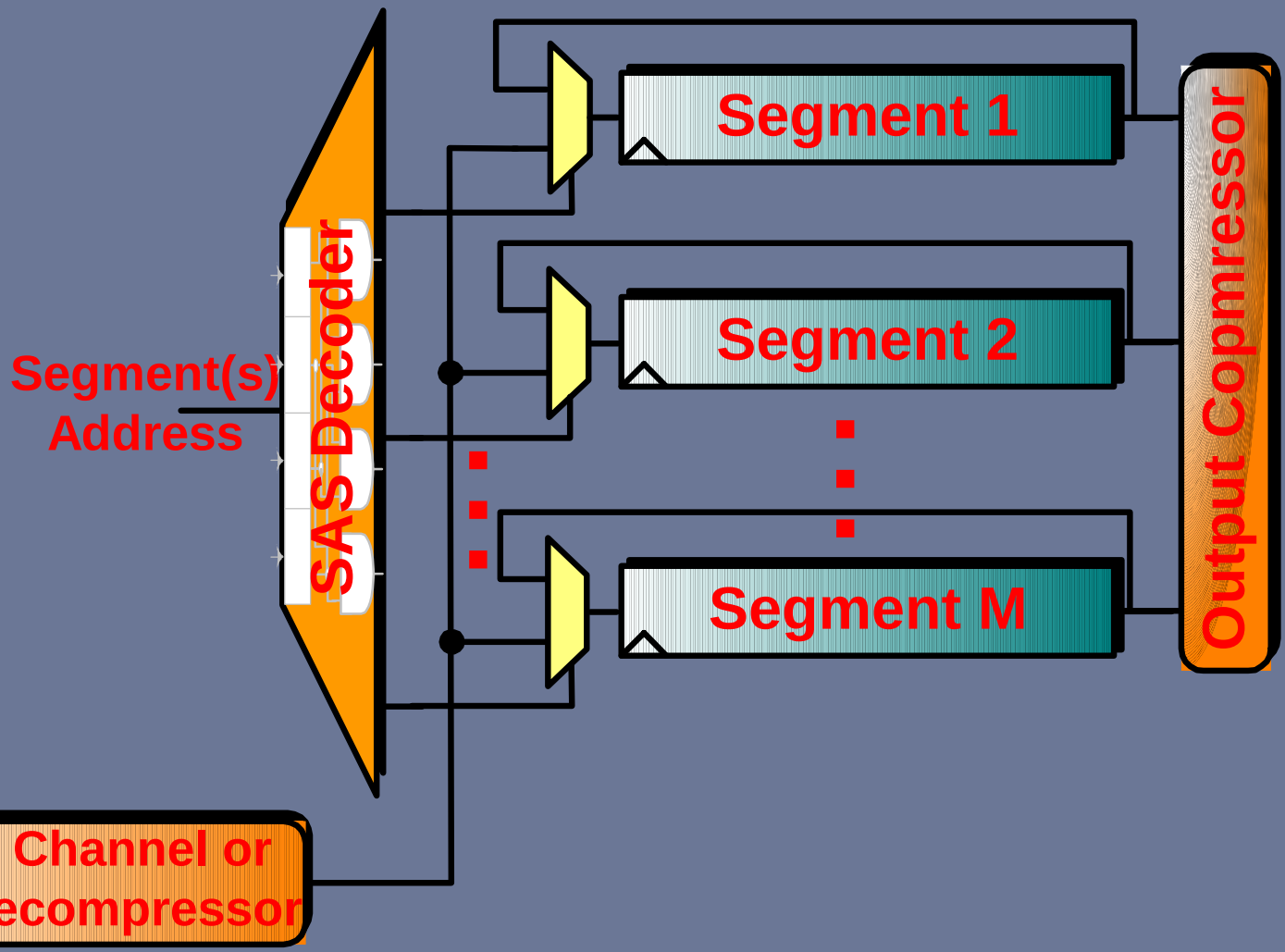

# Systematic Scan Reconfiguration

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- While there are undetected faults
  - Select a set of segments and tie them together
  - Feed that to the ATPG tools with the undetected faults
  - Save the generated patterns and drop the detected faults
- The segments selection should be done in a way that reduces the number of addresses required to cover the patterns
- No need for don’t cares
- The ATPG tool will do the optimization
- Power can be controlled by choosing how many segments to activate at a time

# Example

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- Take 8 segments with addresses (000 through 111)
  - Tie all segments together (Call this class I)
    - Run the ATPG tool to get as many faults as possible
    - Load patterns together and apply them
  - Tie the first four together and last four together (class II)
    - 0dd and 1dd
  - Use these second and third configurations
    - d0d and d1d (tying 0, 1, 4, 5 and 2, 3, 6, 7)
    - dd0 and dd1 (tying 0, 2, 4, 6 and 1, 3, 5, 7)
  - With every configuration
    - Load patterns for the 1st segment
    - Load patterns for the 2nd segment
    - Apply the patterns

# Example

- If you want to cut power consumption by 75%, use the following configurations (class IV)
  - 00d 01d 10d 11d
  - 0d0 0d1 1d0 1d1
  - d00 d01 d10 d11
- Finally, if there any left over faults, get them with serial mode (class VIII)
  - 000 001 010 011 100 101 110 111

# Test Cases

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| | flip-flops | Gate count | Clock domains | Test Patterns |
|---|---|---|---|---|
| Ckt1 | 29K | 350K | 10 | 1.5K |
| Ckt2 | 35.5K | 450K | 26 | 3.4K |

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# Ckt1 – Data Volume & Test Time SAF

| Total Data Volume | | 40 Mb | Compression Ratio |
|---|---|---|---|
| SSR Data Volume | 32 Segments | 3.3 Mb | 12x |
| | 64 Segments | 2.4 Mb | 16x |
| | 128 Segments | 2.0 Mb | 19x |
| | 256 Segments | 1.9 Mb | 21x |

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# Ckt2 – Data Volume & Test Time SAF

| Total Data Volume | | 120 Mb | Compression Ratio |
|---|---|---|---|
| SSR Data Volume | 32 Segments | 7.5 Mb | 16x |
| | 64 Segments | 5.8 Mb | 20x |
| | 128 Segments | 4.8 Mb | 25x |
| | 256 Segments | 3.7 Mb | 32x |

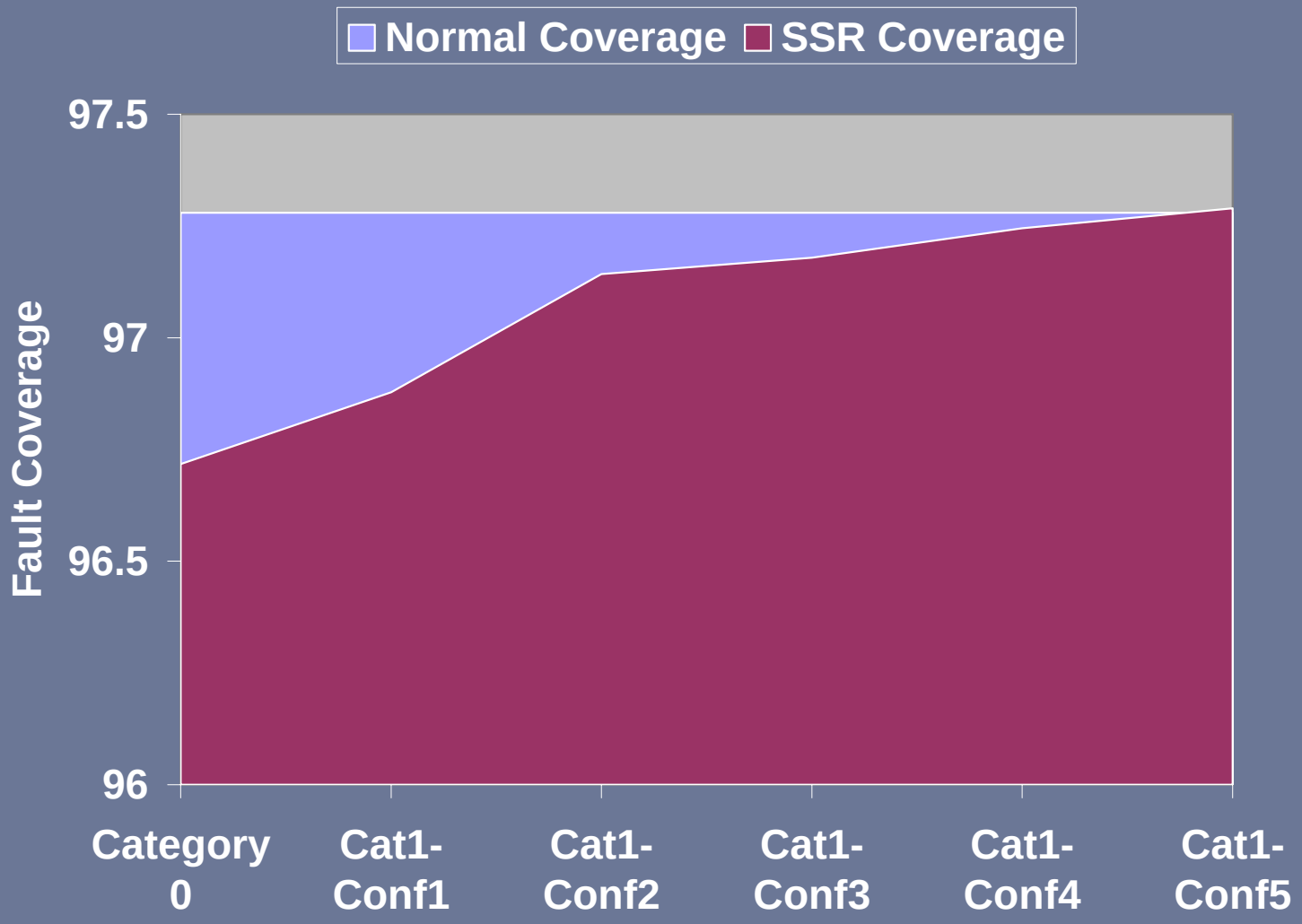
# Ckt1 – Data Volume & Test Time TF

| Total Data Volume | | 98 Mb | Compression Ratio |
|---|---|---|---|
| SSR Data Volume | 32 Segments | 7.7 Mb | 12x |
| | 64 Segments | 5.3 Mb | 18x |
| | 128 Segments | 4.5 Mb | 22x |
| | 256 Segments | 3.6 Mb | 27x |

# Ckt2 – Data Volume & Test Time TF

| Total Data Volume | | 300 Mb | Compression Ratio |
|---|---|---|---|
| SSR Data Volume | 32 Segments | 21.7Mb | 14x |
| | 64 Segments | 14.1Mb | 21x |
| | 128 Segments | 11.8Mb | 25x |
| | 256 Segments | 7.7Mb | 39x |

# SSR Coverage - SAF



# SSR Coverage - transition

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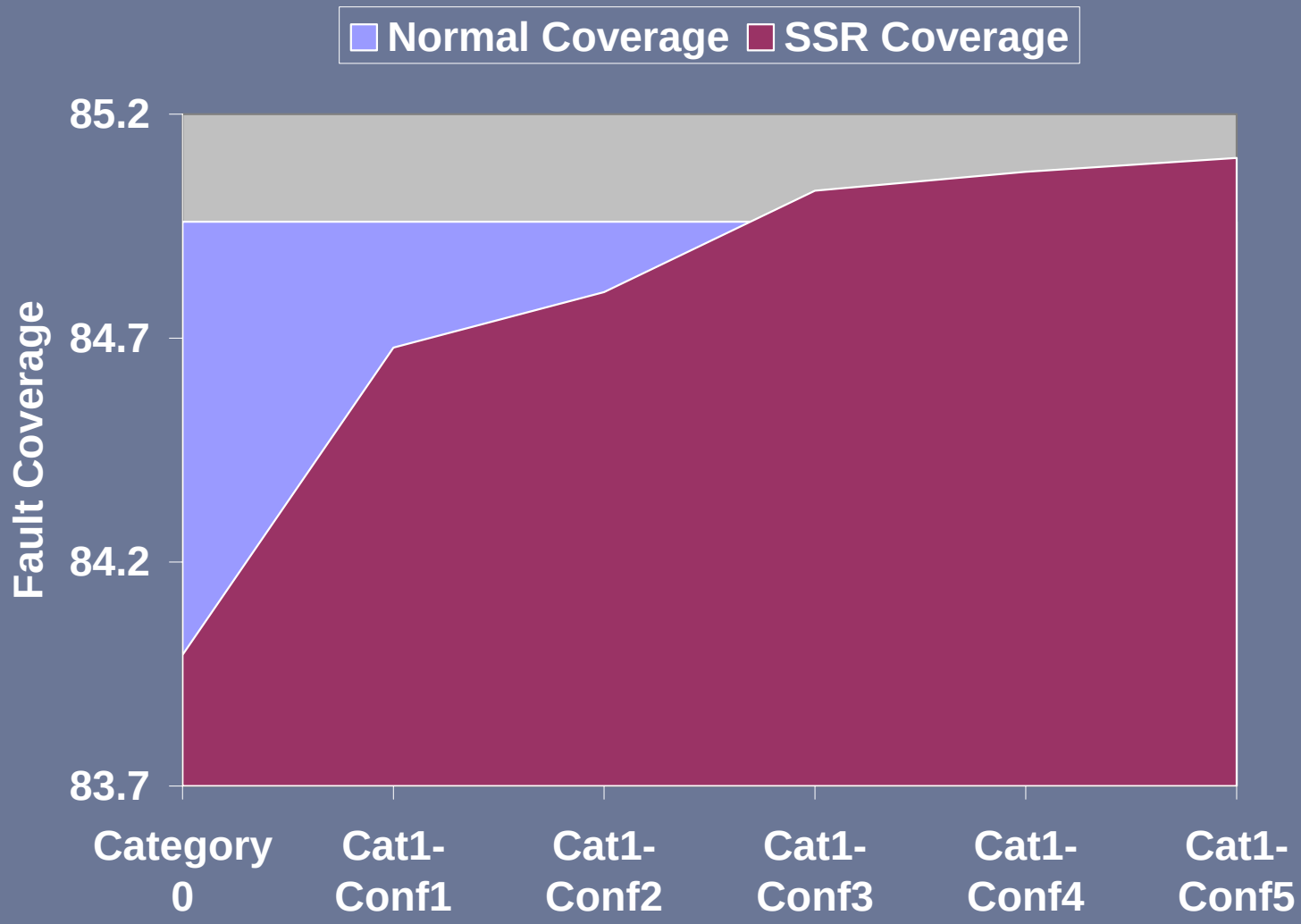

# Runtime

- Runtime is an order of magnitude longer!
- How about reducing the number of configurations?
  - Config-1: All 64 segments connected to one scan input
    - # of faults detected = 1,049,342
    - # of patterns = 3,633
  - Config-2: 64 separate scan chains (serial mode)
    - # of faults detected = 9,358
    - # of patterns = 366
  - 57 + 366 = 423 standard patterns
    - Compared to original 1,381 patterns = 3x data reduction
  - Cutting SAS run time by 50%

# Runtime reduction (SAF)

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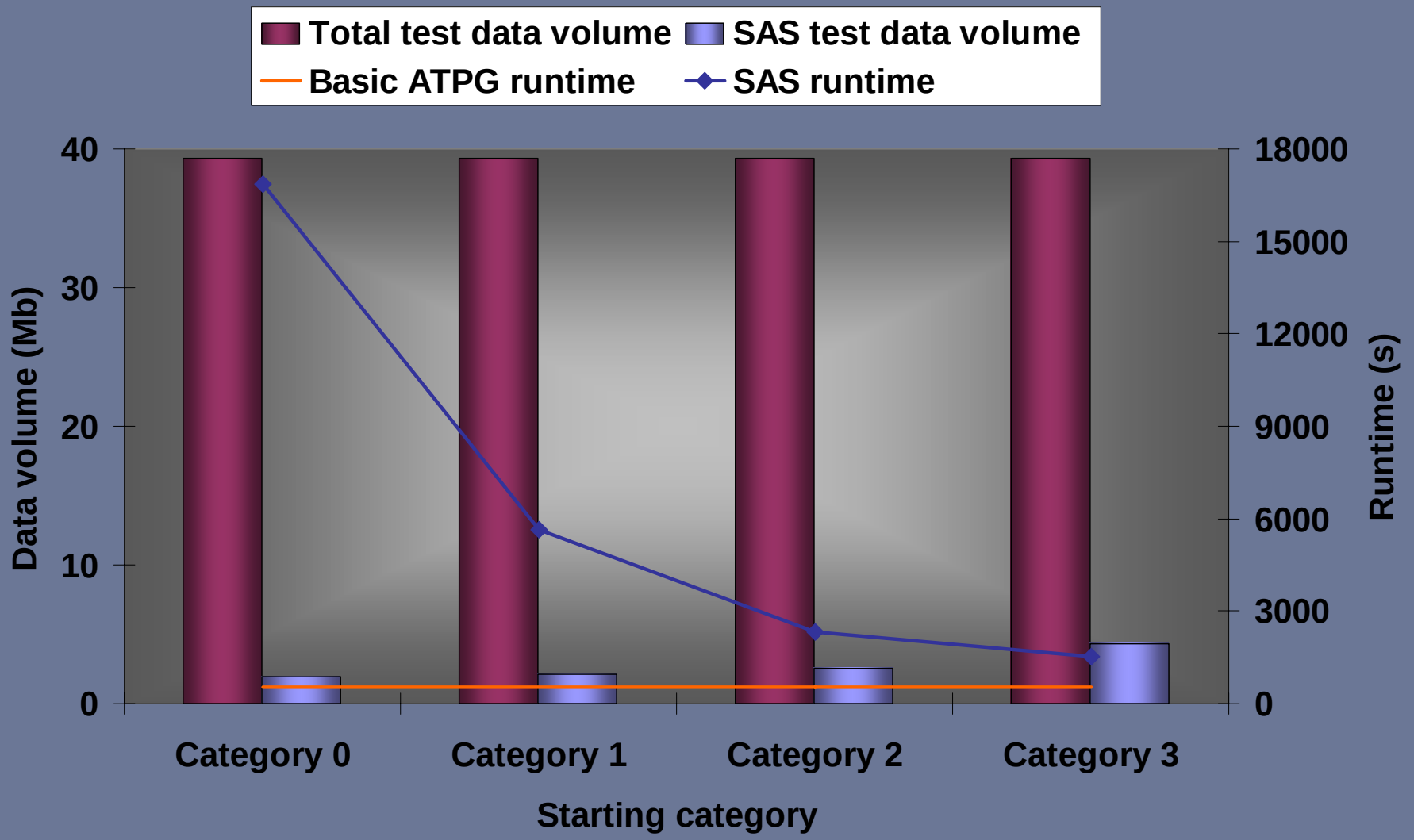

# Runtime reduction (TF)

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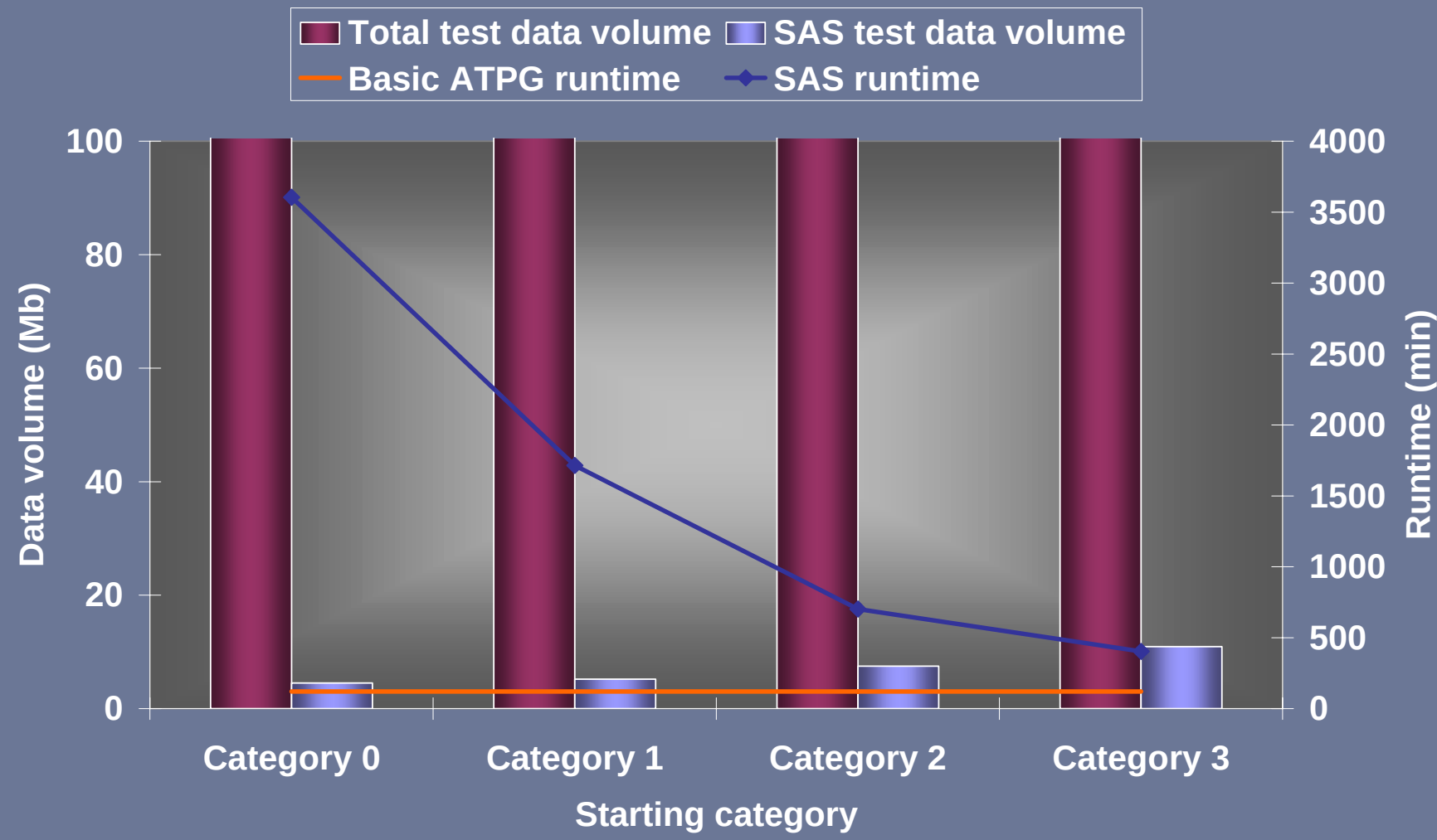

# Power-optimized SAS

$$P = \sum_{n} \frac{1}{2} C_n \Delta V V dd \alpha_n f$$

- Assume, normal shift speed is 20MHz
  - For class I patterns, shift at 20MHz
  - For class II patterns, shift at 40MHz
  - For class IV patterns, shift at 80MHz
  - For class VIII patterns, shift at 160MHz
- If tester is limited to 100 MHz
  - Power-optimized partitioning is class IV
- Speed up by parallelization AND by faster shifting
  - Always *S* speed up factor (*S* = No of segments)

# Conclusion

- Necessity is the mother of invention
- SSR
  - Test data volume
  - Test time
  - Tester pin requirements
  - Power optimized
  - Minimal hardware overhead
  - No don’t care bits requirements